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ABSTRACT

The electrostatic potential variation across etched-and-regrown GaN *p-i-n* diodes for power electronics has been studied using electron holography in a transmission electron microscope. The potential profiles have been correlated with the composition profiles of Mg, Si, and O obtained by secondary ion mass spectroscopy. Electronic charges obtained from the potential profiles correlate well with the presence of Si and O impurities at regrown interfaces. The overlap of Mg and Si when Mg doped GaN is grown directly over an etched undoped GaN surface results in the formation of a highly doped *p-n* junction. The introduction of a thin undoped layer over the etched GaN surface prevents the formation of such a junction as the regrowth interface is moved away from the Mg-doped GaN, and results in diodes with improved reverse leakage currents, close to the best values of continuously grown *p-i-n* diodes. Potential profiles of continuously grown (not etched) *p-i-n* diodes are compared to those of etched-and-regrown diodes.

The fundamental requirements for semiconductors in power electronics applications include wider bandgaps, higher electron mobilities, and high breakdown electric fields.[1] These basic material properties translate into higher switching speeds, lower switching losses, and compact device sizes.[2] Following the success of gallium nitride (GaN) based semiconductors in multiple applications, there is now much interest in developing GaN-based power devices with a vertical architecture. Typically, GaN is grown on foreign substrates like sapphire, silicon, or SiC, with threading dislocation densities (TDD) of $\sim 10^8$–10^{10} cm^{-2}.[3] Vertical devices with high dislocation densities suffer from premature breakdown and higher leakage currents. The recent availability of free standing GaN substrates with a TDD of 10^4–10^6 cm^{-2} has helped realize vertical GaN devices with performance close to the material limit.

The vertical junction field effect transistor (VJFET) is a favored device design, consisting of *p*-GaN as the gate, undoped GaN (*i*-GaN) as the drift region, and *n*-GaN acting as the source and the drain.[4] The GaN-based VJFET has a superior theoretical performance in terms of lower switching losses compared to SiC.[4] The device design requires selective area doping, which can typically be realized via etch-and-regrowth or by ion implantation.[5,6]

For high power devices using the VJFET design, blocking voltages are held between the gate and the drain. Typically, the gate is operated at a small positive voltage, the drain is held at a high positive voltage, and the source region is connected to the ground. This translates to a *p-i-n* structure operating at a high reverse bias voltage. For selective area doped structures realized using the etch-and-regrowth approach, the etched interface is present at or near the *p-i* junction. It has been found that regrowth of Mg-doped GaN directly over an etched *i*-GaN surface results in diodes with lower breakdown voltages.[5,7,8] The introduction of a thin undoped layer over the etched surface before the growth of *p*-GaN recovers the diode performance characteristics to a level comparable to continuously grown (not etched) diodes. It is important to understand the nature of the regrowth interface in order to effectively incorporate dry etching techniques in the fabrication of GaN based power devices. Thin undoped underlayers have been employed in GaN-based light emitting diodes, with improved electrical characteristics.[9,10]

In GaN-based devices, silicon and magnesium are typically used as *n*-type and *p*-type dopants, with dopant activation energies of about 25 meV and 200 meV, respectively.[11] A device quality *n*-GaN is usually doped with $\sim 10^{18}$ cm^{-3}, which results in a donor concentration of the same order of magnitude. For the *p*-type doping, Mg concentrations

of $\sim 10^{19}$ cm^{-3} result in acceptor concentrations of $\sim 2 \times 10^{17}$ cm^{-3} after thermal annealing at about 750 °C, corresponding to 1%–2% ionization.[12] The background impurity concentration in thin films grown by metal-organic chemical vapor deposition (MOCVD) is $\sim 10^{15}$–10^{17} cm^{-3} depending on the condition of the reactor. Thus, the undoped GaN (*i*-GaN) has donor concentrations of that order of magnitude.

In this study, we analyze the electrostatic potential energy profiles across *p-i-n* structures, in order to understand the charge distribution at the various interfaces. The potential profiles provide insight into variations from the intended dopant distribution and the presence of unwanted impurities, leading to the detection of interface trap states introduced by the etch-and-regrowth process. The potential profiles across the interfaces are obtained using electron holography (EH) in a transmission electron microscope (TEM). EH is an interferometric technique that can be used to retrieve the phase and the amplitude shifts of the electron wave within the material with respect to vacuum.[13,14] The phase shift is proportional to the electrostatic potential energy. We show that the etch-and-regrowth introduces charges near the regrowth interface which can be correlated with the presence of impurities. The introduction of a thin undoped layer over the etched surface leads to *p-i-n* junctions with reverse leakage currents equivalent to that of as-grown *p-i-n* junctions, which results from the regrowth interface being moved away from the Mg-doped GaN.

The GaN *p-i-n* structures in this study were grown by MOCVD on *n*-GaN substrates with a carrier concentration of $\sim 10^{18}$ cm^{-3}, at a growth temperature of ~1040 °C. The precursors were trimethyl gallium (TMGa) and ammonia (NH_3), with H_2 as the carrier gas. Bis(cyclopentadienyl)magnesium (Cp_2Mg) and silane (SiH_4) were the sources for Mg and Si.[15] The background impurities for *i*-GaN in our reactor were measured using secondary ion mass spectroscopy (SIMS) to be Si $\sim 6 \times 10^{15}$ cm^{-3}, O $\sim 4 \times 10^{15}$ cm^{-3}, and C $\sim 3 \times 10^{16}$ cm^{-3}.

A chlorine-based inductively coupled plasma (ICP) dry etching recipe (ICP power = 400 W, RF power = 70 W, pressure = 5 mTorr, Cl_2 = 32 sccm, BCl_3 = 8 sccm, Ar = 5 sccm) was used to etch the sample. The surface is then sequentially etched with an RF power of 35 W, followed by 5 W in order to reduce the etch damage. The etching rates for RF powers of 70 W, 35 W, and 5 W are 290, 140, and 20 nm/min, respectively.[5,7] Silicon was used as the carrier wafer. Before the regrowth, the samples were first treated with UV-ozone for 45 min to oxidize the surface. The samples were then immersed in hydrofluoric (HF) acid and hydrochloric (HCl) acid for 5 min each to remove the contaminants.[7]

TEM specimens were prepared by wedge polishing using a tripod polisher and were further thinned down to electron transparency using a 3 keV Ar^+ beam. Silver paste was used to ground the samples to avoid charging due to electron beam irradiation in the TEM. Electron holograms were acquired on an FEI Titan microscope operated at an electron beam accelerating voltage of 300 kV, equipped with a quartz biprism biased at 160 V. The holograms were acquired in a weakly diffracting condition, with the interfaces of interest edge-on. The relative phase shift and the amplitude variation of the electron wave were retrieved using a standard process.[13] The electrostatic potential (V) is calculated from the phase shift ($\Delta\varphi$) using Eq. (1), where C_e is an electron energy dependent constant (0.00653 rad/V.nm for 300 keV electrons), and t is the thickness of the TEM sample. The charge distribution (ρ) is obtained using Poisson's equation in Eq. (2), where ε is the dielectric constant of the material

$$\Delta\varphi = C_e V t, \tag{1}$$

$$\rho = -\varepsilon \nabla^2 V. \tag{2}$$

The built-in potentials at *p-n* junctions measured using electron holography are usually lower than the actual values. This is due to the presence of the electrically dead surface layers and surface states on either side of the thin TEM specimen.[16] The inelastic mean free path value for 300 keV electrons in GaN used in our studies is 100 nm.[17] In our case, the average built-in potential value, experimentally obtained for a standard GaN *p-n* junction, is in the range of 2.5–3 V. For comparison purposes, the energy values on the potential profiles are adjusted for a GaN *p-n* junction built-in potential of about 3.2 eV.

Secondary ion mass spectroscopy (SIMS) was used to simultaneously acquire the Mg and Si profiles from the GaN *p-i-n* structures. SIMS measurements can vary with changing experimental conditions like the choice of energy and the type of the primary ion source, the surface roughness of the crater, the charge neutralization mechanism used, and the ability to reject the signal from the crater walls.[18] The signal broadening depends on all the above-mentioned factors. The SIMS profiles can vary with the experimental conditions, but the trends of dopant distributions are reproducible. Multiple measurements were performed to ensure the repeatability of dopant profile trends that are discussed in this work.

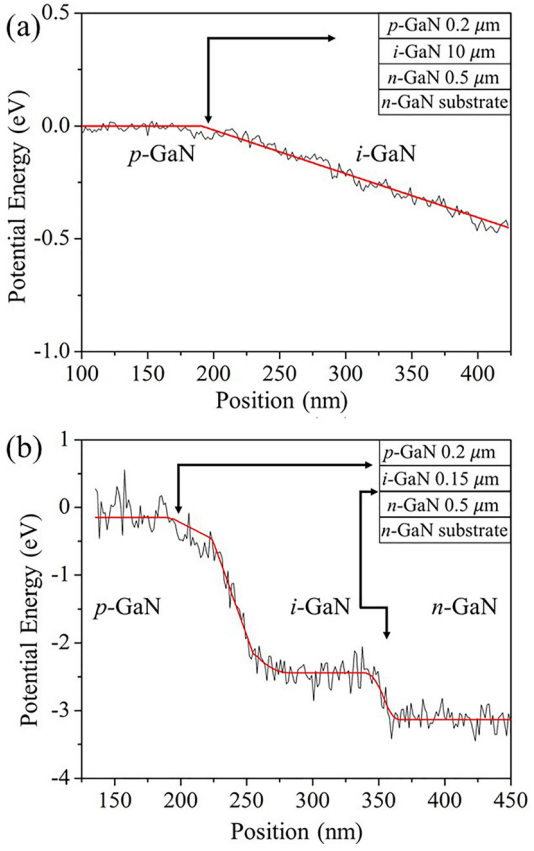

FIG. 1. Electrostatic potential profile for the continuously grown GaN *p-i-n* structures with *i*-GaN layer thicknesses of (a) 10 μm, and (b) 0.1 μm. The inset shows the epilayer structure.

Potential profiles of four structures are reported in this study. Two of them are continuously grown *p-i-n* diodes with different *i*-GaN thicknesses (0.1 μm and 10 μm). The objective is to examine the potential profiles for the as-grown structures, at the *p-i* and the *i-n* interfaces. The other two structures include an etched and regrown interface at the *p-i* junction, one with *p*-GaN directly on top of the etched surface and one with an intermediate 50 nm undoped layer over the etched surface.

Figure 1(a) shows the potential profile at the *p-i* interface of a continuously grown *p-i-n* GaN structure with an *i*-GaN layer of thickness 10 μm.The potential in the *p*-GaN looks flat, indicating the presence of no electric field due to high doping. In the *i*-GaN, we observe a constant electric field of magnitude ~0.003 MV/cm. Figure 1(b) shows the potential profile across a *p-i-n* GaN structure with an *i*-GaN layer of thickness 0.15 μm. A step in the potential profile is observed at the *i-n* interface with a flat potential in the *i*-GaN region directly above the *n*-GaN.

Figure 2(a) shows the potential energy profile at the *p-i* junction with an etched interface between the *p*-GaN and the *i*-GaN, with features that indicate a ~10^{19} cm^{-3} electronic charge accumulation on each side of the interface [calculated using Eq. (2)]. Figure 2(b) shows a SIMS depth profile indicating that the regrowth interface region has an overlap of Mg, Si, and O with peak concentrations of ~2×10^{19} cm^{-3}, ~3×10^{19} cm^{-3}, and ~3×10^{17} cm^{-3}, respectively. The significant broadening of the Mg, Si, C, and O signals at the regrowth interface is due to surface roughening and cascade mixing during the SIMS sputtering process.[18] This indicates that the introduction of an ICP etching step causes the accumulation of Si and O impurities at the etched-and-regrown interface. Figure 3 shows the SIMS profiles for Mg in the *p-i* junctions with an etched interface for different Mg concentrations in the *p*-GaN films. Each profile shows a local maximum in the Mg concentration at the etched interface, which indicate some form of gettering of Mg. Cross sectional TEM images exhibit precipitates at the *p-i* junctions with an etched interface for all Mg concentrations, which are probably associated with the Mg local maxima in the SIMS profiles. Figure 4(a) shows the potential profile across a *p-i* junction that contains an undoped GaN layer of thickness 50 nm deposited on an etched *i*-GaN layer. The dip in the potential profile at the regrown interface indicates the presence of a positive sheet charge, surrounded by the negatively charged regions, which are indicated in the figure. Figure 4(b) shows the SIMS profiles of Mg and Si for the sample in Fig. 4(a). The Si accumulation due to the regrowth process is shifted from the Mg, compared to the sample in Fig. 2(a), due to the introduction of a 50 nm intermediate undoped layer.

In the case of the continuously grown *p-i-n* GaN structures, with a 10 μm thick *i*-GaN layer in Fig. 1(a), we observe a uniform electric field in the *i*-GaN layer near the *p-i* junction. The potential variation near the *i-n* interface may be understood as a result of the relative concentrations of carbon and silicon impurities in the *i*-GaN (from SIMS measurements). It has been reported that if [C] > [Si] in GaN, the Fermi level is pinned midgap.[19] This is because the formation energy of C_{Ga} (donor) becomes equal to C_N (acceptor), effectively pinning the Fermi level as it approaches midgap. The potential profile in the *i*-GaN layer follows the evolution of the Fermi level inside the bandgap. For a thicker *i*-GaN layer, as in the case of Fig. 1(a), the potential in the *i*-GaN near the *p-i* interface has a uniform slope because of a large depletion width.

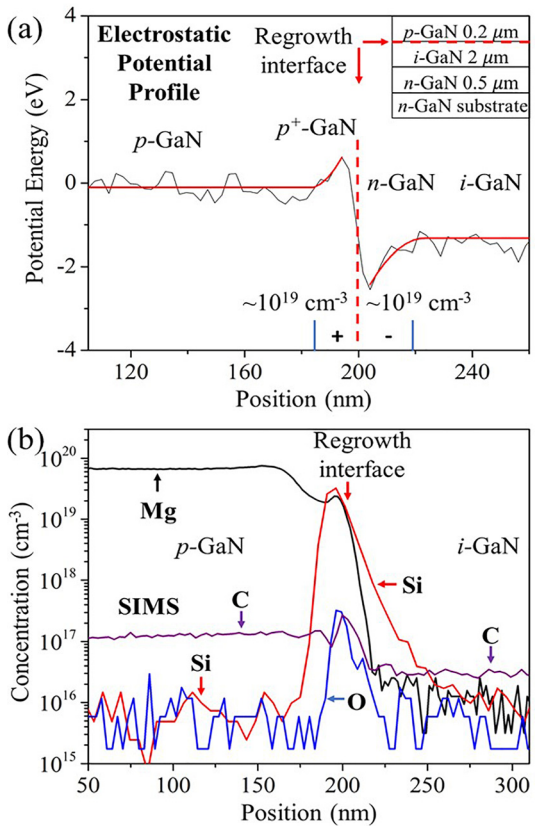

FIG. 2. Electron holography and SIMS profiles of the *p-i* interface of an etched-and-regrown grown GaN *p-i-n* structure. The inset shows the epilayer structure. (a) Electrostatic potential profile indicating the accumulation of a negative charge at the *i*-GaN and a positive charge at the *p*-GaN regions next to the *p-i* interface. The estimated charge densities near the regrowth interfaces are indicated on the image. (b) SIMS profiles of Mg, Si, C, and O at the *p-i* interface of an etched-and-regrown GaN *p-i-n* structure corresponding to Fig. 2(a). Notice the peak in the Mg concentration indicating an Mg accumulation at the regrowth interface. The broadening of the signals at the regrowth interface is an artifact of the SIMS measurements.

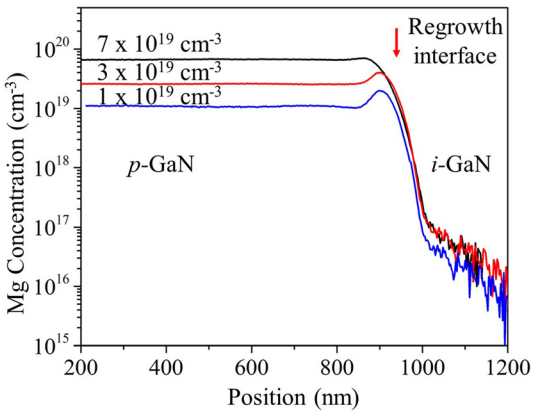

FIG. 3. SIMS profiles of Mg at the *p-i* interface of the etched-and-regrown GaN *p-i-n* structures corresponding to the *p*-GaN layers with Mg concentrations of 1, 3, and 7×10^{19} cm^{-3}. Notice the peak in the Mg concentration indicating an Mg accumulation at the regrowth interface.

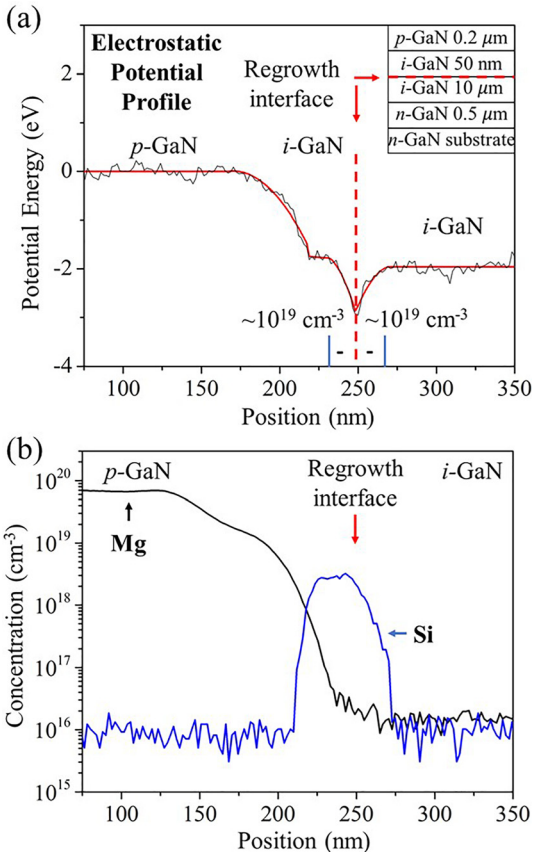

FIG. 4. The etched-and-regrown GaN *p-i-n* structure with a 50 nm undoped GaN insertion layer. The inset shows the epilayer structure. (a) Electrostatic potential profile of the *p-i* interface. Charges near the regrowth interfaces are indicated. (b) SIMS profiles of Mg and Si in the region corresponding to Fig. 4(a). The broadening of the Mg and Si signals at the regrowth interface is due to surface roughening, and cascade mixing during the SIMS sputtering process.

Etch-and-regrowth structures are very different from continuously grown structures. The etch-and-regrowth involves several steps: a growth interruption, removal from the growth chamber, transfer to an etching chamber, the etching process itself, surface treatment to remove any possible damage and contamination, and reinsertion into the MOCVD chamber for the growth of subsequent layers. SIMS measurements on the etched-and-regrown structures show an accumulation of $\sim 10^{18}$–10^{19} cm^{-3} of Si and O impurities at the regrowth interface, as observed in Fig. 2(b). Anomalous impurity accumulation has been reported earlier.[20,21] In one particular study, impurity accumulation has been investigated for a variety of growth interruptions, including retaining the wafer in the growth chamber, exposure to air, and etching the surface prior to regrowth.[21] In all cases, impurity accumulation in the range of 10^{17}–10^{19} cm^{-3} of Si and O was reported at the regrowth interfaces. The origin of this impurity accumulation is not well understood. Given that a simple growth interruption can result in such an accumulation, we can rule out the possibility of etching being the only reason for the presence of impurities. It is possible that the impurities on the walls of the MOCVD chamber condense onto the growth surface during the interruption. Also, the SIMS profiles of Mg [Fig. 2(b)] near the etched and regrown interfaces suggest Mg gettering, which is likely associated with the precipitates typically observed by TEM at the etched interface. The presence of high levels of Si at the regrowth interface may influence Mg gettering and Mg precipitate formation.

In Fig. 2(a), where *p*-GaN is grown directly over the etched *i*-GaN surface, the SIMS analysis shows the presence of Mg, Si, and O on the *p*-GaN side of the interface [Fig. 2(b)]. The downward curvature of the potential profile on the *i*-GaN side of the interface is related to the presence of Si and O, which may act as donors on the *i*-GaN side of the regrowth interface, turning it into *n*-type GaN. The overlap of Mg, Si, and O impurities could lead to a case where *p*-GaN is codoped close to the etched interface region. It has previously been reported that codoping Mg doped GaN with Si or O can lead to an enhancement in hole concentration by up to two orders of magnitude.[22] The increase in hole concentration would result in an upward curvature in the potential profile on the *p*-GaN side of the etched interface. Codoping is a complex phenomenon where multiple factors play a role in the enhancement of the hole concentration of the *p*-GaN film. The formation of the acceptor-donor-acceptor (ADA) complexes has been proposed to result in increased hole concentrations due to lower ionization energies for such complexes.[22] Predictions for hole concentrations using the ADA complex model match well with the experimental data for Si-Mg and O-Mg codopings.[22] Thus, the etch-and-regrown region behaves like a p^+-n^+ junction which may be due to codoping on the *p*-GaN side and a highly Si-doped region on the *i*-GaN side. This would explain the reported temperature independent I-V diode characteristics under reverse bias that suggest tunneling as the transport mechanism.[5] In a recent study on doping profiles in GaN tunnel junctions, it was found that the overlap of Mg and Si at the interface leads to low resistive tunnel junctions.[23] A tunnel junction would result in high reverse leakage currents, which is undesirable for power applications.

In the case of an etched *p-i* junction with a 50 nm undoped GaN layer over the etched surface before regrowth of *p*-GaN layer [Fig. 4(a)], the potential profile indicates the presence of a fixed positive sheet charge at the regrowth interface. The presence of Si impurities (3×10^{18} cm^{-3}) at the regrowth interface [Fig. 4(b)], measured by SIMS, acts as shallow donors resulting in the formation of a thin *n*-type layer sandwiched between the 50 nm insertion layer and the *i*-GaN layer beneath. C-V measurements on similar structures indicate the presence of $\sim 10^{19}$–10^{20} cm^{-3} positive charges at the regrowth interface.[5] The addition of an undoped layer on top of the etched surface helps move the defective regrowth interface away from the *p-i* junction and prevents codoping as in the case of Fig. 2(a). The diode reverse leakage currents (5 nA at 600 V) with the insertion layer were close to as-grown *p-i-n* structures (1 nA at 600 V). More in-depth studies about the electrical characterization can be found in Refs. 5 and 7.

The ICP etching process was reported to produce non-stoichiometric surfaces in GaN.[24,25] The presence of deep donors ($\sim 1 \times 10^{20}$ cm^{-3} to an estimated depth of 8 nm) and deep acceptors near the surface was reported for ICP etched *p*-GaN and *n*-GaN surfaces, respectively.[24–26] The charge concentration obtained from our potential profiles near the regrowth interface is consistent with these reports.

In summary, we have found a close correlation between the electrostatic potential profiles obtained by electron holography and the

composition profiles obtained by SIMS. A uniform electric field is present in the *i*-GaN near the *p-i* interface for a 10 μm thick *i*-GaN layer. The etch and regrowth process results in the accumulation of Si and O at the regrowth interface. The growth of the Mg-doped GaN directly over the etched surface results in the formation of a highly doped *p-n* junction. The introduction of an insertion layer prevents such a junction, as observed in the potential profiles. In the design of power electronics, care should be taken to consider these effects.

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