Ultra-low turn-on voltage and on-resistance vertical GaN-on-GaN Schottky power diodes with high mobility double drift layers

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Ultra-low turn-on voltage and on-resistance vertical GaN-on-GaN Schottky power diodes with high mobility double drift layers

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This letter reports the implementation of double-drift-layer (DDL) design into GaN vertical Schottky barrier diodes (SBDs) grown on free-standing GaN substrates. This design balances the trade-off between desirable forward turn-on characteristics and high reverse breakdown capability, providing optimal overall device performances for power switching applications. With a well-controlled metalorganic chemical vapor deposition process, the doping concentration of the top drift layer was reduced, which served to suppress the peak electric field at the metal/GaN interface and increase the breakdown voltages of the SBDs. The bottom drift layer was moderately doped to achieve low on-resistance to reduce power losses. At forward bias, the devices exhibited a record low turn-on voltage of 0.59 V, an ultra-low on-resistance of 1.65 $m\Omega\,cm^2$, a near unity ideality factor of 1.04, a high on/off ratio of $\sim 10^{10}$, and a high electron mobility of 1045.2 $cm^2/(V\,s)$. Detailed comparisons with conventional single-drift-layer (SDL) GaN vertical SBDs indicated that DDL design did not degrade the forward characteristics of the SBDs. At reverse bias, breakdown voltages of the DDL GaN SBDs were considerably enhanced compared to those of the conventional SDL devices. These results showed that GaN vertical SBDs with DDL designs are promising candidates for high efficiency, high voltage, high frequency power switching applications. *Published by AIP Publishing.* https://doi.org/10.1063/1.4993201

Wurtzite III-nitride semiconductors have been extensively investigated in optoelectronics[1–11] and high electron mobility transistors (HEMTs).[12,13] Recently, GaN based power diodes such as p-n diodes[14–17] and Schottky diodes[18] have gained considerable attention for power switching applications due to their high frequency capability and large critical electrical field. However, conventional GaN power diodes were heteroepitaxially grown on foreign substrates such as sapphire,[19–22] which led to large dislocation densities ($>10^9\,cm^{-2}$) in the materials. These dislocations serve as current leakage pathways and reduce the breakdown voltage (V_{BD}) of the devices.

Recently, due to advancements in GaN crystal growth, bulk GaN substrates with dislocation densities of $<10^6\,cm^{-2}$ have become commercially available,[4,5,23] which enable homoepitaxial growth of GaN power diodes with much reduced dislocation densities and improved performance. For example, Kizilyalli *et al.*[14] reported a vertical GaN-on-GaN PN diode with a V_{BD} of 3.7 kV using a GaN single drift layer (SDL). Furthermore, Ohta *et al.*[15] proposed a multi-drift-layer (MDL) design for GaN PN diodes, which increased the V_{BD} of the device to 4.7 kV. Despite these encouraging results, GaN PN diodes typically have a very large turn-on voltage (V_{ON}) of >3 V,[16] which leads to large power loss for power switching applications. The two main loss mechanisms in a power switch are conduction loss (P_C) and switching loss (P_S).[24] P_C is expressed as $(IV_{ON}+I^2R_{ON})$, where V is the forward voltage, I is the current, and R_{ON} is the on-resistance of the devices. The large V_{ON} of GaN PN diodes will induce a large P_C. P_S is given by $[IV(T_R+T_F)f]$, where T_R is the rise time, T_F is the fall time, and f is the switching frequency. Since GaN PN diodes are minority carrier devices, they will have very large T_R, T_F, and therefore P_S, due to the reverse recovery charge during on/off transition. To minimize these power losses, new device structures must be explored for GaN power diodes.

GaN vertical Schottky barrier diodes (SBDs) are ideal candidates for efficient low loss power switching. Due to the Schottky barrier interface, SBDs can achieve small V_{ON} (usually <1 V) and therefore reduce P_C. Furthermore, because SBDs are majority devices and have no reverse recovery charge, P_S can also be eliminated. Despite these advantages, to date there have been only limited reports on GaN vertical SBDs, and their performances (e.g., V_{BD} and R_{ON}) are still inferior to those of GaN vertical PN diodes. This is mainly due to the following two challenges: The first challenge is the growth of high quality thick GaN drift layers and precisely controlling the doping concentrations,[18] which has been partially solved by metalorganic chemical vapor deposition (MOCVD) growth optimizations. The second challenge is the device design to balance R_{ON} and V_{BD}. While low R_{ON} requires thin and highly doped drift layers, high V_{BD} has the opposite requirements. The solution to this problem is to introduce MDL design into GaN vertical SBDs. It has already been shown in GaN PN diodes that reducing the doping concentration of the top drift layer can suppress the peak electric field at the junction and thus enhance V_{BD}. At the same time, the bottom drift layer can be moderately doped to achieve low R_{ON}.[15] The same principle can also be applied to SBD devices. Figure 1 illustrates how double drift layer (DDL) structures can increase the V_{BD} in SBDs, where the properties of the top drift layer (doping, thickness, etc.) play significant

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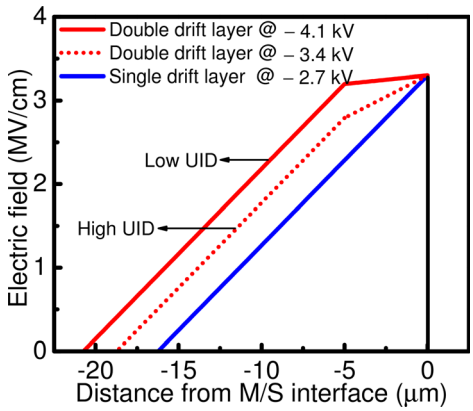
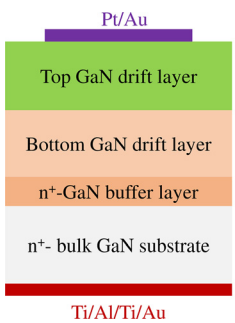


FIG. 1. Theoretical calculation of electric fields by one-dimensional Poisson's equation for the SDL structure biased at −2.7 kV, the DDL structure with the high unintentionally doping (UID) top drift layer biased at −3.4 kV, and the DDL structure with the low UID top drift layer biased at −4.1 kV. The top drift layer was 5 μm thick. A carrier concentration of $5\times10^{15}\,cm^{-3}$ was used for high UID and $10^{15}\,cm^{-3}$ for low UID. The Si concentration of $2\times10^{16}\,cm^{-3}$ was used for the bottom drift layer with compensation considered. Breakdown was assumed to occur at a peak electric field of 3.3 MV/cm. The horizontal axis was the distance from the metal/semiconductor interface. The kinks in the electric field profile were due to different doping concentrations in the DDL structures.

roles. In this work, we demonstrate a vertical GaN-on-GaN SBD with DDL, whose device performances are comprehensively compared with conventional GaN SBDs with SDL. The results indicate that GaN DDL SBDs can achieve low V_{ON}, low R_{ON}, and high V_{BD} simultaneously, which are ideal for high efficiency, high voltage, and high frequency power switching applications.

GaN SBD epilayers were grown by conventional MOCVD on n^+-GaN bulk substrates with a carrier concentration of $1.6\times10^{18}\,cm^{-3}$ supplied by Sumitomo Electric Industries Ltd. The Ga and N sources were trimethylgallium (TMGa) and ammonia (NH_3), respectively. Diluted silane (SiH_4) was used as the precursor for the n-type Si dopant. The carrier gas was hydrogen (H_2). More information about growth methods can be found elsewhere.[1] Figure 2 shows the schematics of device structures for diode A and diode B. Diode A consists of a 400 nm n^+-GaN buffer layer ($[Si]=2\times10^{18}\,cm^{-3}$) and a 9 μm lightly doped ($[Si]=2\times10^{16}\,cm^{-3}$) GaN SDL. Diode B is comprised of DDLs on top of the same GaN buffer layer as diode A. The total thickness of the double drift layers is kept at 9 μm, the same as diode A. The top drift layer is a 5-μm-thick unintentionally doped (UID) GaN layer, and the bottom



	Samples	
Layer description	Diode A	Diode B
Top GaN drift layer	NA	5μm, UID
Bottom GaN drift layer	9μm, $[Si]=2\times10^{16}\,cm^{-3}$	4μm, $[Si]=2\times10^{16}\,cm^{-3}$
n^+-GaN buffer layer	400nm, $[Si]=2\times10^{18}\,cm^{-3}$	400nm, $[Si]=2\times10^{18}\,cm^{-3}$
Substrate	n^+- bulk GaN substrate	

FIG. 2. Schematic view of the cross-section of the GaN SBDs (left) and detailed description of each layer (right) for diode A and diode B.

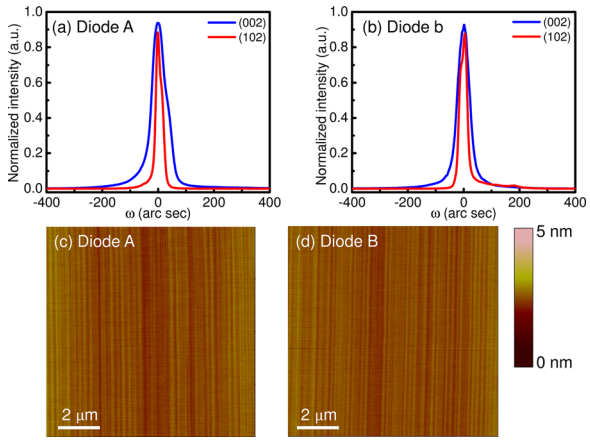


FIG. 3. Rocking curves of the (002) plane and (102) plane by HRXRD for (a) diode A and (b) diode B. (c) and (d) AFM images (10 μm × 10 μm) of diode A (c) and diode B (d).

drift layer is a 4 μm lightly doped ($[Si]=2\times10^{16}\,cm^{-3}$) GaN layer. The n-type conductivity of the UID drift layer can be controlled via tuning the MOCVD growth parameters such as V/III ratio and growth pressure and reducing the background impurities.[25]

Before device fabrication, the crystal quality of as-grown samples was characterized by the high resolution X-ray diffraction (HRXRD) measurement using the PANalytical X'Pert Pro materials research X-ray diffractometer (MRD) system using Cu Kα radiation with a wavelength of 0.154 nm. The incident and diffracted beam optics were hybrid monochromator and triple axis module, respectively. Figures 3(a) and 3(b) show the (002) symmetric and (102) asymmetric plane rocking curves (RCs) of the two samples. For diode A, the full width at half maximum (FWHM) of (002) RC was 60 arc sec and the FWHM of (102) RC was 26 arc sec. For diode B, they were 50 arc sec and 32 arc sec, respectively. It is worth mentioning that the (102) FWHM is smaller than the (002) FWHM for both samples. This is quite unusual in GaN on foreign substrates but commonly seen in high quality GaN epilayers grown on bulk GaN substrates.[18] The dislocation density of the samples can be estimated using the following equation:[26,27] $D=\frac{\beta^2_{(002)}}{9\vec{b}_1^{-2}}+\frac{\beta^2_{(102)}}{9\vec{b}_2^{-2}}$, where β is the FWHM and $\vec{b}$ is the Burgers vector. The first term represents the screw dislocation density, and the second term is the edge dislocation density. In both samples, the screw dislocation dominates. Both samples have dislocation densities in the low $10^6\,cm^{-2}$ range, which are significantly lower than that of typical GaN devices grown on sapphire ($>10^9\,cm^{-2}$). The surface morphology of diode A and diode B were also examined by Bruker Dimension atomic force microscopy (AFM), and the results are shown in Figs. 3(c) and 3(d). The root-mean-square (RMS) roughness of the scanning area of $10\times10\ \mu m^2$ of the samples was 0.15 nm for diode A and 0.13 nm for diode B. Table I summarizes the material properties of the as-grown samples. HRXRD and AFM results indicate that high quality GaN epilayers with low dislocation density and good surface morphology were obtained on bulk GaN substrates.

The GaN SBDs were fabricated using conventional optical photolithography and lift-off processes. The as-grown

TABLE I. Material characterization results of diode A and diode B by HRXRD and AFM.

Sample	(002) FWHM (arc sec)	(102) FWHM (arc sec)	Screw dislocation ($\times 10^6$ cm^{-2})	Edge dislocation ($\times 10^6$ cm^{-2})	RMS (nm)
Diode A	60	26	3.5	0.2	0.15
Diode B	50	32	2.4	0.3	0.13

samples were cleaned in acetone and isopropyl alcohol under ultrasonic and dipped in hydrochloric acid before metal deposition to remove native oxides on the surface. The chlorine based inductively coupled plasma (ICP) dry etch at an ICP power of 350 W and a pressure of 5 mTorr was used to define the mesa isolation with an etching depth of $\sim$1 μm. For the Schottky contact (diameter of 200 μm), Pt/Au (30 nm/120 nm) metal stacks were deposited by electron beam evaporation. For n-type ohmic contact, non-alloyed Ti/Al/Ti/Au (20 nm/50 nm/20 nm/100 nm) stacks were formed at the backside of the GaN bulk substrate using electron beam evaporation without thermal annealing. No passivation, field plate (FP) or edge termination technologies were employed in the devices. The electrical measurements were performed on a probe station with a thermal chuck. The capacitance-voltage (C–V) characteristics were measured using the Keithley 4200-SCS parameter analyzer at room temperature (RT). The current-voltage (I–V) characteristics were obtained using the Keithley 2410 sourcemeter. The reverse breakdown measurements were performed at RT in electronically insulating Fluorinert liquid FC-70.

Figure 4(a) shows the forward I–V characteristics of the two devices at RT on a linear scale. The upper current limit of the measurement setup is 0.1 A. The forward current is over 0.1 A at a voltage larger than 1.0 V (diode A) or 1.2 V (diode B). Diode A turned on at $\sim$0.52 V, and diode B turned on at $\sim$0.59 V. Both devices demonstrated record low V_{ON} values for vertical GaN-on-GaN diodes. The ideality factor n as a function of voltage was also extracted by[18]

$$n = \frac{q}{kT}\frac{1}{d\log(J)/dV}, \tag{1}$$

where q is the electron charge, k is the Boltzmann constant, T is the temperature, and J is the current density. Near unity idealities were obtained for both diodes at low bias: $n = 1.06$ for diode A and $n = 1.04$ for diode B, which indicate nearly ideal GaN SBDs. In Fig. 4(b), the current density and differential specific on-resistance (dV/dI) were plotted as a function of voltage on a semi-log scale. The off current densities of both devices is below 10^{-7} A/cm^2, limited by the apparatus lower current limit of 0.1 nA. Both diodes showed a high on/off ratio on the order of 10^{10}, which is among the highest values demonstrated in vertical GaN power diodes. At the current of 0.1 A, diode A has a R_{ON} of 1.39 mΩ cm^2, while diode B has a slightly larger R_{ON} of 1.65 mΩ cm^2 due to the lack of electrons in the top drift layer. Figure 4(c) compares the obtained V_{ON} and R_{ON} with previous reports,[18,28–30] where the devices in this work showed considerable improvements. R_{ON} consists of several components and is given by[18]

$$R_{ON} = R_{SUB} + R_{SBD} + R_{CON} = R_{sh}d^2 + t/q\mu N + R_{CON}, \tag{2}$$

where R_{SUB}, R_{SBD}, and R_{CON} are the resistance of the substrate, the SBD, and the contact, respectively, R_{sh} is the sheet resistance of the substrate, d is the thickness of the substrate, and t, μ, and N are the thickness, the electron mobility, and the free carrier concentration of the drift layers of GaN SBDs. The R_{SUB} of our devices was 0.47 mΩ cm^2. Since the resistance from the contact is expected to be much less than R_{SUB} and R_{SBD},[18] R_{CON} can be neglected. The electron mobility of the drift layers of diode A was calculated to be 886.1 cm^2/(V s) and that of diode B was 1045.2 cm^2/(V s), which are close to the highest mobilities reported in GaN drift layers of vertical GaN diodes.[18,28–30] Diode A had a lower electron mobility possibly due to stronger impurity scattering from silicon dopants. These results indicated that GaN SBDs with DDLs could have forward device characteristics comparable to, if not better than, SDL GaN SBDs in terms of V_{ON}, R_{ON}, n, and μ.

Figure 5 shows the C–V and 1/C^2–V characteristics of diode A and diode B at a frequency of 1 MHz. The net carrier concentration ($N_D - N_A$) of the GaN SBDs can be obtained using the following equations:[31]

$$1/C^2 = \frac{2}{q\varepsilon_0\varepsilon_r(N_D - N_A)}(V_{bi} - V - kT/q), \tag{3}$$

$$d(1/C^2)/dV = -\frac{2}{q\varepsilon_0\varepsilon_r(N_D - N_A)}, \tag{4}$$

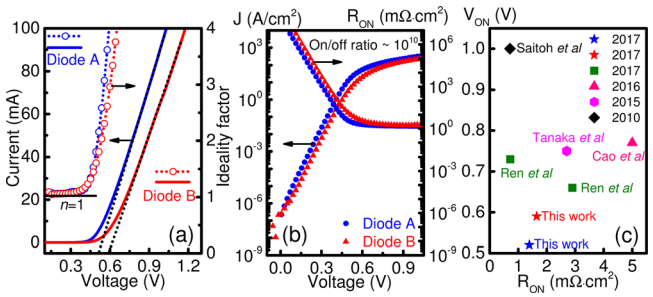


FIG. 4. (a) Forward current and ideality factor as a function of voltage on a linear scale. The V_{ON} values of diode A and diode B were also obtained by linear extrapolation. (b) Forward current density and on-resistance versus voltage on a semi-log scale. (c) Comparison of V_{ON} and R_{ON} of recently reported vertical GaN-on-GaN SBDs.[18,28–30]

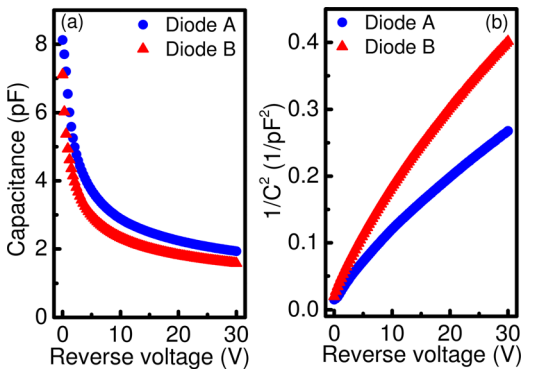


FIG. 5. (a) C–V and (b) 1/C^2–V characteristics of diode A and diode B at 1 MHz.

where ε_0 is the permittivity of the vacuum, ε_r is the relative permittivity of GaN, and V_{bi} is the built-in voltage. The net carrier concentrations of diode A and diode B are $6.9 \times 10^{15}\,\mathrm{cm}^{-3}$ and $4.6 \times 10^{15}\,\mathrm{cm}^{-3}$, respectively. With a nominal Si concentration of $2 \times 10^{16}\,\mathrm{cm}^{-3}$, a very low compensating acceptor concentration at the level of $10^{16}\,\mathrm{cm}^{-3}$ was determined.[32]

Figure 6(a) presents the reverse I–V characteristics of diode A and diode B. Diode A showed a V_{BD} of ~340 V, while diode B broke down at ~503 V, indicating that DDLs can enhance the breakdown capability of GaN SBDs. Since we did not employ FP or edge termination, the breakdown was expected to be determined by the device edge breakdown. Optical microscopy examination confirmed that the catastrophic damages of the GaN SBDs indeed occurred at the edge of Schottky contacts possibly due to severe edge electric field crowding. The measured breakdown voltages were therefore a bit lower than the theoretical values based on the intrinsic critical electric field of GaN. With the critical electric fields obtained using Eq. (6), the electric field profiles in diode A and diode B are plotted in Fig. 6(b) by one-dimensional Poisson's equation

$$\frac{dE}{dt} = \frac{q(N_D - N_A)}{\varepsilon_0 \varepsilon_r}, \tag{5}$$

where dE/dt is the slope of the electric field profile. Both devices were reverse biased at their V_{BD}. The breakdown voltage and the critical electric field of the punch-through planar junction are related by[33]

$$V_{BD} = E_c t_{DL} - \frac{q(N_D - N_A) t_{DL}^2}{2\varepsilon_0 \varepsilon_r}, \tag{6}$$

where E_c is the critical electric field and t_{DL} is the thickness of the drift layer. The E_c values were calculated to be 1.17 MV/cm and 1.30 MV/cm for diode A and diode B, respectively. The smaller breakdown voltage and critical electric field of diode A can be a result of larger net carrier concentration. These values are lower than previous reports (~3.0 MV/cm) due to the absence of FP and edge termination, insufficient mesa isolation, and large contact area. Table II summarizes the device performance metrics of diode A and diode B at RT.

Figures 7(a)–7(b) show the temperature-dependent forward I–V characteristics from 25 °C to 250 °C. The I–V–T curves were described using the thermionic emission model given by[21]

$$I = I_0 \exp(q(V - IR_s)/nkT - 1), \tag{7}$$

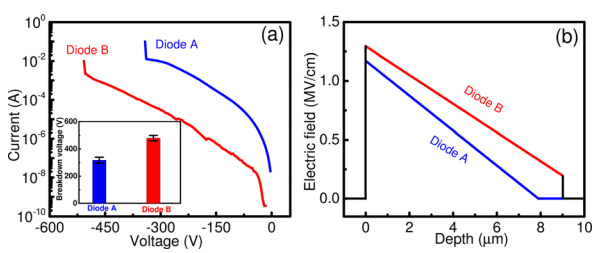


FIG. 6. (a) Reverse I–V characteristics of diode A and diode B. The inset shows the measured breakdown voltages of diode A and diode B. (b) Electric field profiles along the vertical direction of diode A and diode B.

TABLE II. Summary of device parameters for diode A and diode B.

Sample	N_D-N_A ($\times 10^{15}\,\mathrm{cm}^{-3}$)	n	Φ_B (eV)	Mobility [$\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$]	R_{ON} ($\mathrm{m}\Omega\cdot\mathrm{cm}^2$)	V_{ON} (V)	V_{BD} (V)
Diode A	6.9	1.06	0.69	886.1	1.39	0.52	340
Diode B	4.6	1.04	0.70	1045.2	1.65	0.59	503

$$I_0 = AA^*T^2 \exp(-\Phi_B/kT), \tag{8}$$

where I_0 is the saturation current, Φ_B is the barrier height, A is the contact area, A^* is the Richardson constant, and R_s is the series resistance. After plotting $\ln(I_0/T^2)$ vs $1/T$, the barrier height of Pt/GaN were extracted from the slopes as shown in Fig. 7(c). The Φ_B of diode A was 0.69 eV and that of diode B was 0.70 eV. Diode A has a slightly smaller barrier height due to the image force barrier lowering. The low Φ_B values are partly responsible for the obtained record-low V_{ON} in forward bias. The measured Φ_B values are less than the theoretical values, which demands further investigations. Possible explanations include surface roughness,[30] nonuniform current distribution,[21] and so on. In Fig. 7(d), n and R_{ON} were extracted as a function of temperature. n showed a very weak temperature dependence in the range of 1.02–1.09, indicating nearly ideal and highly homogeneous metal/semiconductor interface. However, R_{ON} clearly increased with increasing temperature. Recalling Eq. (2), R_{SBD} can be obtained at each temperature assuming constant R_{SUB} and negligible R_{CON}. R_{SBD} is determined by the free carrier concentration N and mobility μ of the drift layers by $R_{SBD} = t/q\mu N$. N was almost constant from 25 °C to 250 °C, which was confirmed by C–V measurements. Therefore, the temperature dependence of R_{SBD} is mainly determined by μ. μ(T) is predominately limited by the lattice scattering (i.e., phonons) over 100 K and can be characterized by the following power-law relation:[34,35]

$$\mu(T) = \mu_0 (T/T_0)^{\gamma}, \tag{9}$$

where μ_0 is the electron mobility at 300 K, T_0 is 300 K, and γ is the power index. In Fig. 8, good agreements between experimental data and Eq. (8) were obtained on both devices. These results

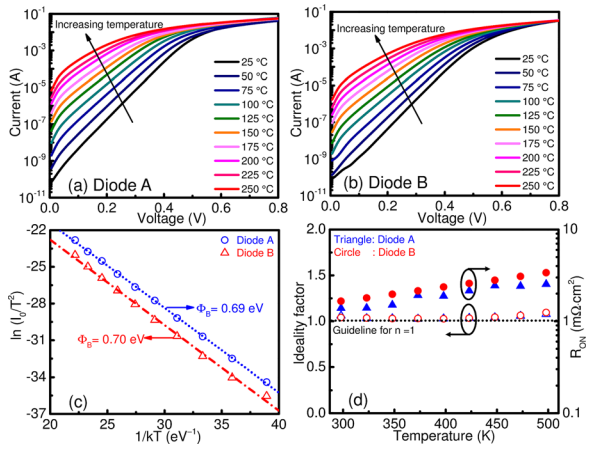


FIG. 7. The temperature-dependent forward I–V characteristics from 25 °C to 250 °C for (a) diode A and (b) diode B. (c) Richardson plot of the two diodes with the Schottky barrier height extracted. (d) Ideality factor and R_{ON} as a function of temperature for the two diodes.

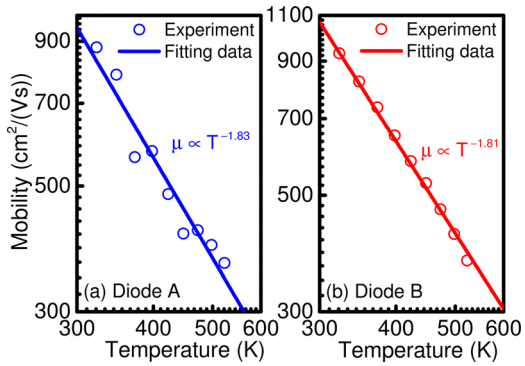


FIG. 8. Mobility as a function of temperature for (a) diode A and (b) diode B on a log-log scale. The mobility was fitted using the power law model.

confirmed that the increase in R_{ON} was caused by the decrease in phonon-limited electron mobility with temperature. γ was -1.83 for diode A and -1.81 for diode B, which is consistent with reported values in the range between -1.5 and -2.5.[34–36]

In summary, vertical GaN SBDs with DDLs were grown and fabricated on free standing GaN substrates, followed by comprehensive device analysis. The devices showed excellent forward characteristics with a record-low V_{ON}, small R_{ON}, near unity ideality factor, and high electron mobility. In addition, R_{ON} showed a positive temperature dependence that was determined by the phonon-limited electron mobility. At reverse bias, diode B showed enhanced breakdown capability due to DDL design. Devices with more complicated drift layer designs are expected to further increase the breakdown voltages and are currently under investigation. This work shows that vertical GaN SBDs with DDLs can have both desirable turn-on characteristics and breakdown capability for efficient high voltage high frequency power switching applications.

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