High Performance Vertical GaN-on-GaN p-n Power Diodes With Hydrogen-Plasma-Based Edge Termination

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***Abstract*—This letter reports the first implementation of a hydrogen-plasma-based edge termination technique (HPET) in vertical GaN p-n power diodes grown on bulk GaN substrates using metalorganic chemical vapor deposition. The device with a 9-μm-thick drift layer exhibited a high breakdown voltage (V_{bd}) of 1.57 kV, a low ON-resistance (R_{ON}) of 0.45 m$\Omega \cdot$ cm^2 (or 0.70 m$\Omega \cdot$ cm^2 with current spreading considered) and a high Baliga's figure-of-merit (V_{bd}^2/R_{ON}) of 5.5 GW/cm^2 (or 3.6 GW/cm^2) without passivation or field plate, which are close to the theoretical limit of GaN. This technique enabled a significant reduction in leakage current ($\sim 10^6$ times at -300 V) and a huge enhancement in V_{bd} (from $\sim$300 V to 1.57 kV). Furthermore, the device showed good forward characteristics with a turn-ON voltage of 3.5 V, an ON-current of $\sim$2 kA/cm^2 (or 1.3 kA/cm^2), an ON/OFF ratio of $\sim 10^9$, and an ideality factor of 1.4. This work shows the HPET can serve as an effective, low cost, and easy-to-implement edge termination technique for high voltage and high power GaN p-n power diodes.**

***Index Terms*—Gallium nitride, wide bandgap semiconductor, p-n diodes, power electronics, breakdown, edge termination.**

I. Introduction

WURTZITE GaN wide bandgap semiconductor (WBG) has attracted considerable attention for optoelectronics [1]–[4], photonics [5] and electronics [6], [7]. For power electronics, GaN based devices can outperform Si and SiC based devices due to their larger bandgap, higher critical electric field and larger Baliga's figure of merit (FOM) [7]. GaN transistors and diodes have already been demonstrated [6]–[8]. Conventional GaN power p-n diodes were grown on lattice-mismatched foreign substrates such as sapphire [9], [10] and Si [11]–[14] with high defect densities, which hindered the device epitaxial growth and performance. Recently, due to the availability of bulk GaN substrates, high performance vertical GaN p-n diodes have been homoepitaxially grown for high voltage and high power applications [15]–[25].

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To prevent the premature breakdown of GaN p-n diodes at the junction edge due to the electric field crowding effects [26], [27], edge termination techniques are indispensable for achieving high breakdown voltages (V_{bd}). Currently, ion-implantation based edge termination technique (IIET) is usually used to form the junction termination extension (JTE) for high voltage SiC devices [28]–[30]. However, energetic ion bombardments during the ion-implantation process induce tremendous damages and the devices need a high-temperature (>1500 °C) thermal activation and annealing process [29], [30] that often results in unwanted defects [31], [32]. Furthermore, the IIET is still difficult to effectively implement in GaN power devices due to material issues [27]. In this work, we propose a low-damage, low-temperature and easy-to-implement hydrogen-plasma based edge termination technique (HPET) to improve the V_{bd} of GaN p-n diodes. It has been well established that hydrogen (H) atoms can strongly bond with Mg acceptors in p-GaN to form Mg-H complexes [33], and effectively passivate p-GaN into highly resistive GaN (HR-GaN) even at high temperatures [34]–[36]. Hao *et al.* [36] have carried out a comprehensive reliability study for the hydrogen-plasma based technique in GaN devices. This process can be easily realized by inductively coupled plasma (ICP) tools that can be almost ubiquitously found in nanofabrication centers. Therefore, the HPET can considerably reduce costs and simplify processes of the device fabrication for high performance GaN p-n diodes.

II. Growth and Device Fabrication

The device epilayers were grown by conventional metalorganic chemical vapor deposition (MOCVD) on n-type bulk GaN substrates from Sumitomo. Trimethylgallium (TMGa) is the precursor for Ga and ammonia (NH_3) is the source for N. Bis(cyclopentadienyl)magnesium (Cp_2Mg) and silane (SiH_4) are used as the precursors for Mg acceptors and Si donors, respectively. The carrier gas is H_2. As shown in Fig. 1(a), the GaN p-n diode consists of a 1 μm n$^+$-GaN buffer layer ([Si] $= 2 \times 10^{18}$ cm^{-3}), a 9-μm-thick unintentionally doped (UID) drift layer, a 500 nm p-GaN ([Mg] $= 10^{19}$ cm^{-3}), and a 20 nm heavily doped p$^+$-GaN contact layer ([Mg] $= 10^{20}$ cm^{-3}). The crystal quality of the GaN epilayers was characterized by high resolution X-ray diffraction (HRXRD). Figure 2(a) represents the (002) symmetric and the (102) asymmetric plane rocking curves (RCs) of the epilayers. The full width at half maximum (FWHM) of the RCs are 62.3 and 37.8 arc sec for the (002) plane and the (102) plane,

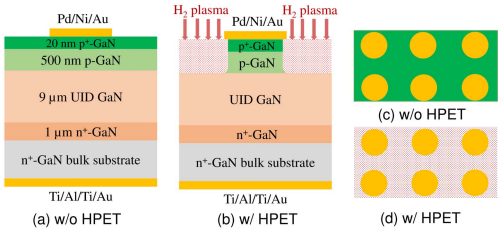

Fig. 1. Schematic cross-section and plane view of GaN-on-GaN p-n diodes (a), (c) without (w/o) HPET and (b), (d) with (w/) HPET.

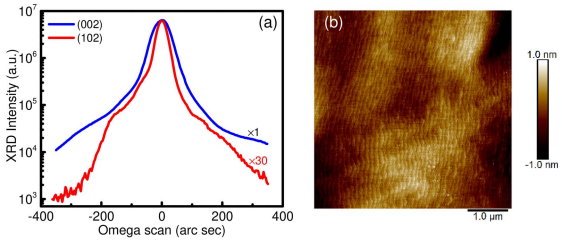

Fig. 2. (a) Rocking curves of the (002) plane and the (102) plane of GaN epilayers. (b) The AFM image of the epilayers.

respectively. Using the method described in [25], the dislocation density of the epilayers is estimated to be 4.2×10^6 cm^{-2}, much lower than that of typical GaN-on-sapphire devices ($>10^9$ cm^{-2}). The surface morphology of the epilayers was also examined by atomic force microscopy (AFM) in Fig. 2(b). The root-mean-square (RMS) roughness of a 5×5 μm^2 scanning area of the epilayers is 0.33 nm. These results indicate the homoepitaxial GaN growth on bulk GaN substrates produced low-defect-density and smooth epilayers.

The GaN p-n diodes were fabricated using the conventional photolithography. The samples were cleaned in acetone and isopropyl alcohol under ultrasonic, and then dipped briefly in hydrochloric acid before metal depositions. The circular p-contacts with a diameter of 80 μm were formed by Pd/Ni/Au metal stacks, which were deposited by electron beam evaporation and subsequently annealed using rapid thermal annealing (RTA). The non-alloyed Ti/Al/Ti/Au metal stacks formed the n-contacts at the backside of the bulk GaN substrates using electron beam evaporation. Then, the devices were treated by H_2 plasma using ICP at an ICP power of 300 W, an RF power of 10 W, and a pressure of 8 mTorr. Finally, the devices [Fig. 1(b)] were thermally annealed using RTA at 400 °C to recover potential plasma damages and fully passivate the p-GaN layer [36]. Please be noted that the rectangular treated regions are only for illustrative purposes, and they don't necessarily have sharp corners [26], [27] due to the thermal diffusion of H atoms by the RTA treatment [36]. Figure 3 showed there were large currents between the two ohmic contacts before the H_2 plasma treatment and no currents after the H_2 plasma treatment. The former is due to the existence of a complete current conduction path, while the latter is due to the complete cutoff of this path. This evidence indicates that the H_2 plasma treatment can reach over the 520 nm p-type GaN layer and effectively passivate all the p-GaN into HR-GaN that serves as the edge termination for the devices. The effects of ICP and RTA conditions on the device characteristics demand further investigations. And future device simulation studies by Silvaco ATLAS will take the shape and resistivity of the HR-GaN edge termination into consideration. No mesa etching or passivation or field

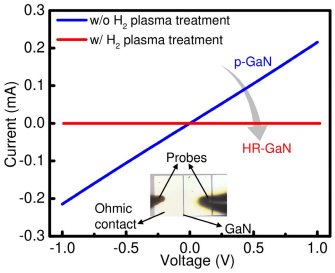

Fig. 3. I-V curves of two ohmic contacts w/o and w/ the H_2 plasma treatment.

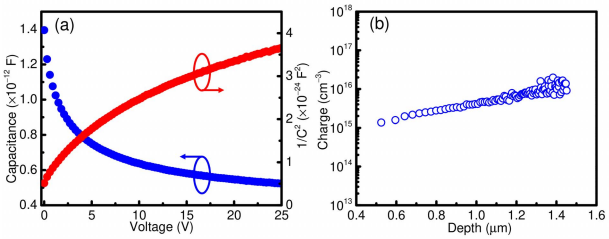

Fig. 4. (a) C and $1/C^2$ versus V for the device drift layer. (b) The extracted carrier concentration profile in the device drift layer.

plates (FP) were incorporated. For reference, the GaN p-n diodes without H_2 plasma treatment was also fabricated by the same processes and examined [26], [27]. The forward current–voltage (I–V) curves were characterized by Keithley 2410 sourcemeter. The capacitance–voltage (C–V) characteristics were measured using Keithley 4200-SCS parameter analyzer. The reverse breakdown measurements were conducted in non-conductive Fluorinert liquid using both Keithley 2410 and Tektronix 370A curve tracer.

III. Results and Discussions

Figure 4 shows capacitance (C)–V and $1/C^2$–V characteristics of the device drift layer at a frequency of 1 MHz. The net carrier concentration N_D can be extracted using [20], [37]

$$N_D = -\frac{2}{q\varepsilon_0\varepsilon_r d(1/C^2)/dV} \tag{1}$$

where q is the electron charge, ε_0 is the permittivity of the vacuum, and ε_r is the relative permittivity of GaN. The carrier concentrations of the UID GaN drift layer is $\sim 6.7 \times 10^{15}$ cm^{-3}, which is determined by the background of the MOCVD reactor.

Figure 5(a) presents the forward I–V characteristics of the GaN p-n diodes. The devices w/ and w/o the HPET showed comparable I-V curves at forward bias, indicating that the H_2 plasma treatment doesn't degrade forward I-V characteristics of the diodes, which was also observed in other edge termination techniques [26], [27]. The device with the HPET had a turn-on voltage (V_{on}) of $\sim$3.5 V. In addition, strong light emission was observed at bias beyond V_{on}. This originates from the electron-hole radiative recombination in the p-n diodes and is often seen as an indicator of high material quality of the devices. Electroluminescence (EL) measurements showed the presence of three peaks at 2.2 eV (deep-level transition), 3.2 eV (conduction band to acceptor-level transition) and 3.4 eV (band-edge emission) [38]. In Fig. 5(b), the GaN p-n diodes with the HPET exhibited good rectifying behaviors with a high on-current of $\sim$2 kA/cm^2, a high ON/OFF ratio

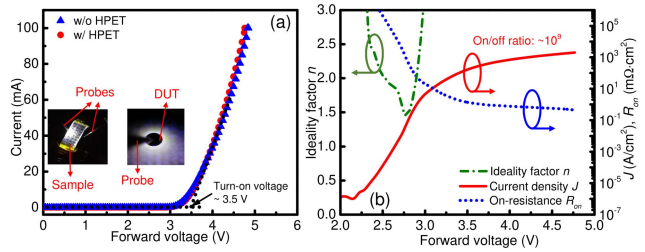

Fig. 5. (a) Forward *I–V* characteristics of GaN p-n diodes w/o and w/ the HEPT. The inset shows the illuminated sample at a high bias and an individual device under test (DUT). (b) The current density, R_{on}, and ideality factor as a function of forward voltage for the device w/ the HPET.

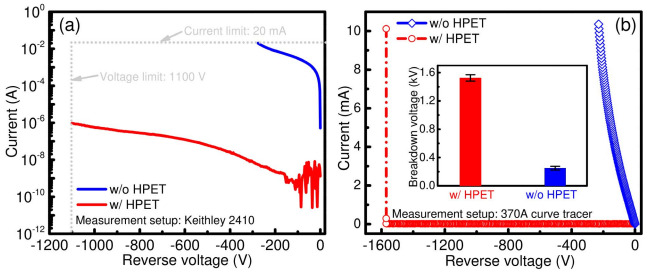

Fig. 6. Reverse *I–V* characteristics of GaN p-n diodes w/o and w/ the HPET measured using (a) Keithley 2410 and (b) Tektronix 370A curve tracer.

$\sim 10^9$ and a low on-resistance (R_{on}) of 0.45 m$\Omega \cdot$ cm^2. In this calculation, the active area is the area of the anode electrode. Taking into account a current spreading of ~ 10 μm from the anode [20], the on-current is calculated to be 1.3 kA/cm^2 and R_{on} 0.70 m$\Omega \cdot$ cm^2. At the voltage of 2.7 V, the ideality factor n reaches a minimum of 1.4. The decrease of the n before 2.7 V is due to the transition from the Shockley-Read-Hall (SRH) recombination current to the diode diffusion current. The n increases with voltage after 2.7 V because of the series resistance effects [20].

Figure 6 shows the reverse I–V characteristics of the GaN p-n diodes. Two sets of measurement setups were used: (i) Keithley 2410 with a voltage limit of 1.1 kV and (ii) Tektronix 370A curve tracer with a voltage limit of 2.0 kV. The former has a low voltage limit but a high current resolution, while the latter has a high voltage limit but a low current resolution. Keithley 2410 is mainly used to measure the leakage currents and 370A curve tracer mainly to conduct the breakdown measurements of the devices. The measurements were conducted on $\sim$25 devices on each sample, $\sim$50 devices in total. The device with the HPET showed a $\sim 10^6$ times smaller leakage current at -300 V than the device without the HPET. This is likely attributed to two mechanisms: (1) The HPET confines the majority of the currents under the device active region and avoids possible leakage pathways; (2) The HPET can help suppress the peak electric fields at the junction edge and thus reduce the leakage currents. The V_{bd} of the devices was significantly enhanced from $\sim$300 V to 1570 V (hard breakdown with catastrophic damages of the contacts) due to the incorporation of the HPET. In addition, avalanche breakdown, i.e., a positive temperature coefficient of V_{bd}, has been well observed in previous reports [20], [23], which is also a topic of undergoing research for the devices w/ the HPET. The critical electric field can be estimated using [20]

$$V_{bd} = E_c t - \frac{q N_D t^2}{2\varepsilon_0 \varepsilon_r} \tag{2}$$

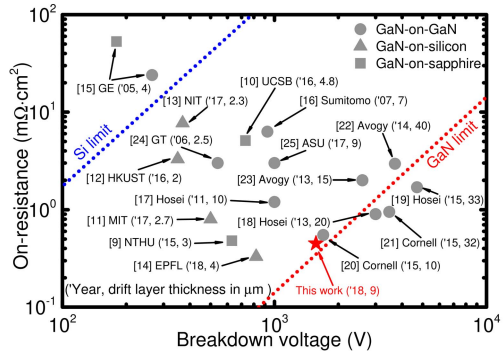

Fig. 7. Benchmark plot of on-resistance versus breakdown voltage for reported vertical GaN diodes and this work. In the parenthesis are the publication year and the drift layer thickness of the devices in μm.

where E_c is the critical electric field and t is thickness of the drift layer. The E_c of the device with the HPET was calculated to be $\sim$3.0 MV/cm, which is among the best reported values for GaN p-n diodes [7], [11], [13], [20], [22], [23], [38]. These results indicate the HPET is highly effective in improving the breakdown capability of GaN p-n power diodes.

To benchmark the device performance, R_{on} and V_{bd} of reported vertical GaN p-n diodes are compared in Fig. 7. With a V_{bd} of 1.57 kV and a R_{on} of 0.45 m$\Omega \cdot$ cm^2 (or 0.70 m$\Omega \cdot$ cm^2), the GaN p-n diode with the HPET in this work has a Baliga's FOM (V_{bd}^2/R_{on}) of 5.5 GW/cm^2 (or 3.6 GW/cm^2), which is very close to the theoretical limit line of GaN. The V_{bd} of our GaN p-n diode is comparable to or higher than other reports with similar drift layer thicknesses [16], [17], [20], [25]. The R_{on} of this work is among the lowest reported values for over 1 kV devices. Considering the low-cost, low-damage and simplified fabrication processes, this demonstrates the potential of the HPET for high performance GaN p-n diodes.

IV. Conclusion

We implemented the HPET on the vertical GaN p-n diodes grown on bulk GaN substrates. At forward bias, the device exhibited excellent rectifying behaviors with an on/off ratio of $\sim 10^9$ and a R_{on} of 0.45 m$\Omega \cdot$ cm^2 (or 0.70 m$\Omega \cdot$ cm^2). At reverse bias, the HPET considerably increased the breakdown voltage of the devices from $\sim$300 V to 1.57 kV. These results indicate the HPET can provide a low-cost, low-damage and easy-to-implement edge termination technique for high performance GaN p-n diodes. And a follow-up work on the dynamic characteristics and reliability issues of the HPET is underdoing.

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References

[1] Y. Zhao, H. Fu, G. T. Wang, and S. Nakamura, "Toward ultimate efficiency: Progress and prospects on planar and 3D nanostructured nonpolar and semipolar InGaN light-emitting diodes," *Adv. Opt. Photon.*, vol. 10, no. 1, pp. 246–308, Feb. 2018, doi: 10.1364/AOP.10.000246.

[2] X. Huang, H. Fu, H. Chen, X. Zhang, Z. Lu, J. Montes, M. Iza, S. P. DenBaars, S. Nakamura, and Y. Zhao, "Nonpolar and semipolar InGaN/GaN multiple-quantum-well solar cells with improved carrier collection efficiency," *Appl. Phys. Lett.*, vol. 110, no. 16, p. 161105, Apr. 2017, doi: 10.1063/1.4980139.

[3] H. Fu, Z. Lu, X. Zhao, Y. Zhang, S. P. DenBaars, S. Nakamura, and Y. Zhao, "Study of low efficiency droop in semipolar (20-2-1) InGaN light-emitting diodes by time-resolved photoluminescence," *J. Display Technol.*, vol. 12, no. 7, pp. 736–741, Jul. 2016, doi: 10.1109/JDT.2016.2521618.

[4] H. Fu, Z. Lu, X. Huang, H. Chen, and Y. Zhao, "Crystal orientation dependent intersubband transition in semipolar AlGaN/GaN single quantum well for optoelectronic applications," *J. Appl. Phys.*, vol. 119, no. 17, p. 174502, May 2016, doi: 10.1063/1.4948667.

[5] H. Chen, X. Huang, H. Fu, Z. Lu, X. Zhang, J. A. Montes, and Y. Zhao, "Characterizations of nonlinear optical properties on GaN crystals in polar, nonpolar, and semipolar orientations," *Appl. Phys. Lett.*, vol. 110, no. 18, p. 181110, May 2017, doi: 10.1063/1.4983026.

[6] Y.-F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 586–590, Mar. 2001, doi: 10.1109/16.906455.

[7] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical power p-n diodes based on bulk GaN," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 414–422, Feb. 2015, doi: 10.1109/TED.2014.2360861.

[8] H. Fu, X. Huang, H. Chen, Z. Lu, I. Baranowski, and Y. Zhao, "Ultra-low turn-on voltage and on-resistance vertical GaN-on-GaN Schottky power diodes with high mobility double drift layers," *Appl. Phys. Lett.*, vol. 111, no. 15, p. 152102, Oct. 2017, doi: 10.1063/1.4993201.

[9] B. S. Zheng, P. Y. Chen, C. J. Yu, Y. F. Chang, C. L. Ho, M. C. Wu, and K. C. Hsieh, "Suppression of current leakage along mesa surfaces in GaN-based p-i-n diodes," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 932–934, Sep. 2015, doi: 10.1109/LED.2015.2458899.

[10] C. Gupta, Y. Enatsu, G. Gupta, S. Keller, and U. K. Mishra, "High breakdown voltage p–n diodes on GaN on sapphire by MOCVD," *Phys. Status Solidi A*, vol. 213, no. 4, pp. 878–882, Apr. 2016, doi: 10.1002/pssa.201532554.

[11] Y. Zhang, D. Piedra, M. Sun, J. Hennig, A. Dadgar, L. Yu, and T. Palacios, "High-performance 500 V quasi- and fully-vertical GaN-on-Si pn diodes," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 248–251, Feb. 2017, doi: 10.1109/LED.2016.2646669.

[12] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, "Fully vertical GaN p-i-n diodes using GaN-on-Si epilayers," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 636–639, May 2016, doi: 10.1109/LED.2016.2548488.

[13] S. Mase, T. Hamada, J. J. Freedsman, and T. Egawa, "Effect of drift layer on the breakdown voltage of fully-vertical GaN-on-Si p-n diodes," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1720–1723, Dec. 2017, doi: 10.1109/LED.2017.2765340.

[14] R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820 V GaN-on-Si quasi-vertical PiN diodes with BFOM of 2.0 GW/cm^2," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018, doi: 10.1109/LED.2018.2793669.

[15] X. A. Cao, H. Lu, S. F. LeBoeuf, C. Cowen, S. D. Arthur, and W. Wang, "Growth and characterization of GaN PiN rectifiers on free-standing GaN," *Appl. Phys. Lett.*, vol. 87, no. 5, pp. 053503-1–053503-3, Aug. 2005, doi: 10.1063/1.2001738.

[16] Y. Yoshizumi, S. Hashimoto, T. Tanabe, and M. Kiyama, "High-breakdown-voltage pn-junction diodes on GaN substrates," *J. Cryst. Growth*, vol. 298, pp. 875–878, Jan. 2007, doi: 10.1016/j.jcrysgro.2006.10.246.

[17] K. Nomoto, Y. Hatakeyama, H. Katayose, N. Kaneda, T. Mishima, and T. Nakamura, "Over 1.0 kV GaN $p-n$ junction diodes on free-standing GaN substrates," *Phys. Status Solidi A*, vol. 208, no. 7, pp. 1535–1537, Jul. 2011, doi: 10.1002/pssa.201000976.

[18] Y. Hatakeyama, K. Nomoto, A. Terano, N. Kaneda, T. Tsuchiya, T. Mishima, and T. Nakamura, "High-breakdown-voltage and low-specific-on-resistance GaN p-n junction diodes on free-standing GaN substrates fabricated through low-damage field-plate process," *Jpn. J. Appl. Phys.*, vol. 52, pp. 028007-1–028007-3, Jan. 2013, doi: 10.7567/JJAP.52.028007.

[19] H. Ohta, N. Kaneda, F. Horikiri, Y. Narita, T. Yoshida, T. Mishima, and T. Nakamura, "Vertical GaN p-n Junction diodes with high breakdown voltages over 4 kV," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1180–1182, Nov. 2015, doi: 10.1109/LED.2015.2478907.

[20] K. Nomoto, B. Song, Z. Hu, M. Zhu, M. Qi, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "1.7-kV and 0.55-m$\Omega\cdot$cm^2 GaN p-n diodes on bulk GaN substrates with avalanche capability," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161–164, Feb. 2016, doi: 10.1109/LED.2015.2506638.

[21] K. Nomoto, Z. Hu, B. Song, M. Zhu, M. Qi, R. Yan, V. Protasenko, E. Imhoff, J. Kuo, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩcm^2: A record high figure-of-merit of 12.8 GW/cm^2," in *IEDM Tech. Dig.*, Dec. 2015, pp. 971–974, doi: 10.1109/IEDM.2015.7409665.

[22] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV vertical GaN PN diodes," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 247–249, Feb. 2014, doi: 10.1109/LED.2013.2294175.

[23] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Disney, and D. Bour, "High voltage vertical GaN p-n diodes with avalanche capability," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3067–3070, Oct. 2013, doi: 10.1109/TED.2013.2266664.

[24] J. B. Limb, D. Yoo, J.-H. Ryou, W. Lee, S. C. Shen, and R. D. Dupuis, "High performance GaN pin rectifiers grown on free-standing GaN substrates," *Electron. Lett.*, vol. 42, no. 22, pp. 1313–1314, Oct. 2006, doi: 10.1049/el:20062261.

[25] H. Fu, X. Huang, H. Chen, Z. Lu, X. Zhang, and Y. Zhao, "Effect of buffer layer design on vertical GaN-on-GaN p-n and Schottky power diodes," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 763–766, Jun. 2017, doi: 10.1109/LED.2017.2690974.

[26] A. M. Ozbek and B. J. Baliga, "Planar nearly ideal edge-termination technique for GaN devices," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 300–302, Mar. 2011, doi: 10.1109/LED.2010.2095825.

[27] S. Han, S. Yang, and K. Sheng, "High-voltage and high-I_{ON}/I_{OFF} vertical GaN-on-GaN Schottky varrier diode with nitridation-based termination," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 572–575, Apr. 2018, doi: 10.1109/LED.2018.2808684.

[28] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer-Verlag, 2008, ch. 3, pp. 91–155.

[29] W. Sung, E. V. Brunt, B. J. Baliga, and A. Q. Huang, "A new edge termination technique for high-voltage devices in 4H-SiC–multiple-floating-zone junction termination extension," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 880–882, Jul. 2011, doi: 10.1109/LED.2011.2144561.

[30] A. V. Bolotnikov, P. G. Muzykov, Q. Zhang, A. K. Agarwal, and T. S. Sudarshan, "Junction termination extension implementing drive-in diffusion of boron for high-voltage SiC devices," *IEEE Trans. Electron Devices*, vol. 57, no. 8, pp. 1930–1935, Jul. 2010, doi: 10.1109/TED.2010.2051246.

[31] R. Ghandi, B. Buono, M. Domeij, C.-M. Zetterling, and M. Östling, "High-voltage (2.8 kV) implantation-free 4H-SiC BJTs with long-term stability of the current gain," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2665–2669, Jun. 2011, doi: 10.1109/TED.2011.2154332.

[32] A. Salemi, H. Elahipanah, K. Jacobs, C.-M. Zetterling, and M. Östling, "15 kV-Class implantation-free 4H-SiC BJTs with record high current gain," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 63–66, Jan. 2018, doi: 10.1109/LED.2017.2774139.

[33] S. Nakamura, N. Iwasa, M. Senoh, and T. Mukai, "Hole compensation mechanism of P-type GaN films," *Jpn. J. Appl. Phys.*, vol. 31, no. 5A, pp. 1258–1266, May 1992, doi: 10.1143/JJAP.31.1258.

[34] R. Hao, K. Fu, G. Yu, W. Li, J. Yuan, L. Song, Z. Zhang, S. Sun, X. Li, Y. Cai, X. Zhang, and B. Zhang, "Normally-off p-GaN/AlGaN/GaN high electron mobility transistors using hydrogen plasma treatment," *Appl. Phys. Lett.*, vol. 109, p. 152106, Oct. 2016, doi: 10.1063/1.4964518.

[35] R. Hao, W. Li, K. Fu, G. Yu, L. Song, J. Yuan, J. Li, X. Deng, X. Zhang, Q. Zhou, Y. Fan, W. Shi, Y. Cai, X. Zhang, and B. Zhang, "Breakdown enhancement and current collapse suppression by high-resistivity GaN cap layer in normally-off AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1567–1570, Nov. 2017, doi: 10.1109/LED.2017.2749678.

[36] R. Hao, N. Xu, G. Yu, L. Song, F. Chen, J. Zhao, X. Deng, X. Li, K. Cheng, K. Fu, Y. Cai, X. Zhang, and B. Zhang, "Studies on fabrication and reliability of GaN high-resistivity-cap-layer HEMT," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1314–1320, Apr. 2018, doi: 10.1109/TED.2018.2803521.

[37] H. Fu, I. Baranowski, X. Huang, H. Chen, Z. Lu, J. Montes, X. Zhang, and Y. Zhao, "Demonstration of AlN Schottky barrier diodes with blocking voltage over 1 kV," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1286–1289, Sep. 2017, doi: 10.1109/LED.2017.2723603.

[38] M. Qi, K. Nomoto, M. Zhu, Z. Hu, Y. Zhao, V. Protasenko, B. Song, X. Yan, G. Li, J. Verma, S. Bader, P. Fay, H. G. Xing, and D. Jena, "High breakdown single-crystal GaN p-n diodes by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 107, pp. 232101-1–232101-4, Dec. 2015, doi: 10.1063/1.4936891.