Nanopatterning

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Atomically Resolved Charge Redistribution for Ga Nanocluster Arrays on the Si(111)-7 × 7 Surface**

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In recent years, nanocrystals with size-dependent structural, electronic, and chemical properties have attracted increasing interest for fundamental studies and applied technology. Nanoscaled structures have unique properties that often differ from bulk materials, and a well-ordered array of such nanocrystals is expected to show additional phenomena arising from the periodic arrangement. Nanocrystals, whether isolated or arranged in arrays, are attractive for a wide range of applications[1,2] such as catalysis,[3–6] electronic devices,[7–10] and magnetic devices and storage.[11–14] Hence, the recent discovery of materials that self-assemble into ordered arrays of identical nanoclusters on the Si(111)-7 × 7 surface is an enabling development.[15–28] The Si(111)-7 × 7 surface is particularly noteworthy for nanoelectronics, molecular electronics, and chemical sensing because of its rich electronic and chemical structure. For example, recent scanning tunneling microscopy (STM) studies of covalently bound organic molecules on the Si(111)-7 × 7 surface have revealed delocalized charge transfer that modulates the local electronic properties at the atomic scale.[29,30] It is thus reasonable to expect comparable charge rearrangement and electronic property modulation from self-assembled nanocrystals on this surface.

The formation of uniform nanocluster arrays on the Si(111)-7 × 7 surface[24] has been demonstrated for a wide variety of materials, including In,[15,16] Ga,[15,16,19] Al,[15–18,20,21] Tl,[28] Na,[23] Co,[26,27] Cu,[25] and Pb.[22] These nanoclusters have many intriguing features in common: uniform atomic structure; high thermal stability; formation via carefully controlled deposition and annealing conditions; and self-assembly into well-ordered, large-area arrays. In particular, the nanoclusters formed by the group-III metals (i.e., In, Ga, and Al) have a common atomic structure consisting of six metal atoms bonded to Si surface atoms.

The Ga nanocluster system was chosen for this work because many of its structural and thermodynamic properties have been studied in previous investigations[15,16,19,31–34] but its electronic properties are not yet well understood. This system is also attractive for its ease of preparation: the Ga is simply deposited onto the Si surface at room temperature, and annealing the substrate at 300 °C readily forms arrays of uniform nanoclusters. This low-temperature preparation procedure suggests compatibility and possible integration with conventional microelectronic devices, where low thermal budgets during device fabrication are increasingly important.

Previous experimental studies on the electronic properties of metal nanoclusters on the Si(111)-7 × 7 surface have focused on individual nanoclusters as opposed to the delocalized properties of the two-dimensional array as a whole. For example, STM imaging has been performed at variable applied biases for Co[28] and Ga,[35] and scanning tunneling spectroscopy (STS) data have been gathered in the form of current–voltage curves (I vs. V) and differential tunneling conductance curves (dI/dV vs. V) measured at fixed locations on the sample surface for In[15,16,35] and Co.[27] A preliminary study using current imaging tunneling spectroscopy (CITS) to map the surface local density of states (LDOS) for Al nanoclusters has also been reported,[37] but the results are only shown for a single unit cell. On the other hand, a computational study of Al and In nanocluster arrays has predicted charge redistribution that leads to a spatially modulated two-dimensional electron gas (2DEG) over the surface as well as a reduction in the number of states near the Fermi level caused by the saturation of dangling bonds.[37] However, experimental verification of this two-dimensional charge redistribution has not yet been reported. Furthermore, spatially resolved studies of the delocalized electronic properties of metal nanocluster arrays on silicon have not been conducted.

In this Communication, we report the experimental observation of atomically resolved, delocalized two-dimensional charge redistribution associated with Ga nanocluster arrays on the Si(111)-7 × 7 surface. Using ultrahigh vacuum (UHV) scanning tunneling microscopy and differential tunneling conductance mapping, we correlate the topography of the Ga nanocluster array with its LDOS and demonstrate the presence of surface charge redistribution that results in distinct regions of increased differential tunneling conductance that connect adjacent Ga nanoclusters in the array.

The experimental data presented here consist of topographic STM images and spatial maps of the differential tunneling conductance (dI/dV), which is a measure of the LDOS of the surface.[38,39] To verify that our experimental procedure yields accurate differential tunneling conductance maps (see Experimental Section for details), the clean Si(111)-7 × 7 surface was imaged in both topography and dI/dV modes for sample biases ranging from −2.5 to +2.5 V. When compared with dI/dV and CITS images of Si(111)-7 × 7 reported in the literature,[40–42] our images reveal surface states for dangling bonds and Si–Si back bonds that occur at the expected energies. For example, two representative images are shown in Figure 1b at sample biases of −2.0 and +2.0 V. These images show regions of increased differential tunneling conductance attributed to Si–Si back-bond states.[40] The schematic diagram in Figure 1a shows the structure of the

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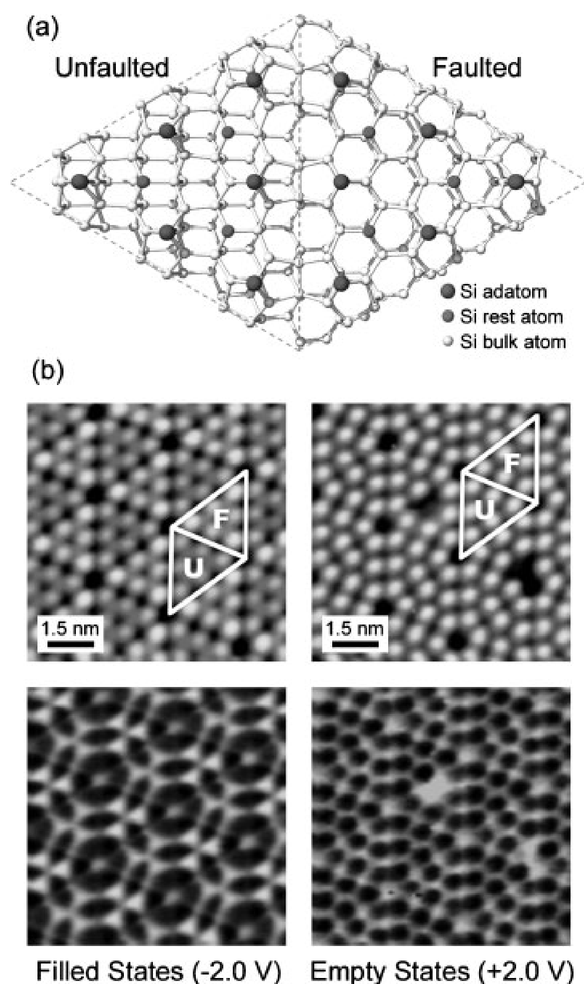

Figure 1. a) Schematic illustration of the Si(111)-7 $\times$ 7 unit cell, with unfaulted and faulted halves indicated. The Si adatom and rest atom dangling bonds are shown as dark gray spheres. b) Topographic STM images (top row) and d*I*/d*V* differential tunneling conductance maps (bottom row) of the clean Si(111)-7 $\times$ 7 surface. The left column shows filled states imaging (sample bias = −2.0 V), and the right column shows empty states imaging (sample bias = +2.0 V). The tunneling current setpoint is 0.5 nA.

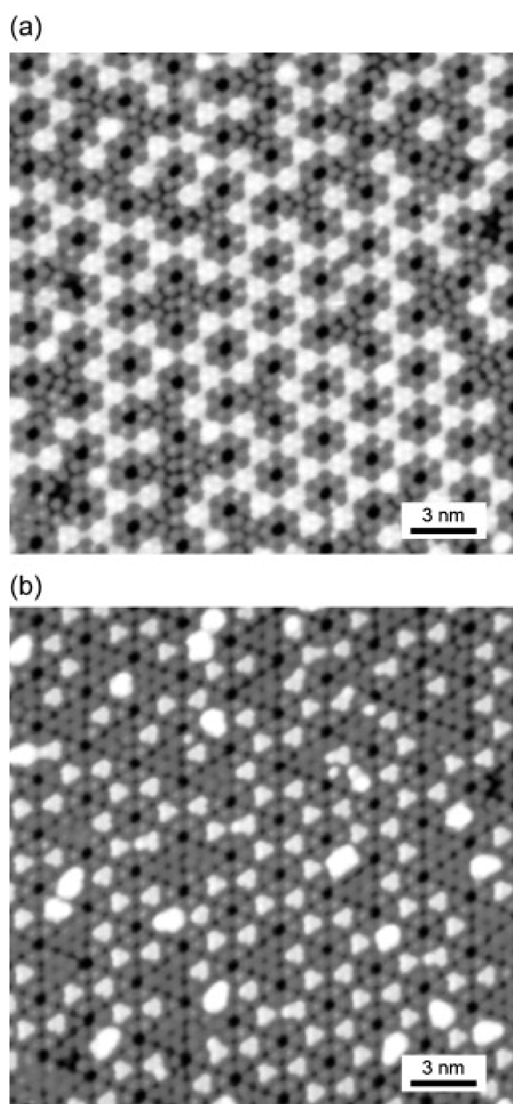

Figure 2. Large-area STM topographic images of the Ga nanocluster arrays in a) empty states (sample bias = +2.0 V) and b) filled states (sample bias = −2.0 V). Tunneling current setpoint is 0.1 nA.

Si(111)-7 $\times$ 7 reconstructed surface, which follows the dimer-adatom-stacking (DAS) model of Takayanagi et al.[43,44] One half of the unit cell contains a stacking fault, and has a higher density of states than the unfaulted half. There are 19 dangling bonds per unit cell: 12 adatom dangling bonds located in the top atomic layer of the reconstruction, 6 rest atom dangling bonds in the next layer, and one corner hole dangling bond.

An array of identical Ga nanoclusters was formed by Ga evaporation onto the Si(111)-7 $\times$ 7 surface followed by annealing of the substrate (see Experimental Section for details). Figure 2 shows both filled and empty states STM topography images of the array. An incomplete Ga nanocluster array was intentionally formed to allow the boundaries of the array to be studied and to allow comparisons with the clean Si(111)-7 $\times$ 7 surface. The atomic structure of the Ga nanoclusters has been verified using STM topography scans, computations of simulated STM images and total energies,[15,16] dynamical low-energy electron diffraction (LEED),[32] and reflection high-energy electron diffraction (RHEED) rocking curve analysis,[34] and is shown in the schematic in Figure 3 along with high-resolution STM images of the nanoclusters in filled and empty states. Within each nanocluster, which is confined to one half of the unit cell, six Ga atoms are bound to the three center Si adatoms in a ring-like structure. The Ga atoms are also each bound to two other Si atoms. The corner Si adatoms are not involved in nanocluster formation. In the high-resolution STM images in Figure 3b, the six bright protrusions in the empty-states image correspond to Ga atoms, while the three bright protrusions in the filled-states image correspond to the Si atoms. These atoms are circled on one half of the unit cell as a guide to the eye.

High-resolution images of the topography and differential tunneling conductance were simultaneously obtained for a 10 nm $\times$ 10 nm area of the Ga nanocluster array surface for a

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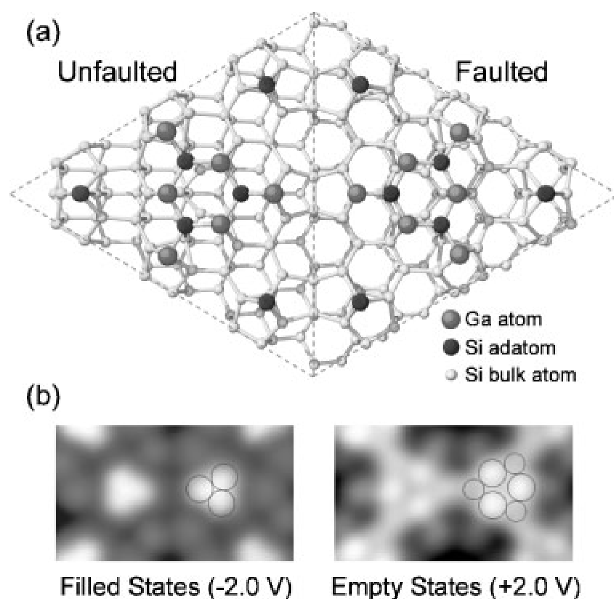

Figure 3. a) Schematic illustration of Ga nanoclusters bound to the Si(111)-7 $\times$ 7 substrate. The light gray spheres represent Ga atoms, while the dark gray spheres represent Si adatom dangling bonds. b) High-resolution topographic STM images of two Ga nanoclusters in filled states, left, and empty states, right. In both STM images, the tunneling current setpoint is 0.1 nA, the scan sizes are approximately 4 nm $\times$ 2 nm, and circles have been drawn on one half of the unit cell to aid the eye. The circles indicate Si and Ga atoms in filled states and empty states, respectively.

wide range of negative and positive sample-bias voltages. The forthcoming discussion will focus on a series of images for sample biases ranging from +0.75 to +1.5 V, shown in Figure 4, in order to highlight a two-dimensional interconnected network of increased LDOS, which is most readily visible in this voltage range. A small region of clean Si(111)-7 $\times$ 7 in the image shows that the topography and dI/dV images are accurate and allows the topography and dI/dV maps of the nanoclusters to be compared to those of the clean substrate. Observations from the topographic images, which are shown in the first row of images in Figure 4, will be discussed first, followed by analysis of the dI/dV maps, which are shown in the second row.

The topographic images contain some noteworthy features that hint at more complex electronic properties. At the lower positive bias values, the Ga atoms (light gray arrows) appear smaller than surrounding Si atoms (dark gray arrows); however, as the bias increases, the Ga atoms appear larger and brighter than the Si atoms. This change in apparent relative size and height with sample bias suggests an electronic effect since the actual topography is unchanged. A difference in brightness between the nanoclusters on the faulted and unfaulted halves of the Si unit cell is also observed. Since the atomic structure of the nanoclusters on the two halves is identical, the difference in brightness must arise from an electronic difference between the two halves of the substrate. These observations indicate that the electronic properties of the nanoclusters should be studied in more detail.

To characterize the electronic properties of the nanocluster array, differential conductance mapping was used to deconvolve the electronic and topographic components of the tunneling current. The dI/dV maps in the lower row of Figure 4 clearly show a delocalized two-dimensional network of increased LDOS wherever the nanoclusters are present, forming a continuous swath that connects adjacent nanoclusters. This network appears to be similar in nature to the 2DEG predicted by computational simulations for Al and In nanoclusters.[37] Interestingly, the network abruptly disappears at the boundary of the clean Si(111)-7 $\times$ 7 unit cells that do not contain nanoclusters. In other words, the LDOS is enhanced for the

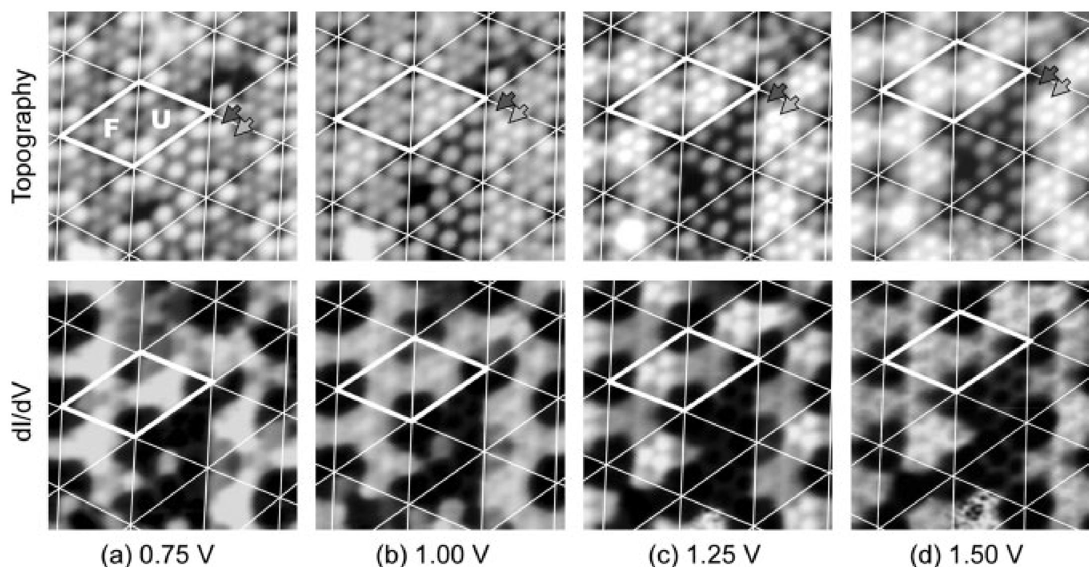

Figure 4. Simultaneous topography (top row) and dI/dV maps (bottom row) of the Ga nanocluster array. Images are all 10 nm $\times$ 10 nm. Each column shows data measured at a different sample bias: a) 0.75, b) 1.00, c) 1.25, and d) 1.50 V. Tunneling current setpoint is 0.5 nA. The same unit cell is outlined in each image. The dark gray arrow in each STM topography image indicates a representative Si atom, while the light gray arrow indicates a Ga atom.

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Ga nanocluster array compared to the LDOS of clean Si(111)-7×7, as seen directly in the dI/dV maps of Figure 4. The contribution to the LDOS from the electronic structure of the underlying Si substrate is seen in the variation in the dI/dV patterns between the faulted and unfaulted halves and in increases in dI/dV that spread across unit-cell boundaries. Finally, the corner Si adatom sites do not appear to contribute to the two-dimensional network, which is not especially surprising since they are not directly bonded to the Ga nanoclusters. These observations point to a 2DEG induced by the array of Ga nanoclusters. Clear evidence exists for an increased LDOS along specific channels or pathways, which is mediated by the close bonding of the nanoclusters with the substrate, thus forming a surface phase with electronic properties that are distinct from those of the clean Si(111)-7×7 surface.

The apparent 2DEG is most prominently observed between 0.75 and 1.50 V, but further dI/dV imaging of the Ga nanocluster array at sample biases beyond this range was also conducted. At biases above +1.50 V, increased differential tunneling conductance was observed primarily on individual Ga nanoclusters rather than spread across the entire array, suggesting that the states at those biases are localized rather than delocalized. At negative sample biases, the delocalized enhancement of the LDOS over the Ga nanocluster array was also suppressed. Finally, imaging at bias magnitudes below 0.50 V or above 2.50 V was unreliable because of instabilities in the STM probe.

A qualitative comparison of these experimental results with the calculations of Zhang et al.[37] indicate similarities in the LDOS of the nanocluster array as well as the presence of a two-dimensional interconnected network of charge rearrangement. However, efforts to seek further quantitative agreement are unwarranted because the conditions of our experiment are different from those of the computational study. In particular, experimental considerations required the use of n-type Si, while the computations assumed undoped Si. Furthermore, reliable measurements could only be achieved in the bias range of ±0.5 to ±2.5 V, whereas the computations focused on the range -1.0 to $+1.0$ V. Nevertheless, the qualitative agreement between experiment and theory is evident and justifies future computational effort that more closely approximates experimentally realizable conditions.

In conclusion, the electronic properties of self-assembled Ga nanocluster arrays on the Si(111)-7×7 surface have been mapped with atomic-scale spatial resolution. The differential tunneling conductance maps show regions of increased LDOS that form an interconnected two-dimensional network where the Ga nanoclusters are present. Furthermore, this enhancement of the LDOS abruptly disappears over clean Si(111)-7×7 unit cells, which suggests that selective masking of Ga nanocluster formation could be a potential pathway for nanopatterning the electronic structure of this surface. These results further indicate that a delocalized 2DEG has been induced by the Ga nanocluster array, which was previously predicted theoretically for metal nanocluster arrays on the Si(111)-7×7 surface. Close integration of the Ga nanocluster array with the Si substrate is manifested in differences in the LDOS between the faulted and unfaulted unit cell halves and in charge delocalization that extends over entire half cells that connect adjacent nanoclusters. This atomic-scale knowledge of the electronic properties of nanocluster arrays on silicon is likely to impact further fundamental studies and possible nanoelectronic device applications.

Experimental Section

The experiments were performed using a home-built UHV STM system with separate preparation and imaging chambers operating at room temperature and a base pressure of 5×10^{-11} Torr.[45] STM imaging employed commercially available PtIr tips (Materials Analytical Research) and W tips that were electrochemically etched in our laboratory. The Si(111) substrates (Virginia Semiconductor) possess the following characteristics: n-type, degenerately As-doped, resistivity $<0.005\,\Omega$ cm, miscut angle $\pm0.5\,^{\circ}$. The Si(111) samples were degreased using organic solvents prior to loading into the UHV chamber. Once in UHV, the samples were thoroughly outgassed at 600 °C by resistive heating. To prepare the clean Si(111)-7×7 reconstructed surface, the sample was annealed at 1220 °C for 30 s, then slowly cooled (ca. 6 °C s^{-1}) to 900 °C where it was held for 90 s, and then further cooled (ca. 12 °C s^{-1}) to room temperature.

The Ga metal (99.99999% purity, Alfa Aesar) was placed in an alumina-coated W wire boat and then thoroughly outgassed in the UHV chamber. The boat was resistively heated to achieve a steady flux of Ga atoms at which point the Si sample was held in the metal flux at a distance of approximately 2–3 cm from the Ga source. The substrate was then annealed at approximately 300 °C for several minutes to form uniform nanoclusters. The deposition time was adjusted between 10 to 45 s to achieve Ga nanocluster coverage levels ranging from isolated nanoclusters to a full array.

Topographic STM scans were performed in constant-current mode with the bias voltage applied to the sample with respect to the tip, which was electrically grounded through a current preamplifier. To measure the differential tunneling conductance (dI/dV), a periodic dither signal (10 kHz frequency, 40 mV RMS amplitude) was superimposed on the applied sample voltage. The tunneling current response at the same frequency was measured using a lock-in amplifier (Stanford Research Systems). The tunneling current and differential tunneling conductance were recorded simultaneously to produce topographic and (dI/dV) maps over the same area.

Keywords:

electronic structure · scanning tunneling microscopy · self-assembly · semiconductor nanocrystals · surface patterning

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