SAR ADC architecture with 98% reduction in switching energy over conventional scheme

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A high energy-efficiency switching scheme for a successive approximation register (SAR) analogue-to-digital converter (ADC) is presented. The proposed method can achieve 98.4% savings in switching energy when compared to a conventional SAR. The proposed technique also achieves a 4 × reduction in total capacitance used in the digital-to-analogue converter (DAC) compared to the conventional DAC.

Introduction: The SAR ADC is a very popular choice for low power analogue-to-digital conversion. The highly digital nature of the SAR combined with its low power sets it up to reap the full benefits of technology scaling. This has led to a renewed interest of the research community in the SAR as the ADC of the future. Many studies have been carried out in recent times to reduce the switching power of the DAC [1–5]. The split-capacitor technique of [1] achieves a 37% reduction in switching energy compared to a conventional SAR. The monotonic switching technique of [2] achieves an 81% reduction in switching energy. The V_{cm}-based switching technique of [3] reduces the switching energy by 88% compared to the conventional technique, while the reduction in switching energy achieved by the MCS technique of [4] is 93.4%. The technique of [5] achieves 96.9% reduction in switching energy. In this Letter, a new switching technique is presented that achieves a reduction of 98.4% in the switching energy of the DAC.

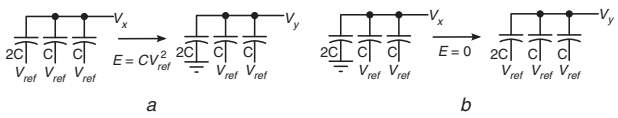

Fig. 1 *Illustration of idea behind initial sequence used in DAC*

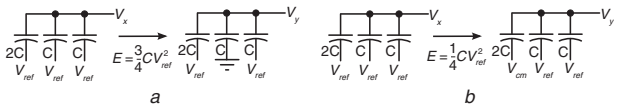

Fig. 2 *Illustration of idea behind energy saving*

SAR switching scheme: The key to reducing switching energy in the capacitive DAC is to cut down on the energy consumed in the first few comparison cycles since that is when the bulk of the switching energy is consumed. Use of top-plate sampling ensures that the switching energy is zero during the first comparison cycle. In the proposed scheme, the bottom-plates of the capacitors in the DAC are initially loaded with the sequence [011···1], i.e. the bottom-plate of the most-significant bit (MSB) capacitor is initially setto '0', and the bottom-plates of the other capacitors are set to V_{ref}. Thus every cycle, only one capacitor needs to switch. The reason for using this sequence instead of charging the bottom-plates of the capacitors to all '0's or all '1's can be appreciated from Fig. 1.

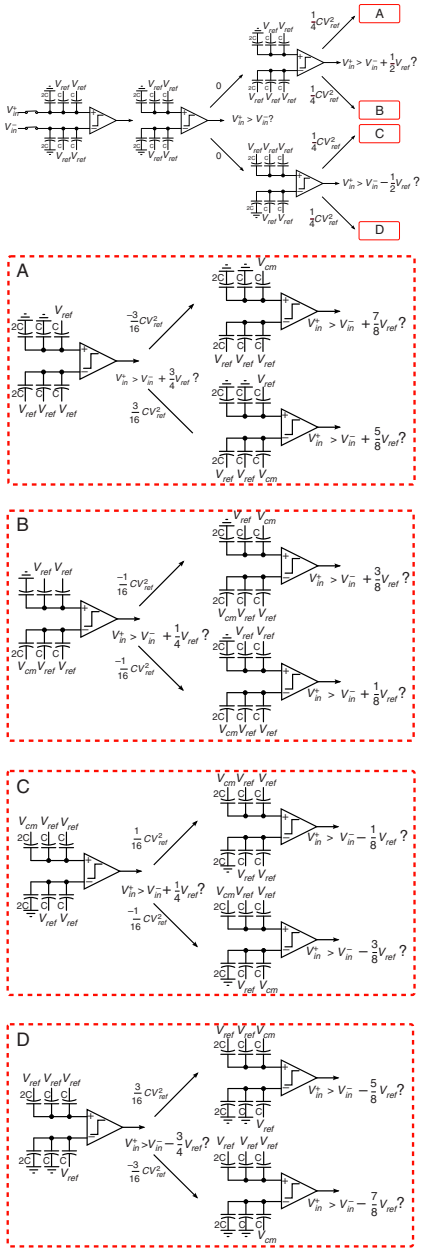

Fig. 3 *Proposed switching technique applied to 4-bit SAR*

Let us assume that the capacitors are initially all discharged. As can be seen from Fig. 1*a*, an energy of CV_{ref}^2 is required to discharge the '2C' capacitor from V_{ref} to '0'. In Fig. 1*b*, the energy required to charge up the '2C' capacitor from '0' to V_{ref} is provided by the '1C' capacitors and no net energy is drawn from V_{ref}, resulting in zero energy transfer. It can be easily shown that an energy of CV_{ref}^2 is also consumed if all the capacitors were initially connected to '0' instead of V_{ref}. Thus, by adopting the initial sequence used in the proposed switching technique, the switching energy during the second comparison cycle can also be set to zero. The switching energy can be saved further by utilising the technique illustrated in Fig. 2. It is easy to see that discharging the bottom-plate of the capacitor $C_i (i \neq \{0, N\})$ in the DAC array $[C_N C_{N-1} \cdots C_1 C_0]$ from V_{ref} to '0' is equivalent to keeping the bottom-plate of C_i at V_{ref} and instead discharging the bottom-plate of C_{i+1} from V_{ref} to $V_{cm} = V_{ref}/2$. Fig. 2 shows that much less switching energy is consumed if the bottom-plate of C_{i+1} is discharged to V_{cm} instead of discharging the bottom-plate of C_i to '0'. This technique has been incorporated in the proposed switching scheme. In addition, the proposed technique achieves a 4 × reduction in the total capacitance in the DAC by switching C_0 between (V_{ref}, V_{cm}) instead of (V_{ref}, 0) which allows an additional 2-bits of resolution compared to a conventional DAC with the same total capacitance. Fig. 3 illustrates the proposed switching technique for a 4-bit SAR ADC. The input is initially sampled onto the top-plates of the capacitor array and the sequence

[011···1] on the bottom-plates of the capacitor array. No switching energy is consumed in the first comparison due to top-plate sampling. The second comparison follows the principle illustrated in Fig. 1 and hence does not consume any switching energy either. Subsequent comparisons follow the technique illustrated in Fig. 2 and hence consume a lot lower switching energy than the techniques reported in the literature. The penultimate comparison also draws zero average switching energy as shown in Fig. 3. It should be pointed out here that a negative switching energy is not non-physical; rather it implies that the DAC gives energy back to the reference voltage sources. Switching the LSB capacitors between (V_{ref}, V_{cm}) allows an additional comparison to be made and the outputs of the comparator are combined with the DAC outputs to give the final result. This allows a total of 4 × reduction in capacitance of the DAC compared to the conventional technique. A 2 × reduction in capacitance of the DAC is reported in [2–4] while [5] also achieves a 4 × reduction in capacitance. Reference [5] achieves the additional 2 × reduction over [2–4] at the cost of input-dependent common-mode voltage variation at the comparator's inputs. The input-dependent variation of the common-mode voltage can lead to increased harmonic distortion at the output. In contrast, in the proposed scheme, the common-mode voltage at the comparator's inputs is independent of the input signal. The common-mode voltage starts at V_{cm}, goes up to $1.5V_{cm}$ in the second cycle, and gradually converges towards V_{cm}.

Comparison with existing switching schemes: A behavioural simulation of the different switching techniques for a 10-bit SAR ADC was performed in MATLAB for comparison with the proposed scheme and is shown in Fig. 4.

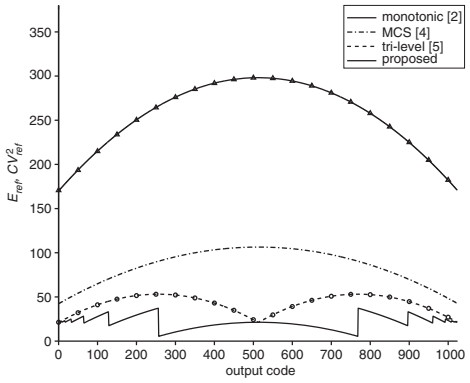

Fig. 4 *Switching energy comparison for 10-bit SAR*

The average switching energy for a 10-bit conventional SAR is $1363.3CV_{ref}^2$ whereas the switching energy for a 10-bit SAR using the proposed technique is only $21.3CV_{ref}^2$ which amounts to a reduction of 98.4% in the switching energy. The switching energy numbers for the different techniques are given in Table 1.

Table 1: Comparison of switching techniques for 10-bit SAR

Switching method	Switching energy (CV_{ref}^2)	Energy savings (%)
Conventional	1363.3	0
Monotonic [2]	255.5	81.2
MCS [4]	85.1	93.7
Tri-level [5]	42.4	96.9
This work	21.3	98.4

It can be seen from Table 1 that the switching energy of the proposed scheme is half that of the highest energy-efficiency technique reported in the literature [5].

Conclusion: A high energy-efficiency capacitor switching scheme for the SAR ADC, with energy savings of 98.4% compared to the conventional switching technique, is presented. The proposed technique has only one switching every comparison cycle, thus saving greatly on the power required to drive the switches in the DAC. In addition, the proposed technique achieves a 4 × reduction in total capacitance compared to a conventional SAR, thus offering an additional 2-bits of resolution for the same total capacitance.

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One or more of the Figures in this Letter are available in colour online.

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