(Special Session)

Machine-learning based Blind Digital Calibration of Time-Interleaved ADC

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***Abstract*—This work presents a supervised machine learning (ML) technique to suppress static and dynamic errors in time-interleaved (TI) successive-approximation-register (SAR) analog-to-digital converters (ADCs). Traditional methods rely on high-speed buffers and complex calibration algorithms to address reference ripple, gain mismatch, timing mismatch, and offset mismatch, increasing area/cost and design complexity. By contrast, the proposed ML-based approach uses a low-speed SAR ADC to digitally correct these errors, enhancing performance and lowering power consumption without requiring implicit knowledge of error sources or complex calibration procedures. The proposed ML calibration is demonstrated on a 2-channel time-interleaved ADC test-chip fabricated in 28nm CMOS and improves SNDR/SFDR by more than 21/38dB respectively.**

keywords- successive approximation register (SAR), analog-to-digital converter (ADC), machine learning, time-interleaving

I. Introduction

Time-interleaving of low-speed analog-to-digital converters (ADCs) is the most widely used approach to reach high-speeds using silicon. Successive approximation register (SAR) has emerged as the choice of architecture for time-interleaved ADCs (TI-ADCs) due to the mostly digital architecture of SAR ADC and its high energy-efficiency. The key challenges in designing high-performance SAR TI-ADCs are - a) regulation of reference voltage for each SAR ADC; b) mismatches (gain, timing, offset and bandwidth) between each sub-ADC. As the capacitors in SAR ADC switch during conversion, the reference voltage line is disturbed. For high-speed SAR ADCs, ripples on the reference voltage line do not settle before the next conversion which might lead to incorrect bit decisions and manifest as spurs and increased noise floor in the SAR output. For TI-ADCs, mismatches between each sub-ADC further increases spurs and noise floor.

Several existing techniques address the key limitations of high-speed SAR ADCs. Ripples in reference line in high-speed SAR ADCs are suppressed through a variety of techniques, such as using pre-charged reservoir capacitors [1]–[3], dynamic reference regulation [4], charge neutralization [5], and canceling the reference ripple by emulating ripple with a replica DAC [6]. However, these techniques still need either a large reservoir capacitor or a clean supply voltage or are limited by replica matching. Similarly, many works have proposed background calibration techniques to address interleaving mismatches in TI-ADCs. While offset and gain mismatches are usually easy to calibrate digitally, time-skew calibration is the most challenging. Existing digital calibration techniques typically estimate error due to mismatches by either – a) extracting differences in cross-correlation of sub-ADC outputs to estimate time-skew [7], [8]; b) dithering the input buffer and cross-correlation of sub-ADC output with the injected dither to estimate time-skew [9], [10]; c) adaptive signal processing to suppress mismatches by minimizing correlations between the actual signal and its images [11], [12]. These techniques perform calibration with the erroneous ADC samples and have limited spurious free dynamic range (SFDR) usually less than 60dB. Additionally, some of these calibration techniques either require prior knowledge of signal frequency and do not work for multi-tone signals or require complicated frequency-domain techniques (shifting/folding/Hilbert transform) that are difficult to implement on-chip with low area/power cost. In contrast, this work proposes a supervised machine learning (ML) approach for blind digital calibration that uses a low-speed, high accuracy ADC as reference for comparing the erroneous ADC samples against and correcting errors. The use of a high accuracy reference ADC improves SFDR to $>$ 70dB in this work.

The rest of this paper is organized as follows: Section II presents a brief review of existing blind digital calibration techniques for both non-ML and ML approaches, Section III introduces the proposed technique, Section IV presents measurement results on a $2\times$ interleaved TI-ADC test-chip fabricated in 28nm CMOS, and finally, Section V brings up the conclusion.

II. Review of prior blind digital calibration and ML techniques

Blind digital calibration techniques perform error corrections in the digital domain after ADC conversion is complete. These techniques have the advantages of – a) not requiring any analog delay tuning, and thus, are insensitive to process, voltage and temperature variations; b) can leverage benefits of technology scaling to reduce hardware cost and can be easily migrated to any TI-ADC architecture on any technology node. Recent blind digital calibration techniques can be grouped into conventional signal processing techniques based on digital mixing and ML based approaches. Traditional signal processing based blind digital calibration techniques can be further grouped into three categories. The first category extracts timing skew from correlations between the sub-ADCs

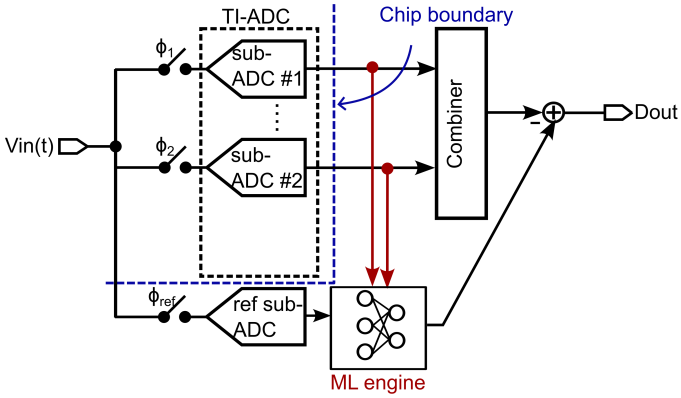


Fig. 1: Proposed TI-ADC architecture with supervised ML calibration

in a TI-ADC. The work in [13] extracts polarity of timing skew from digital mixing while [8], [14] extracts the timing-skew itself by calculating derivative of auto-correlation function. However, [8], [14] needs knowledge of the signal frequency for Hilbert transform that is used for calculating derivative of the ADC output which limits the application of this work. The second category combines digital mixing and redundancy to calculate derivative of auto-correlation function without requiring knowledge of the input signal statistics. However, this advantage comes at the cost of significant overhead due to the need of multiple redundant sub-ADCs as well as the need for careful control of timing skew between main and auxiliary sub-ADCs. The third category [11] minimizes correlation between the original signal and its images to suppress errors due to interleaving mismatches. While this technique does not need to knowledge of input signal statistics, it needs complicated signal processing techniques such as frequency shifting, folding and Hilbert transform for computing images. Additionally, all these conventional digital mixing techniques use erroneous TI-ADC samples for all computations which limits the improvement in ADC performance after calibration.

A few recent works have applied supervised ML to improve TI-ADC performance [15]–[18]. While [17], [18] presents simulation results, [15], [18] presents measurement results on test-chip. All these techniques generate ground truth through digital filtering of the actual ADC output or fitting a sine-wave on the ADC output during training with sinusoidal inputs. This can lead to the ML model converging to incorrect local minima. [16] addresses this by re-fitting the ADC output to a sinewave recursively. In contrast, this work uses a reference ADC to generate ground truth for training which ensures that the ML model will always converge to the correct operating point.

III. Proposed Architecture

A. ADC design

Fig. 1 shows the proposed TI-ADC architecture with supervised ML calibration. A low-speed SAR ADC is used as reference ADC whose output samples align alternately with samples from one of the two interleaved sub-ADCs. The ML model is trained when the reference and sub-ADC samples align. To reduce the training requirement, the ML model is trained to estimate only errors between the main TI-ADC and reference ADC outputs rather than letting the ML model learn the sub-ADC transfer functions. While the training happens only when the sampling instants of the main and sub-ADCs are aligned, the trained ML model performs calibration for all the TI-ADC outputs.

The main ADC is a (11+1)-bit, top-plate sampled synchronous SAR ADC with 1-bit redundancy and unit capacitor of 0.6fF. The ADC uses bi-directional single-sided switching (BDSS) technique to reduce switching energy [19]. In this work, the reference ADC used for supervised ML training is a copy of the main ADC but runs at Fs/15 where the Fs is the sampling speed of the main TI-ADC. The speed of the main TI-ADC is an odd integer multiple of the reference ADC which ensures that the reference ADC aligns with samples from both sub-ADCs and the ML model learns errors in both sub-ADCs. In-order to achieve high SFDR without requiring a complex deep neural network for calibration, this work proposes a circuits-informed approach that allows the use of a shallow artificial neural network (ANN). The proposed technique derives insights from ADC behavior to extract key features for training the ANN. Static errors, such as capacitance mismatch and comparator offset can be estimated by comparing the main ADC and reference ADC outputs directly when they align. On the other hand, dynamic errors depend upon both past and current ADC samples. Timing skew and bandwidth error depend upon derivative of the input signal, and hence, requires knowledge of both current and previous ADC samples. Similarly, reference ripple in SAR ADCs depend on outputs from previous conversions. Hence, the current and several past samples of the main ADC output are used as features to the ML model for calibrating both dynamic and static errors. The ANN adaptively computes derivatives from the current and past samples of the main ADC without requiring knowledge of the input signal. Since, the derivative computation is a function of the input statistics, the ANN has to keep training in the background.

The ADCs used in this work does not use reference decoupling capacitors or on-chip reference buffers which reduces area and power costs but comes with the trade-off of increased reference line ripple which leads to spurs in the output. The inadequate reference line regulation is also corrected by the proposed ML calibration. One of the sub-ADCs from another chip is used as reference ADC in this work. Since the reference ADC runs at much slower speed than the main ADC, its performance is not degraded by reference ripple. A one-time foreground calibration is performed on the reference ADC to suppress capacitor mismatch.

B. ML model

A two-layer ANN is used in this work. The ANN has one hidden layer with tanh activation and an output layer with one neuron and linear activation. Fig. 2 plots the improvements

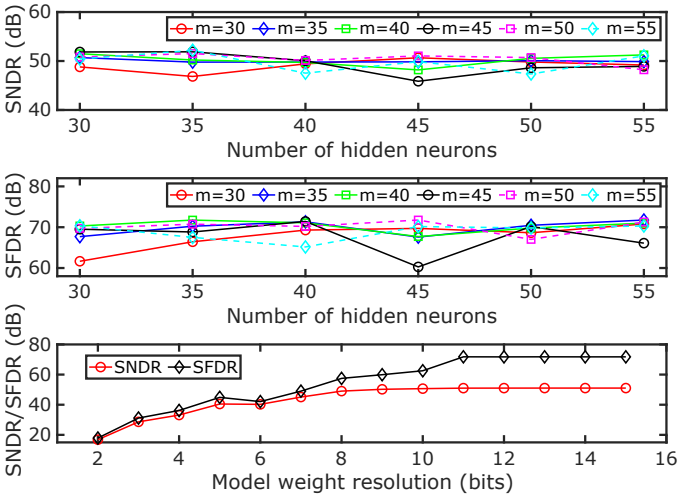


Fig. 2: SNDR/SFDR as a function of ML parameters and SNDR/SFDR of main ADC after ML calibration as a function of model weight bit precision

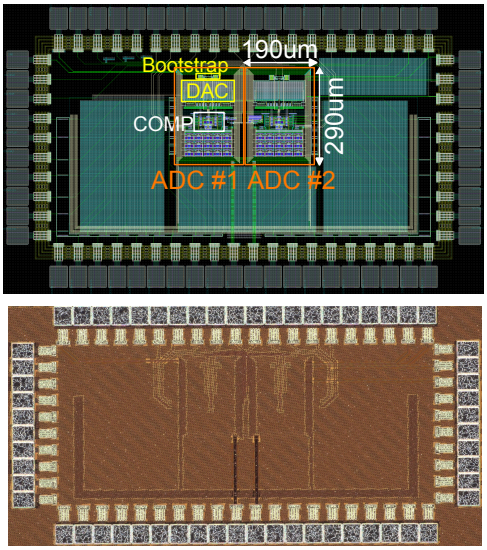


Fig. 3: Layout and die photograph of the ADC

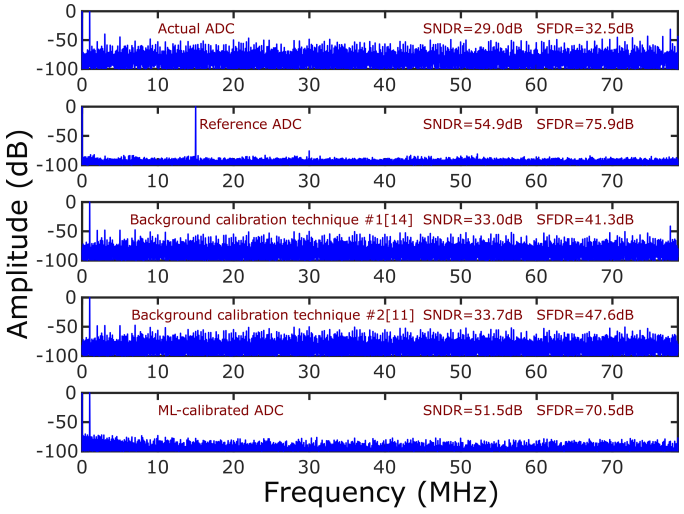
in SNDR and SFDR as a function of the number of hidden neurons and number of features (m). The ANN performance initially improves and then saturates as the model size becomes larger. For this work, the number of hidden neurons and number of features are selected as 45 and 50 respectively. Fig. 2 also plots the SNDR and SFDR of the main ADC after calibration as a function of model weight precision. A 12-point fixed-precision is used for the ANN implementation. The small size of the ANN model is a key enabler for it to be included in the back-end DSP for calibration. The ML model also needs fast convergence, and plots the SNDR and SFDR convergence performance with different popular backpropagation algorithms. RMSprop algorithm is used for backpropagation [20] which results in faster convergence than gradient descent since the learning rate for each model weight is tuned adaptively throughout the training instead of using a fixed, global learning rate for all the model weights. The trade-off for quicker convergence comes at the cost of increased hardware but the power consumption of training the model is lower compared to inference since the training happens at a lower speed than that of the main ADC.

IV. Measurement Results

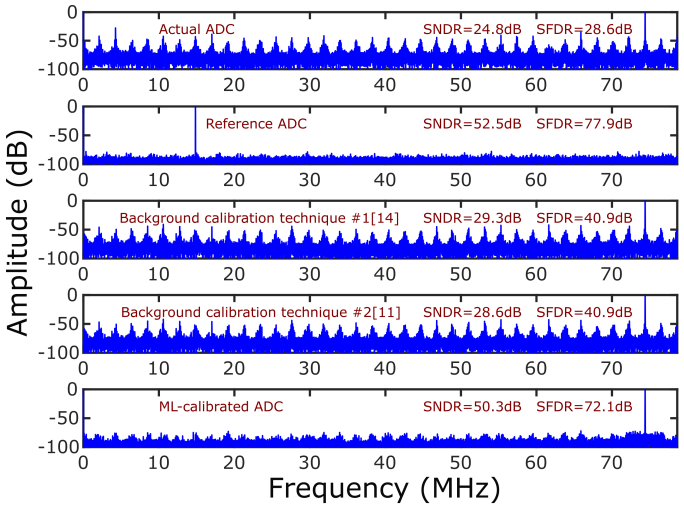
Fig. 3 shows layout and die photo of a test-chip fabricated in 28nm CMOS. The TI-ADC operates at 157.5MHz while the reference ADC operates at 10.5MHz. The TI-ADC consumes 2.1mW at Fs=157.5MHz and the reference ADC consumes 0.1mW at Fs=10.5MHz from 0.9V supply. The ML model is synthesized digitally and is estimated to consume 1.16mW from 0.5V supply (0.62mW for training and 0.54mW for inference) with 12-bit fixed-point precision. Fig. 4 plots the measured FFT of the TI-ADC before and after proposed ML correction as well as with background calibration techniques from [14] and [11] for low frequency and near-nyquist input for 1V pk-pk amplitude sinusoid signals. Fig. 4a) shows results for 1MHz input frequency. After digital gain and offset calibration, the TI-ADC has SNDR/SFDR of 29/32.5dB which is primarily limited by reference ripple. The low-speed reference ADC has SNDR/SFDR of 54.9/75.9dB. The background calibration techniques of [11], [14] improves SNDR/SFDR to 33/41.3dB and 33.7/47.6dB respectively and only suppresses mismatches between the two sub-ADCs. In contrast, the proposed ML calibration suppress both errors due to reference ripple and interleaving mismatches and improves SNDR/SFDR to 51.5/70.5dB. As shown in Fig. 4b), the TI-ADC performance is further degraded at 74MHz input frequency due to timing mismatches with SNDR/SFDR of 24.8/28.6dB and is improved to 50.3/72.1dB after the proposed ML calibration. The SNDR/SFDR improvement from the background calibration techniques of [11], [14] is still limited by reference ripple even though they improve SFDR by approximately 12dB over the original TI-ADC compared to 9dB at 1MHz input frequency. The proposed ML calibration improves DNL/INL from 123.8/-158.2 LSB to 0.8/-3 LSB respectively as shown in Fig. 5. Fig. 6 summarizes performance of the proposed ADC. The proposed ML calibration significantly improves both SNDR/SFDR as well as energy-efficiency of the ADC which is captured by Walden figure-of-merit (FoM).

V. Conclusion

This work has presented an ML approach to correcting errors in time-interleaved ADCs through supervised learning. The proposed technique results in significant improvement in SNDR and SFDR of TI-ADCs through fully digital back-end correction without requiring complex circuit design efforts or detailed knowledge of error sources. A 2-channel TI-ADC with relatively low sampling frequency is used in this work as proof-of-concept, but the ML calibration will be applied to our future GHz speed TI-ADCs. While the ML model is off-chip for this work, the relatively small size and simple architecture



(a)



(b)

Fig. 4: Measured FFT of actual, reference and calibrated ADCs for input frequencies of a) 1MHz b) 74MHz

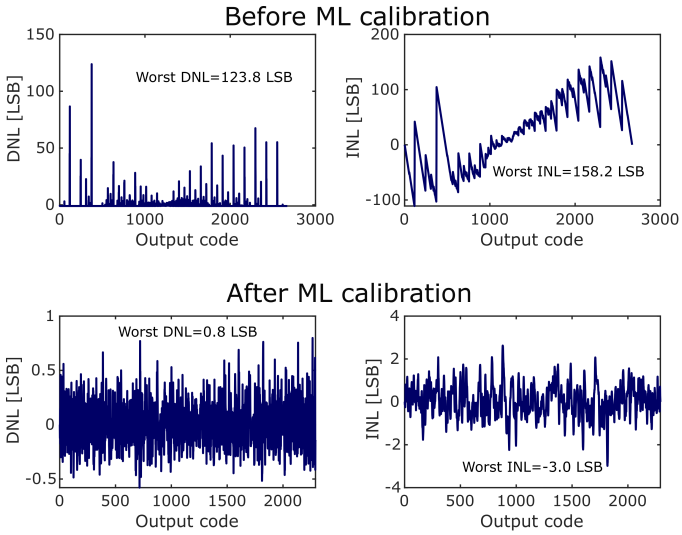


Fig. 5: Measured DNL and INL plots before and after ML correction

Process	28nm	
Architecture	2x time-interleaved SAR ADC	
Supply voltage	0.9V (ADC)/ 0.5V (Machine learning)	
Speed	157.5MHz (TI-ADC)/ 10.5 MHz (reference ADC)	
Errors calibrated	Interleaving mismatch, reference ripple	
	Before calibration	After calibration
SNDR	29dB@1MHz, 24.8dB@74MHz	51.5dB@1MHz, 50.3dB@74MHz
SFDR	32.5dB@1MHz, 28.6dB@74MHz	70.5dB@1MHz, 72.1dB@74MHz
INL/DNL	158.2/123.8 LSB	-3/0.8 LSB
Power	2.1mW	3.36mW
Walden FoM	573.1fJ/step@1MHz, 931.1fJ/step@74MHz	68.1fJ/step@1MHz, 78.3fJ/step@74MHz

Walden FoM = Power/2^ENOB/Sampling frequency where ENOB = (SNDR-1.76)/6

Fig. 6: Performance summary of the test-chip

of the model needed underscores the possibility of integration of ML into ADC chips for real-time error correction given the recent advances in high energy-efficiency ML accelerators in silicon.

VI. Acknowledgements

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