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A 13.2-fJ/Step 74.3-dB SNDR Pipelined Noise-Shaping SAR+VCO ADC

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(Invited Paper)

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ABSTRACT This work presents an OTA-free pipelined passive noise-shaping successive approximation register (NS-SAR) + VCO ADC that offers high resolution (>12-bit) with only a 5-bit NS-SAR stage and 4×–36× lower sampling capacitor compared to state-of-the-art NS-SARs with similar ENOB. Pipelining the NS-SAR and VCO stage linearizes VCO by reducing its input swing, increases the VCO integration time and its energy efficiency, and improves the SFDR of ADC by suppressing frequency dependency of interstage gain. We demonstrate a simple calibration technique to extract interstage gain and track VCO gain accurately in the background. Fabricated in 65-nm CMOS, the prototype ADC achieves the best Walden FoM among state-of-the-art passive NS-SAR ADCs in similar technology and consumes 0.12 mW with SNDR/SFDR of 74.3/89.1 dB at 13.2 fJ/step for OSR of 9.

INDEX TERMS Interstage gain calibration and pipelined ADC, noise-shaping successive approximation register (NS-SAR), oversampling ADC, ring VCO.

I. INTRODUCTION

NOISE-SHAPING successive approximation register (NS-SAR) combines advantages of both SAR and ΔΣ modulators [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11]. NS-SAR filters and feeds back the previous conversion residue to enable noise-shaping as shown in Fig. 1. Based on the implementation of the loop filter, NS-SAR ADCs can be grouped into cascaded integrated feedforward (CIFF) structure or error-feedback structure, with most of the NS-SAR implementations being CIFF. The key advantage of error-feedback structure over CIFF is the use of single-input comparator compared to multi-input comparator needed in CIFF structures that come with increased noise. While the loop filter in CIFF structure needs active amplifiers for pushing the NS-SAR noise-transfer function (NTF) zero closer to dc for more suppression of quantization error in the signal band, the error-feedback architecture allows NTF zero optimization without active amplifiers. However, active amplification is still used in error-feedback structure [9] to suppress noise contributed by the error-feedback path.

Passive loop filter [2], [11], [12], [13] has the advantages of avoiding amplifiers at the cost of weak noise-shaping at low oversampling ratio (OSR). Active integrators with open-loop amplifiers have simple architecture and high energy efficiency [7], [8], [14] but are sensitive to PVT variations that can potentially make the NS-SAR unstable

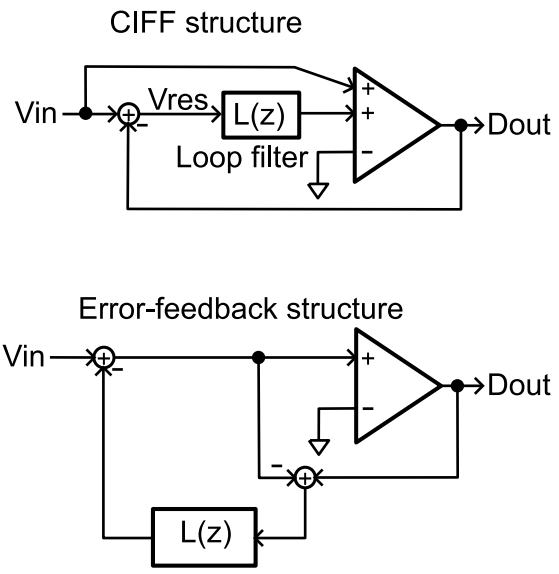
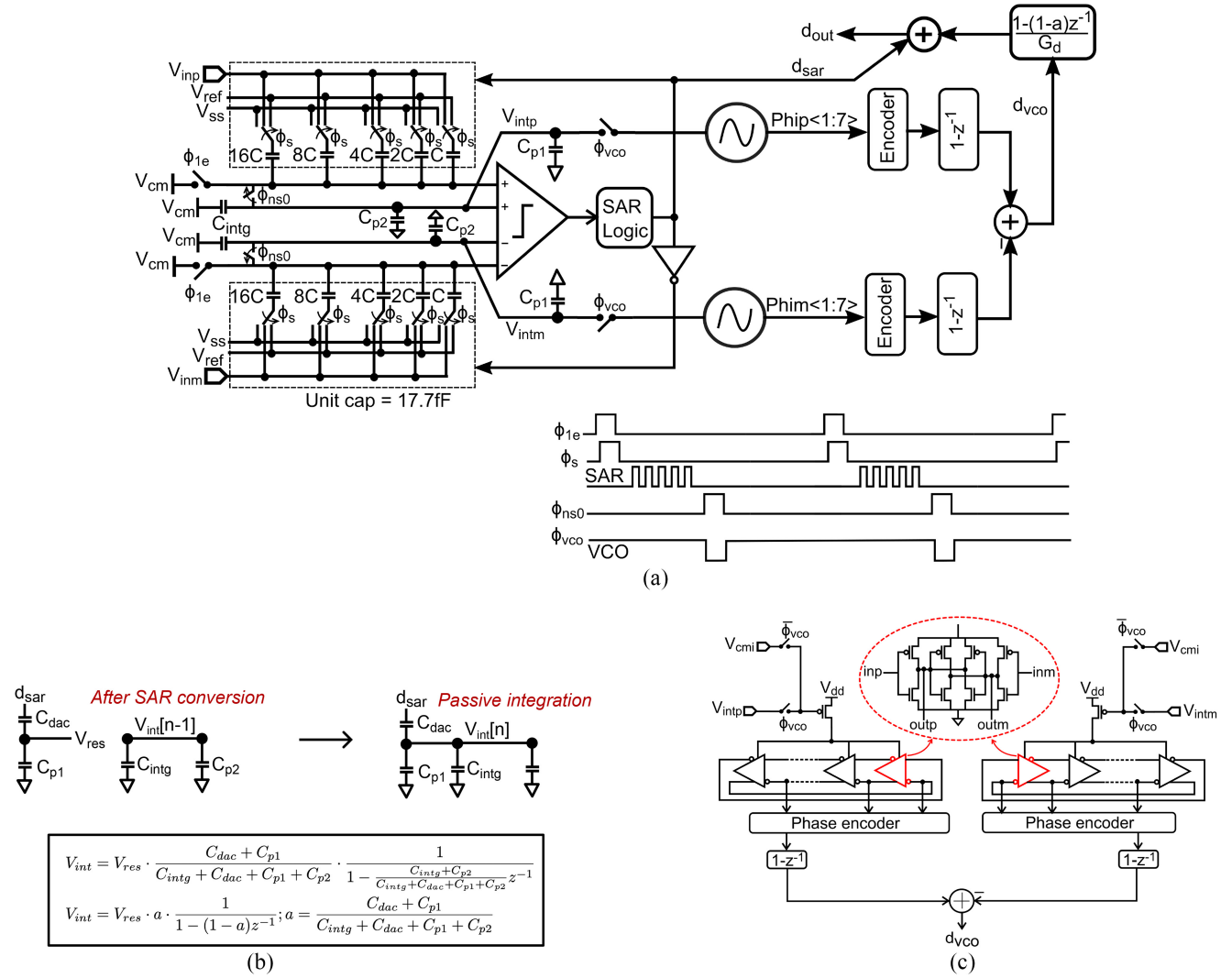


FIGURE 1. Abstracted block diagram of existing NS-SAR that can be grouped into CIFF or error-feedback structures.



$$V_{int} = V_{res} \cdot \frac{C_{dac} + C_{p1}}{C_{intg} + C_{dac} + C_{p1} + C_{p2}} \cdot \frac{1}{1 - \frac{C_{intg}+C_{p2}}{C_{intg}+C_{dac}+C_{p1}+C_{p2}} z^{-1}}$$

$$V_{int} = V_{res} \cdot a \cdot \frac{1}{1-(1-a)z^{-1}}; a = \frac{C_{dac} + C_{p1}}{C_{intg} + C_{dac} + C_{p1} + C_{p2}}$$

FIGURE 2. (a) Schematic and timing diagram of the proposed NS-SAR+VCO ADC. (b) Charge domain behavior of the passive integrator. (c) Circuit schematic of the VCO stage.

without background gain calibration [14]. Closed-loop dynamic amplifiers are more robust against PVT variations but need complex optimization [15]. Despite recent advances, state-of-the-art NS-SARs still need high-resolution SAR quantizer, i.e., at least 10-bit SAR to achieve >12-bit performance at low OSR which brings the additional challenge of driving a large sampling capacitor. Our prior work [16] presented a MASH architecture with NS-SAR as the first stage and a ring voltage controlled oscillator (VCO) as the second stage to relax capacitor driving requirements. However, the MASH architecture creates a frequency-dependent interstage gain that limits suppression of quantization error from NS-SAR at ADC output and reduces SFDR of the ADC. Further, the VCO is used as integrator only when the NS-SAR is not quantizing which limits energy efficiency of the VCO.

This work proposes a pipelined NS-SAR+VCO architecture that addresses the above challenges and brings the following advantages: 1) the VCO suppresses quantization error and comparator noise of SAR stage which address weak noise-shaping from passive integrator; 2) the NS-SAR resolution is low (5-bit) which relaxes the requirements for driving sampling capacitor; 3) the passive integrator linearizes VCO by limiting its input swing; and 4) pipelining suppresses frequency dependence of interstage gain, and improves SFDR by 8 dB and ADC energy efficiency by 2× compared to the MASH architecture in [16]. CIFF architecture is adopted in this work for the NS-SAR stage since the VCO suppresses multi-input comparator noise at the ADC output. This avoids the need for active amplifier in the error-feedback path as in [9]. Section II presents the proposed architecture with detailed noise analysis and interstage gain calibration technique, Section III presents measurement results on 65-nm test-chip and comparison with state-of-the-art, and Section IV brings up the conclusion.

II. PROPOSED PIPELINED NS-SAR+VCO

A. ARCHITECTURE

The proposed pipelined NS-SAR+VCO architecture and associated timing diagram are shown in Fig. 2. The input

signal is sampled during ϕ_s and 5 cycles of SAR conversion follow the sampling phase. After the SAR conversion is over, the residue is dumped on the capacitor C_{intg} which realizes passive integration of the SAR residue during ϕ_{ns0} phase. Thus, the NS-SAR effectively behaves as a feedforward $\Delta\Sigma$ modulator with first-order noise shaping with a signal transfer function (STF) of 1 and noise transfer function (NTF) of $[1-(1-a)z^{-1}]$ where $a = (C_{dac} + C_{p1})/(C_{dac} + C_{intg} + C_{p1} + C_{p2})$ and C_{dac} is the SAR DAC capacitance, and C_{p1} and C_{p2} are parasitic capacitances at the charge conservation node and passive integration node, respectively. Direct integration of SAR residue on C_{intg} instead of charge-sharing with a small capacitor before integration [16] reduces kT/C noise of SAR. The tradeoff with direct integration is that C_{intg} needs to be larger than C_{dac} to push NTF zero close to dc and ensure adequate in-band noise suppression. While this would necessitate a large C_{intg} in high-resolution NS-SAR ADCs with large C_{dac}, the proposed NS-SAR+VCO ADC uses a low-resolution SAR ADC thus ensuring that C_{intg} is still relatively small. In addition, the pipelined architecture cancels quantization noise in SAR thus relaxing the need for an aggressive NTF. Hence, the ratio of C_{intg}/C_{dac} is set to 3 in this design which results in NTF of $(1-0.75z^{-1})$. The unit capacitor in the SAR DAC is set to 17.7 fF in this work. The NS-SAR uses a 2-input comparator to add SAR residue and passive integrator output. While a 2-input comparator has higher noise than single input comparator, the pipelined architecture cancels comparator quantization noise and does not affect SNR of the ADC.

The passive integrator output is sent to the VCO for time-domain quantization. Due to pipelining, C_{intg} acts as zero-order hold for the VCO which performs integration over the entire ADC sampling period except for ϕ_{ns0} as shown in Fig. 2(a). This improves SQNR of the VCO stage and reduces frequency dependence of interstage gain which is discussed in Section II-C. Fig. 2(b) shows the circuit schematic for the second-stage VCO. A seven-stage current-starved ring inverter chain is used as the VCO. At any given time only one of the seven inverters in each VCO stage is undergoing transition, rising or falling. Thus, the 7-stage VCO quantizes the phase interval $(0,2\pi)$ into 14 levels corresponding to 7 rising transitions and 7 falling transitions. The quantized phase is in one-hot format that a phase encoder converts to binary word. The binary phase output is digitally differentiated to form the VCO stage output. The VCO output is digitally differentiated with NTF of NS-SAR and combined with the SAR output after scaling by interstage gain to form the overall ADC output.

Fig. 3 compares behavioral models of proposed ADC architecture with that in [16]. For this comparison, it is assumed that both ADCs have the same NS-SAR NTF, the same VCO back-end, and perfect interstage gain matching. Fig. 3(a) plots the thermal noise power from NS-SAR appearing at the ADC output as a function of NTF zero location for both ADCs after normalization by kT/C_{dac}. The

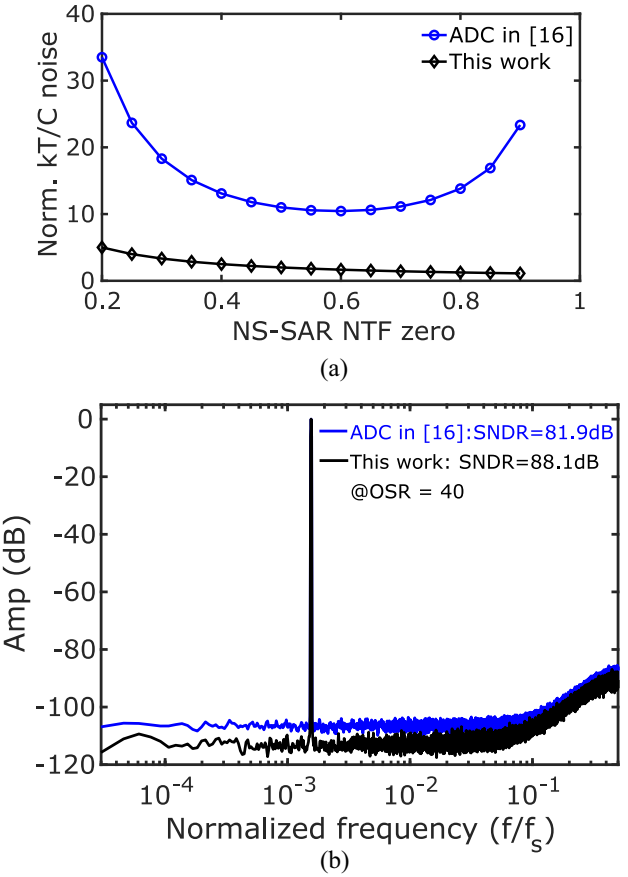


FIGURE 3. Comparison of (a) normalized kT/C noise power of the NS-SAR at the ADC output and (b) FFT plot between [16] and this work from behavioral model.

thermal noise increases as the NTF zero approaches both $f_s/4$ and dc ($z = 1$) for the ADC in [16] whereas thermal noise for the proposed ADC reduces as the NTF zero approaches dc. At $z = 0.75$, the proposed ADC has 9× lower thermal noise power. Fig. 3(b) plots the FFT for both ADCs. Compared to the ADC in [16], the proposed ADC has 6 dB better SNDR at OSR of 40. Detailed noise analysis of the proposed ADC is presented in Section II-D.

Fig. 4 shows a simplified mathematical model of the proposed ADC and its transfer functions. kT/C noise in SAR DAC and passive integrator are denoted by n_1 and n_2, respectively, $g = 1/a$ is gain of the integration path in the comparator, Q_1 is quantization noise in SAR, n_3 is thermal noise of comparator, δ represents capacitance mismatch error in SAR DAC, n_4 is VCO input-referred thermal noise, $G_{\text{vco}} = K_{\text{vco}}T_{\text{vco}}$ is VCO gain where K_{vco} is VCO tuning gain and T_{vco} is the VCO integration time, Q_2 is quantization noise in the VCO, and G_d is interstage gain. The ADC has very low sensitivity to g and precise matching/calibration is not needed to accurately set the value of g. After combining the NS-SAR and VCO outputs with the correct interstage gain, noise in the ADC output comprises of second-order shaped VCO quantization noise, first-order shaped VCO thermal noise, and unshaped DAC mismatch

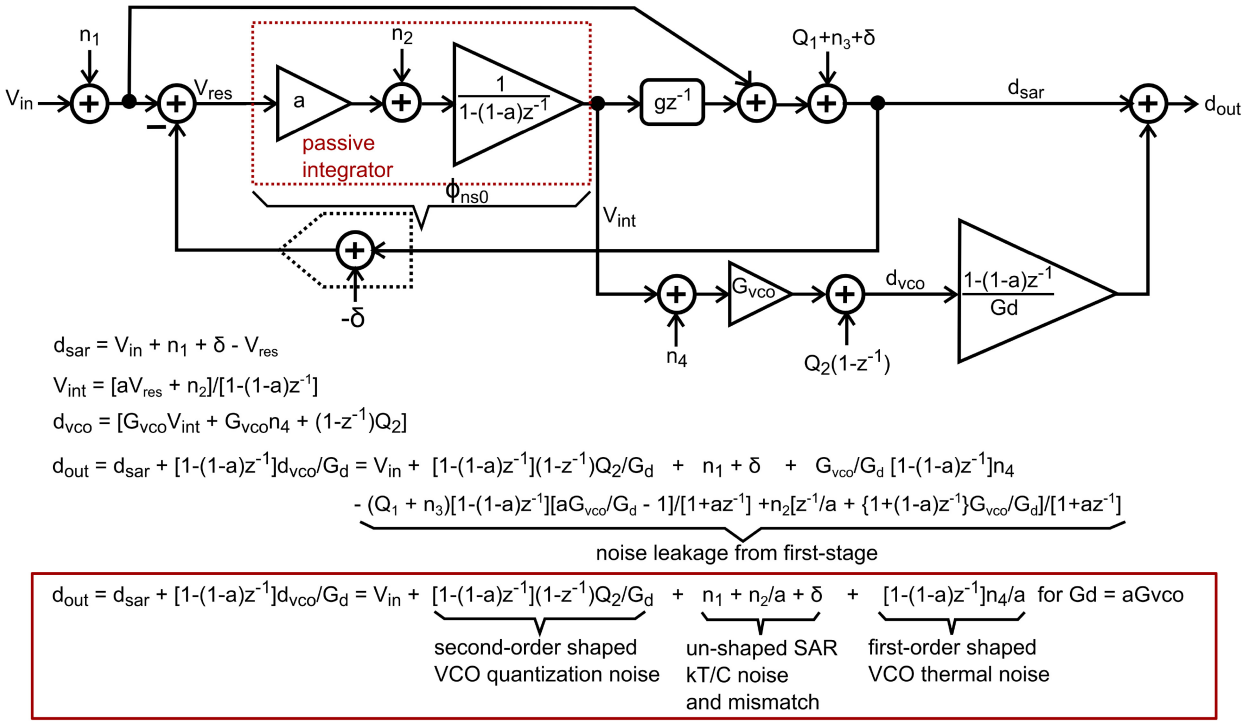


FIGURE 4. Mathematical model of the ADC.

error and kT/C noise from the NS-SAR stage which forms the in-band noise floor. An important property of the ADC is that the interstage gain error, denoted by $[aG_{\text{vco}}/G_d - 1]$ is high-pass shaped by NTF of the NS-SAR stage, i.e., $[1 - (1 - a)z^{-1}]$. This lends robustness to the ADC design and relaxes the interstage gain-matching requirement.

B. CHOICE OF NS-SAR RESOLUTION

The NS-SAR resolution determines energy efficiency of the ADC. If the NS-SAR resolution is too low, the VCO stage becomes highly nonlinear which limits ADC SNDR. On the other hand, if NS-SAR resolution is too high, the ADC power limits energy efficiency since the SAR comparator power increases by $4\times$ for every 1-bit increase in NS-SAR resolution. Even though the comparator noise is suppressed at the ADC output, it is important to reduce comparator noise with increase in NS-SAR resolution to prevent over-ranging the VCO stage. To optimize the NS-SAR resolution, simulations are performed by varying the NS-SAR resolution while keeping the overall ADC resolution around 14-bits at OSR=40. The SAR kT/C noise is kept unchanged for all NS-SAR resolutions. While the passive integrator's output swing scales with NS-SAR resolution, the VCO gain G_{vco} is adjusted to ensure the same quantization noise while keeping the number of inverters in the VCO fixed. Since tuning G_{vco} changes both VCO center frequency and gain proportionally, thermal noise from the VCO is unchanged. However, tuning G_{vco} exercises nonlinearity in the voltage-to-frequency conversion transfer function of the VCO. Fig. 5(a) shows the simulated nonlinear G_{vco} transfer curve as VCO input swing is varied while Fig. 5(b) shows the voltage swing at the VCO input node as a function of NS-SAR resolution. For 5-bit NS-SAR, nonlinearity in G_{vco} is not large enough and the ADC SNDR reduces by only 1 dB compared to perfectly linear case where G_{vco} does not vary with VCO input swing as shown in Fig. 5(c) and (d). However, if the NS-SAR resolution is reduced to 3-bit, the SNDR is reduced by more than 33 dB as shown in Fig. 5(e) since the first stage noise is not adequately suppressed due to nonlinear interstage gain as well as distortions introduced by the VCO stage itself. Fig. 5(f) plots the ADC Walden FoM and ENOB for OSR $=$ 40 as NS-SAR resolution is varied. At low NS-SAR resolution, the ENOB is limited by nonlinear G_{vco} which increases Walden FoM. On the other hand, at high NS-SAR resolution, energy efficiency is limited by increased power consumption without any improvement in ADC ENOB which increases Walden FoM. There is a shallow optima around NS-SAR resolutions between 4 and 6 bits and a 5-bit resolution is selected in this work for maximizing ADC energy efficiency.

C. INTERSTAGE GAIN

The interface between discrete-time (DT) SAR and continuous-time (CT) VCO introduces reconstruction error when outputs from the two stages are combined. Since the VCO quantizes the passive integrator output over a fraction of the ADC sampling period [during ϕ_{vco} phase in Fig. 2(a)], this effectively realizes a passive mixer in front of the VCO as shown in Fig. 6(a) [16]. Mixing spreads out frequency spectrum of the passive integrator output and creates multiple

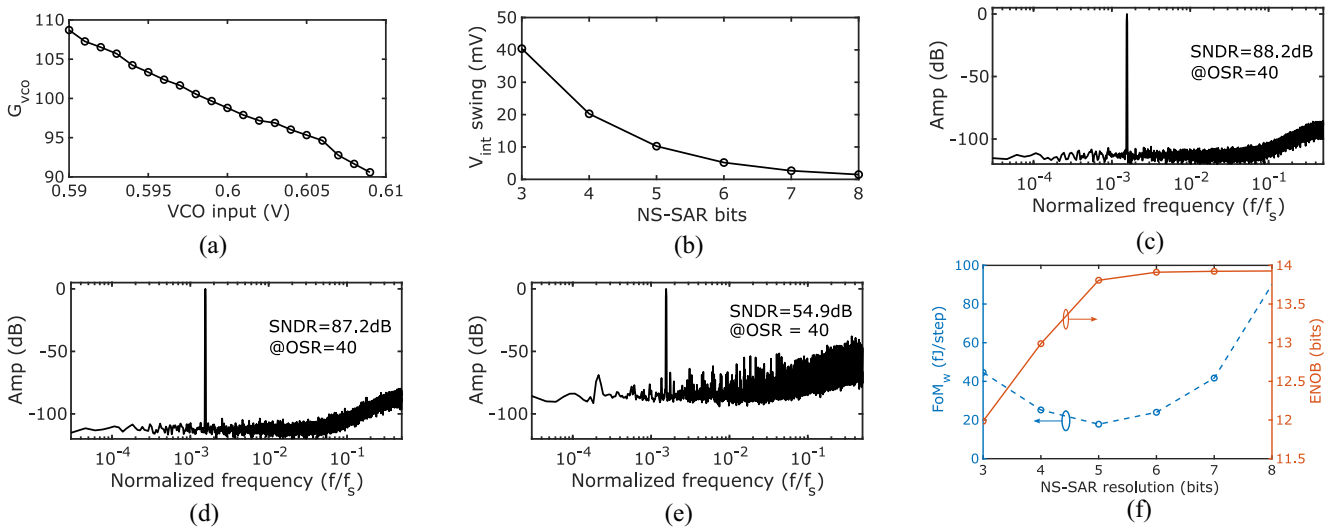


FIGURE 5. (a) Simulated G_{vco} as a function of VCO input voltage, (b) VCO input swing as a function of NS-SAR resolution, (c) simulated FFT with 5-bit NS-SAR assuming constant G_{vco}, (d) simulated FFT with 5-bit NS-SAR with G_{vco} transfer curve, (e) simulated FFT with 3-bit NS-SAR with G_{vco} transfer curve, and (f) ADC Walden FoM and ENOB as a function of NS-SAR resolution.

copies around harmonics of the ADC sampling frequency f_s. Anti-aliasing in the VCO attenuates the mixer output in higher Nyquist bands and hence the sampled VCO output is not a perfect reconstruction of the passive integrator output even if the VCO was an ideal quantizer. Thus, the interstage gain is frequency dependent and quantization noise from the first stage cannot be completely canceled at the ADC output.

Assuming the passive mixer is controlled by a pulse train $p(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_s t)$, where a_0 is the duty-cycle of ϕ_{vco}, Fig. 6(b) plots the interstage gain normalized by G_d for [16] and for this work. For the same ADC sampling frequency, pipelining increases the duty-cycle of ϕ_{vco} by $2\times$ in this work and reduces interstage gain variation with frequency by $20\times$ compared to that in [16]. The in-band quantization noise of the NS-SAR stage at the ADC output with an ideal VCO back-end can be written as

$$P_q = \frac{\left[1 + (1-a)^2 - 2(1-a)\right]}{12(OSR)^3} \frac{\Delta^2}{12} \left(\sum_{n=1} \frac{a_n}{n} \right)^2 \qquad (1)$$

where $a_n = (2/n\pi)\sin(nd\pi)$, and $\Delta^2/12$ is the quantization noise power of the 5-bit SAR. Longer duty cycle of $p(t)$ results in more attenuation of the in-band quantization error from NS-SAR stage. Thus, pipelining NS-SAR+VCO attenuates quantization noise from NS-SAR by more than 10 dB compared to the work in [16] as shown in Fig. 6(c). This relaxes the interstage gain matching requirement.

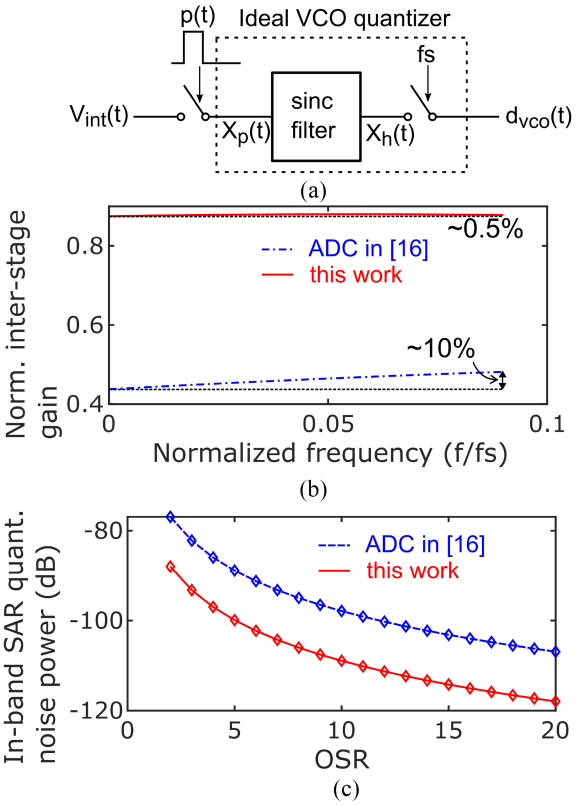


FIGURE 6. (a) Simplified block diagram of passive mixing and ideal VCO back-end quantizer, (b) normalized interstage gain versus frequency, and (c) in-band SAR quantization noise power comparison between [16] and this work.

D. NOISE ANALYSIS

1) SAR NOISE

Noise from the NS-SAR stage is due to kT/C noise in SAR DAC and passive integrator, and can be written as

$$\overline{n_1^2} = \frac{2kT}{C_{dac}} \cdot \frac{1}{\text{OSR}} \qquad (2)$$

and

$$\overline{n_2^2} = \frac{2kT}{C_{intg}} = \frac{2a^2}{1-a} \cdot \frac{kT}{C_{dac}} \cdot \frac{1}{\text{OSR}}. \qquad (3)$$

The kT/C noise from the passive integrator is scaled by $1/a$ and appears at the output as

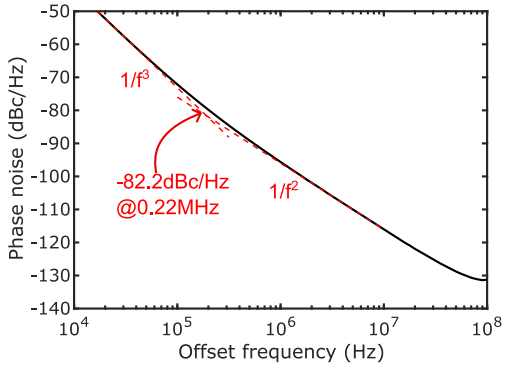


FIGURE 7. Simulated phase noise plot of VCO during its integration phase.

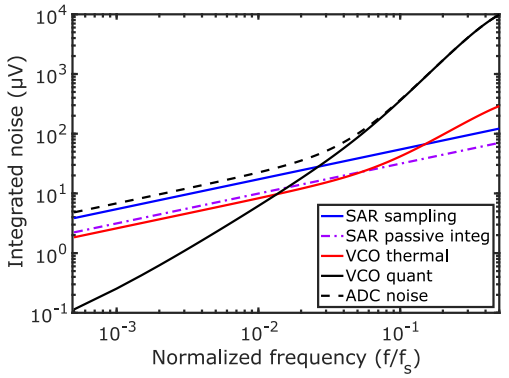


FIGURE 8. Simulated integrated noise at the ADC output from NS-SAR and VCO stages.

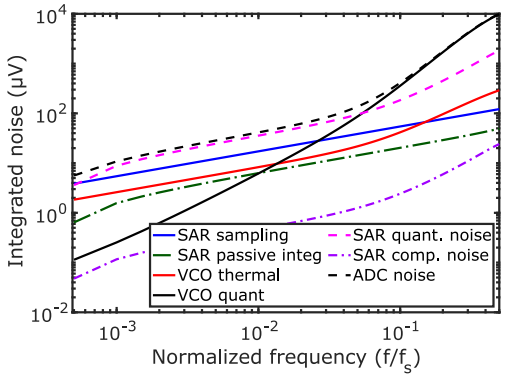


FIGURE 9. Simulated integrated noise at the ADC output from NS-SAR and VCO stages in the presence of 10% mismatch in interstage gain.

$$\frac{\overline{n_2^2}}{a} = \frac{a}{1-a} \cdot \frac{kT}{C_{dac}} \cdot \frac{1}{\text{OSR}} \tag{4}$$

where the factor of 2 in the numerator comes from differential implementation. For an OSR of 40, C_{dac} of 0.55 pF and $a = 0.25$, the in-band kT/C noise from the NS-SAR stage at the ADC output is 24.9 μV. Quantization noise and comparator noise from the NS-SAR are suppressed at the ADC output for perfect interstage gain matching.

2) VCO NOISE

Noise from the VCO stage comes from thermal noise as well as quantization noise. The input referred thermal noise due to the VCO stage is given by

$$\overline{n_4^2} = \frac{D_2(T_s - T_{\text{vco}}) + D_1 T_{\text{vco}}}{2\pi^2 (G_{\text{vco}})^2} \tag{5}$$

where D_1 is the phase diffusion constant [17] of the VCO during the integration phase ϕ_{vco} and D_2 is the phase diffusion constant of the VCO during its sampling phase. The phase diffusion constant D is evaluated from the value of phase noise $\mathcal{L}(\Delta\omega)$ at an offset frequency of $\Delta\omega$ and is given by

$$D = \frac{\mathcal{L}(\Delta\omega) \cdot (\Delta\omega)^2}{2}. \tag{6}$$

Fig. 7 plots the simulated phase noise of the VCO during its integration phase. Phase diffusion constant is evaluated at the corner frequency. For the integration phase, the VCO has a phase noise of -82.2 dBc/Hz at 0.22-MHz offset corresponding to $D_1 = 5.5e3$. For the sampling phase, the VCO has a phase noise of -84.3 dBc/Hz at 0.37-MHz offset corresponding to $D_2 = 9.9e3$. For VCO gain of $G_{\text{vco}} = 97.8$, the input referred thermal noise of VCO is calculated to be 58.1 μV.

The VCO thermal noise is filtered by $G_{\text{vco}}[1 - (1 - a)z^{-1}]/G_d$ before appearing at the output. For matched interstage gain, the noise power at the ADC output due to VCO thermal noise can be written as

$$\overline{n_{\text{vco},th}^2} = \frac{\overline{n_4^2}}{a^2} \cdot \frac{2}{f_s} \int_0^{f_b} \left|1 - (1-a)e^{-j2\pi f/f_s}\right|^2 df \tag{7}$$

where f_b is the signal bandwidth and given by $f_s/2/\text{OSR}$. For large OSR, the above equation can be approximated as

$$\overline{n_{\text{vco},th}^2} = \frac{2}{a^2} \cdot \overline{n_4^2} \cdot \left[\frac{a^2}{2\text{OSR}} + \frac{(1-a)\pi^2}{12(\text{OSR})^3}\right]. \tag{8}$$

For OSR of 40, the in-band VCO thermal noise appearing at the ADC output is 9.2 μV.

The N-stage VCO quantizes the phase interval $[0, 2\pi]$ into $2N$ levels. VCO quantization error is shaped by $[1-z^{-1}][1-(1-a)z^{-1}]/G_d$ at the ADC output and can be written as

$$\overline{n_{\text{vco},q}^2} = \frac{2}{12}\left(\frac{2\pi}{2N}\right)^2 \cdot \frac{2}{f_s} \int_0^{f_b} \left|1 - (1-a)e^{-j2\pi f/f_s}\right|^2 \times \int_0^{f_b} \left|1 - e^{-j2\pi f/f_s}\right|^2 df. \tag{9}$$

For large OSR, the above equation can be approximated as

$$\overline{n_{\text{vco},q}^2} = \frac{1}{3}\left(\frac{\pi}{N}\right)^2 \left[\frac{\pi^2 a^2}{18(\text{OSR})^3} + \frac{(1-a)\pi^4}{10(\text{OSR})^5}\right]. \tag{10}$$

For 7-stage VCO and OSR of 40, in-band quantization noise from VCO appearing at the ADC output is 5 μV. Thus, the total noise power at the ADC output is 27 μV for an OSR of 40. Assuming a 2-V differential peak-to-peak sinusoidal input, the ADC SNR is 88.4 dB. Fig. 8 plots integrated noise from the different sources as a function of ADC bandwidth. At low-bandwidth and large OSR, the in-band noise is set by

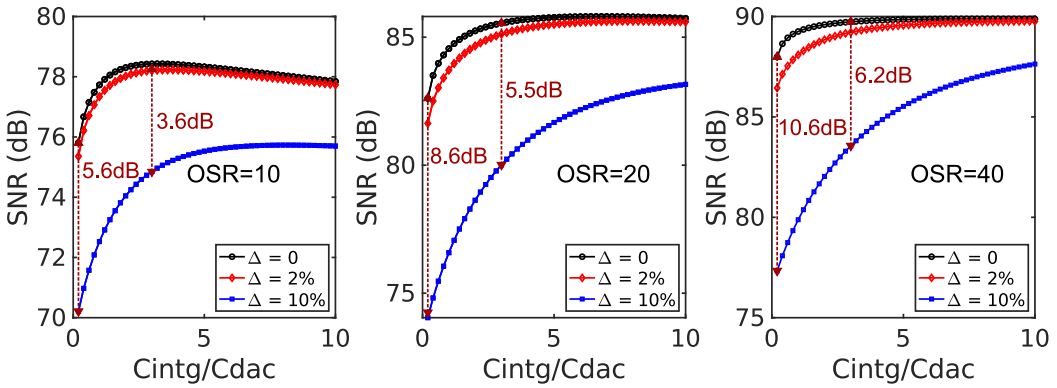


FIGURE 10. Simulated SNR versus the ratio of integrating and sampling capacitors in the NS-SAR for different OSR values and interstage gain errors.

sampling noise from the NS-SAR while VCO quantization error dominates the ADC noise for OSR less than 18.

3) EFFECT OF INTERSTAGE GAIN ERROR

In the presence of interstage gain error and expressing $G_{\text{vco}}/G_d = (1+\Delta)/a$, quantization noise from the NS-SAR and comparator noise appears at the ADC output after being filtered by

$$H_{q,err} = \frac{1-(1-a)z^{-1}}{1+az^{-1}} \cdot \Delta \tag{11}$$

while the kT/C noise from the NS-SAR passive integrator appears at the ADC output after being filtered by

$$H_{n2,err} = \frac{1}{1+az^{-1}}\left[\frac{z^{-1}}{a} + \left(1-(1-a)z^{-1}\right)\frac{1+\Delta}{a}\right]. \tag{12}$$

For a 10% error in interstage gain, the SNR drops to 83.4 dB at OSR of 40 and the integrated noise from the different sources are plotted as a function of ADC bandwidth in Fig. 9. As is expected, in the presence of interstage gain error, the ADC in-band noise is limited by the quantization error from the NS-SAR stage. Fig. 10 plots the simulated ADC SNR for different interstage gain errors at OSR = 10, 20, and 40 and for different ratios of $C_{intg}/C_{dac} = (1-a)/a$. While SNR reduces expectedly as the interstage gain error increases, the reduction in SNR from perfectly matched interstage gain case is less for higher values of C_{intg}/C_{dac}. This is due to more aggressive noise-shaping in the NS-SAR stage as C_{intg}/C_{dac} increases. The drop in SNR due to interstage gain error reduces more quickly with C_{intg}/C_{dac} for smaller values of Δ. Since, gain calibration is used in this work, the choice of $C_{intg}/C_{dac} = 3$ results in an SNR close to the ideal case without any interstage gain error and limits the area consumption by the integration capacitor.

E. ADC CALIBRATION

Fig. 11 shows the proposed calibration method that employs a combination of foreground and background techniques. The foreground calibration runs once at chip startup to extract the interstage gain, and the background calibration keeps running during normal operation to track the interstage gain with changes in voltage/temperature. During foreground calibration, the ADC differential input is set to 0, and the NS-SAR output is dominated by its high-pass-shaped quantization error due to low resolution (5-bit) of the NS-SAR, while the VCO output is dominated by the high-pass-shaped quantization error from NS-SAR stage scaled by interstage gain. The variance of SAR output can be written as

$$\begin{aligned}\sigma^2(d_{\text{sar}}) &= \sigma^2\Big(\{1-(1-a)z^{-1}\}Q_1\Big) + \sigma^2(n_1) \\ &\quad + \sigma^2\Big(\{1-(1-a)z^{-1}\}n_3\Big) + \sigma^2(n_2)/a^2 \\ &\approx \sigma^2\Big(\{1-(1-a)z^{-1}\}Q_1\Big)\end{aligned} \tag{13}$$

where the in-band quantization noise power of SAR stage dominates the thermal noise sources. Similarly, variance of VCO output after passing through $[1-(1-a)z^{-1}]$ filter, $d_2 = [1-(1-a)z^{-1}]d_{\text{vco}}$, can be written as

$$\sigma^2(d_2) \approx [G_{\text{vco}}a]^2\sigma^2\Big(\{1-(1-a)z^{-1}\}Q_1\Big). \tag{14}$$

Thus, ratio of variance of filtered VCO output to variance of NS-SAR output gives the square of the interstage gain. The NS-SAR NTF zero location is extracted in the foreground using Nelder–Mead optimization. Since the NS-SAR NTF zero is set by ratio of capacitors, background calibration is not required for tracking its location. During background calibration, the ADC operates normally and the 2π-crossing points of the differential VCOs are recorded by counters that operate at rising edges of 1 inverter from each VCO. The counter outputs are differentiated and added together, and temporal average of the sum represents the free-running frequency of the VCOs. Variations in PVT are captured in the temporal average, and the interstage gain is updated in the background by multiplying the interstage gain calculated using foreground calibration with fractional change in VCO frequency as shown in Fig. 11.

While the proposed calibration technique can track interstage gain, the calibration technique is limited by G_{vco} mismatches between the two VCOs as well as overflow in the VCOs. If there is no mismatch between the VCOs and no overflow, the accuracy of interstage gain tracking is limited by quantization error in recording the VCO frequency using counter. As shown in Fig. 12(a), the interstage gain

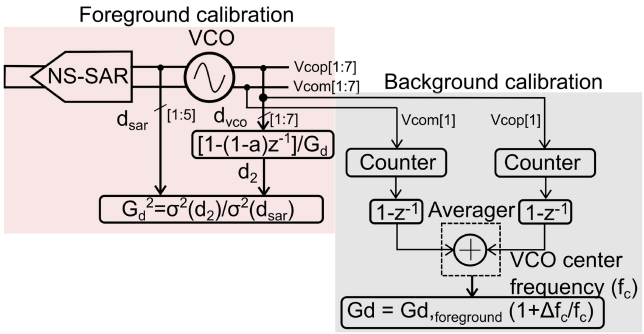
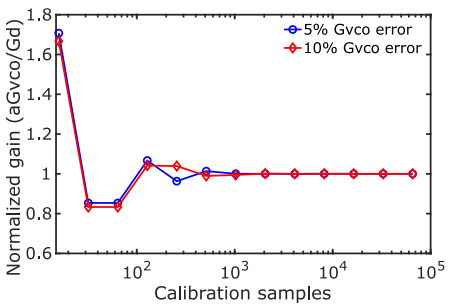
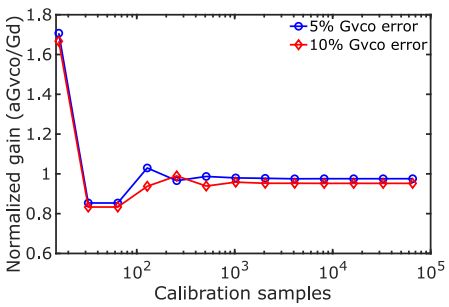


FIGURE 11. Foreground and background calibration techniques to estimate and track interstage gain across PVT.



(a)

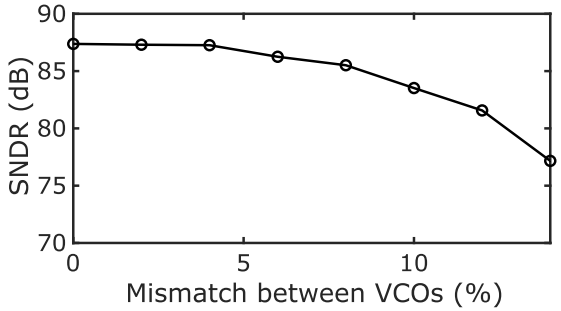


(b)

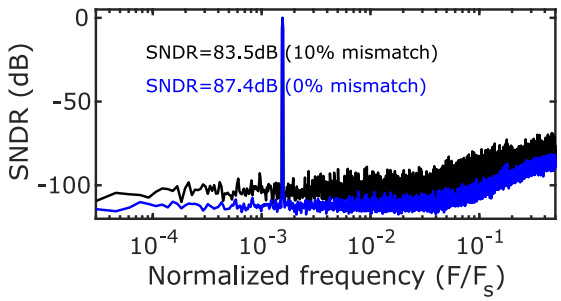
FIGURE 12. Simulated interstage gain extraction convergence for (a) without any mismatch between the VCOs and (b) with 10% mismatch between the VCOs.

tracking converges after 1000 samples. In the presence of 10% mismatch between the two VCOs, the extracted interstage gain does not converge to the correct value as shown in Fig. 12(b). Since the interstage gain error is shaped by the NS-SAR NTF, the ADC can tolerate inaccuracies in interstage gain extraction. Fig. 13(a) plots simulated ADC SNDR as a function of G_{vco} mismatches between the two VCOs for OSR=40. The SNDR remains above 80 dB till up to 12% mismatch between the VCOs which shows the effectiveness of interstage gain error shaping. Fig. 13(b) plots FFTs for without any mismatch between the VCOs and for 10% mismatch between the VCOs. The SNDR drops by 4 dB for 10% mismatch.

Yet another factor that limits the calibration range is overflow in VCO. As long as the phase of both VCO overflows or wraps over the same number of times between



(a)



(b)

FIGURE 13. (a) Simulated SNDR versus mismatch in G_{vco} between the VCOs and (b) FFT plot for no mismatch and 10% G_{vco} mismatch between the VCOs.

any two sampling instants, no error is introduced in the VCO quantization step, and the proposed calibration technique can track interstage gain. Since VCO performs modulo integration, the center frequency F_{vco} can be set to $0.5kf_s$, $k \in [0, 1, 2, \ldots]$ to maximize instantaneous frequency swing without causing overflow [18] which improves energy efficiency of the VCO stage. While the VCO center frequency should ideally be set to $0.5f_s$ to reduce power and noise, it also reduces G_{vco} since VCO center frequency and tuning gain are coupled together by transconductance of the tail current source. A low G_{vco} in turn reduces the resolution of the VCO stage and ADC energy efficiency. Fig. 14 plots ADC SNDR versus normalized VCO center frequency for behavioral model and measurement results at OSR=9 which show good agreement. Local peaks in SNDR for VCO center frequency around $F_{\text{vco}} = kf_s$ correspond to stable regions without overflow. At low center frequencies, G_{vco} is also reduced which accounts for wider stable regions with the widest around $F_{\text{vco}} = 0.5f_s$ and narrowest around $F_{\text{vco}} = 2.5f_s$. The SNDR is lower around $F_{\text{vco}} = 0.5f_s$ since G_{vco} is low which reduces SQNR of the VCO. Conversely, around $F_{\text{vco}} = 2.5f_s$, SNDR is limited by increased thermal noise. The drops in SNDR around these local maxima are due to overflow in the VCOs which results in inaccurate phase count from the VCO stage and corrupts the VCO outputs. The measured SNDR is slightly lower with wider unstable regions due to mismatch between the two VCOs which have different center frequencies and thus have a narrower span of instantaneous frequencies without causing overflow.

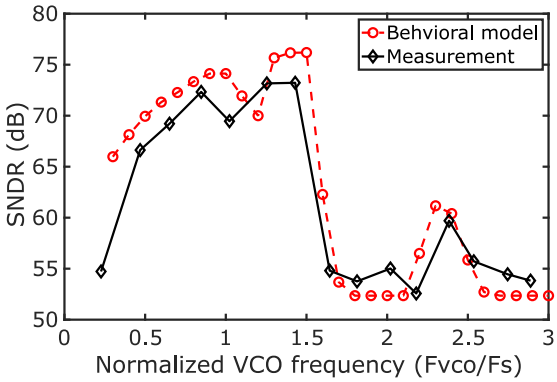


FIGURE 14. Simulated and measured ADC SNDR as a function of normalized VCO center frequency for OSR=9.

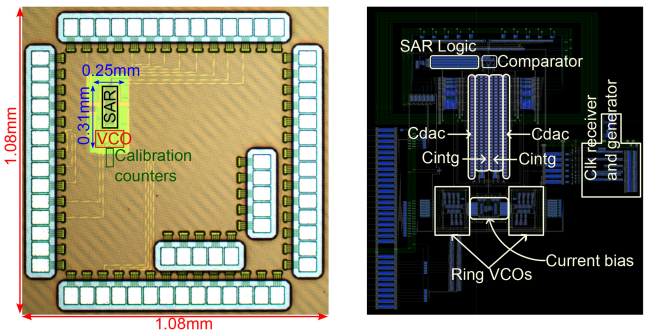


FIGURE 15. Die microphotograph and layout of the ADC.

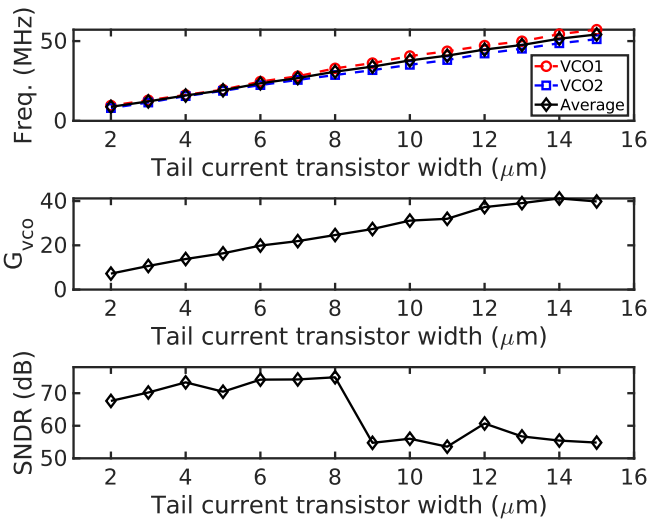


FIGURE 16. Measured VCO frequency, tuning gain, and ADC SNDR at OSR=9 versus tail current transistor width.

III. MEASUREMENT RESULTS

The ADC is fabricated in 65-nm CMOS process and Fig. 15 shows the die photograph and layout. The ADC consumes 120 μW at 18.75-MHz operating frequency. The NS-SAR consumes 74.4 μW from 1.2-V supply while the VCO and background calibration circuit consumes 45.6 μW from 0.95-V supply.

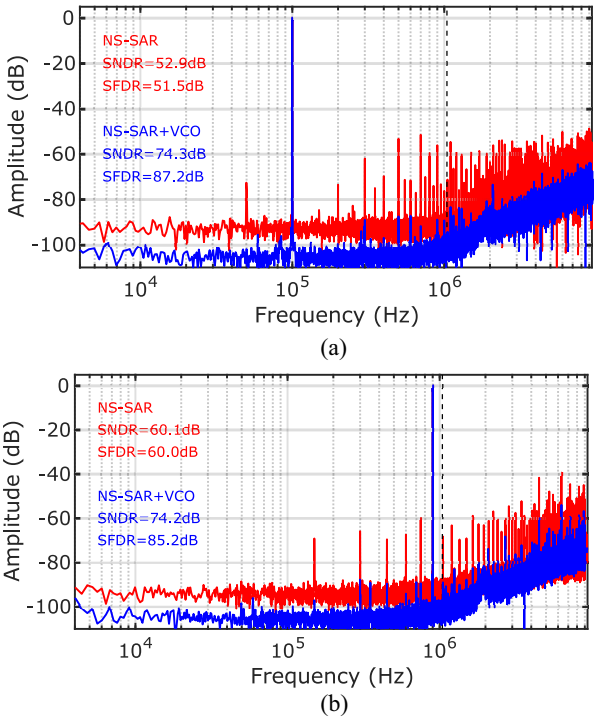


FIGURE 17. Measured FFT with 2.2-V pk–pk sinusoidal input at (a) 100 kHz and (b) 1 MHz input frequencies.

Fig. 16(a) plots the measured center frequencies of the two VCOs and their average as a function of width of the pMOS tail current transistor biasing the VCOs. The transistor width is digitally tuned using a 4-bit control word in steps of 1 μm. The average center frequency varies from 4.25 to 51.2 MHz with the tail current transistor width. The two VCOs have 11% mismatch between their tuning gains. Fig. 16(b) plots the average G_{vco} of the two VCOs while Fig. 16(c) plots ADC SNDR at OSR=9 as a function of tail current transistor width. The tail current transistor width is set at 7 μm for the measurements during foreground calibration which corresponds to average VCO center frequency of 26.8 MHz$= 1.4f_s$ and $G_{\text{vco}} = 24.6$. The measured G_{vco} is approximately 4$\times$ smaller than the schematic simulated value which is likely due to increased parasitic after layout and fabrication, and reduces the measured SNDR compared to simulated SNDR. The drop in SNDR beyond 10-μm width of tail current source is due to overflow in the VCOs. Fig. 17(a) and (b) shows the measured FFT of the test-chip with 2.2-V differential peak-to-peak sinusoidal inputs at input frequencies of 100 kHz and 1 MHz, respectively. SNDR and SFDR are reported for an OSR of 9 which corresponds to input bandwidth of 1.04 MHz. The VCO stage suppresses quantization error tones from NS-SAR by $>$ 35 dB, reduces in-band noise floor by $>$ 25 dB, and improves SFDR by 8 dB compared to [16].

Fig. 18(a) shows the measured SNDR versus input amplitude for OSR of 9. The ADC has a measured dynamic range of 76 dB. Fig. 18(b) plots Walden and Schreier FoM versus OSR. The best Walden FoM of 13.2 fJ/step is achieved at

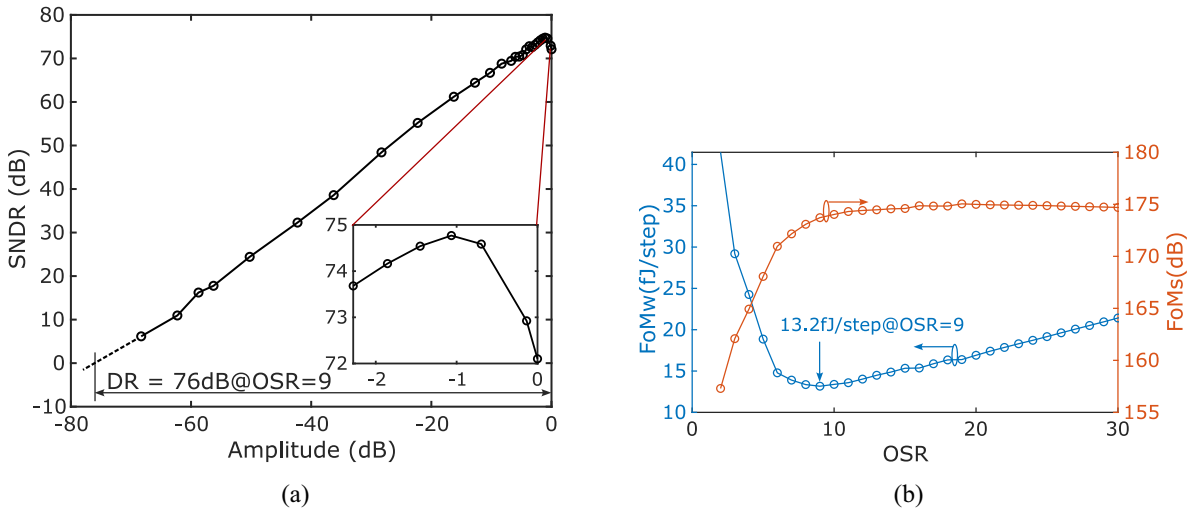


FIGURE 18. Measured (a) dynamic range of the ADC at OSR=9 and (b) Walden and Schreier FoM versus OSR.

TABLE 1. Comparison with state-of-the-art NS-SAR ADCs.

	This work		JSSC' 2021 [16]	ISSCC' 2020 [12]	ISSCC' 2021 [13]	VLSI' 2022 [19]	VLSI' 2022 [20]	ESSCIRC' 2021 [21]	CICC' 2019 [3]
Process	**65nm**		65nm	40nm	40nm	65nm	65nm	65nm	65nm
Area (mm^2)	**0.08**		0.04	0.06	0.09	0.13	0.03	0.04	0.08
Fs (MHz)	**19**		24	2	5	0.2	2	1	80
Supply (V)	**1.2/0.95**		1.1/1	1.1	1.1	1	1	1.2	0.9/2.1
SAR resolution	**5b**		5b	14b	13b	7b	12b	10b	3+7b
Sampling cap	**1.1pF**		1.1pF	36pF	16pF	–	4pF	2pF	1.6pF
$\Delta\Sigma$-order	**2**		2	1	4	3	2	2	2
PVT-robust	**Yes**		No	Yes	Yes	–	No	No	Yes
Power (μW)	**120**		160	67.4	340	5.2	13.5	7.3	870
BW (kHz)	**1040**	**235**	1100	40	250	10	62.5	31.25	2000
OSR	**9**	**40**	11	25	10	10	16	16	20
SNDR (dB)	**74.3**	**82.3**	71.5	90.5	93.3	80.7	77.3	80	73.8
FoM_W(fJ/step)	**13.2**	**23.2**	23.3	29.7	18.1	28.5	18	14.3	52.8
FoM_S(dB)	**173.7**	**175.2**	169.9	178.2	182	173.5	174	176.3	167.4

on OSR of 9. At small OSR values, the ADC SNDR is limited by second-order quantization noise from the VCO stage, while the ADC SNDR is limited by kT/C noise from the SAR stage at large OSR values. The Schreier FoM is limited by quantization noise from VCO stage at small OSR values and flattens out for large OSR values in the kT/C noise limited regime.

Fig. 19(a) and (b) shows SNDR as a function of input frequency and SNDR for multiple test-chips at OSR of 9, respectively. Fig. 19(c) and (d) shows SNDR variation with supply voltage and temperature with 100-kHz input frequency and OSR of 9, respectively. Reduction in supply voltage reduces ADC SNDR, but background calibration improves SNDR by 11 dB at 15% reduction in supply voltage. Background calibration also improves SNDR by 15 dB in the temperature range from 40 °C to 70 °C. Table 1 summarizes the performance of the test-chip and compares with state-of-the-art. The proposed ADC achieves the best Walden FoM among passive NS-SAR ADCs in similar process and needs only a 5-bit SAR with 1.1-pF sampling capacitor compared to 4–36 pF needed by state-of-the-art NS-SAR to achieve high ENOB at low OSR. Thanks to the pipelined architecture, the proposed ADC has higher SNDR and 2× better energy efficiency than [16].

IV. CONCLUSION

This work has presented a pipelined NS-SAR+VCO ADC that significantly relaxes the challenge of driving large sampling capacitance while improving suppression of in-band quantization noise. Thanks to the pipelined architecture, the proposed ADC achieves the best energy efficiency among high-resolution passive NS-SAR ADCs.

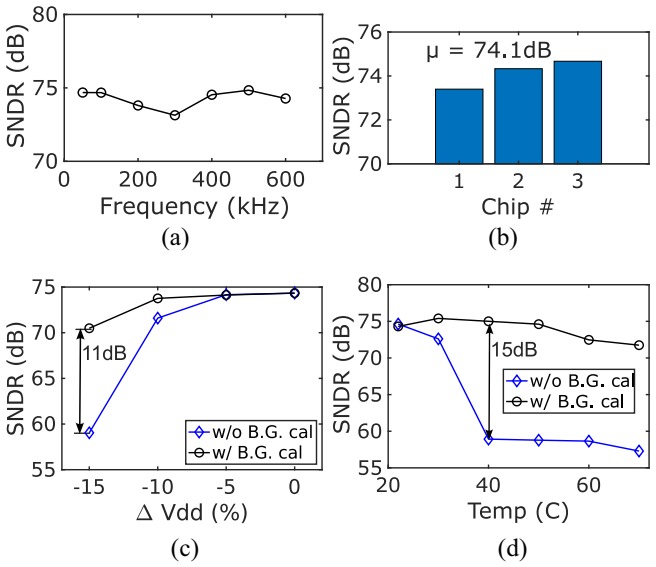


FIGURE 19. Measured SNDR (a) versus input frequency. (b) for three test-chips. (c) versus supply voltage with and without calibration. (d) versus temperature with and without calibration.

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