An 8-bit Split CDAC-Based Noise-Shaping SAR ADC in 180 nm CMOS for Power Efficient Digitization of Sensor Signals

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***Abstract*— Noise shaping (NS) successive approximation register (SAR) analog-to-digital converters (ADCs) can achieve high resolution with low power consumption without the need to incorporate power-hungry transconductance amplifiers. An improved NS architecture is proposed that takes only one extra clock cycle for NS and achieves a first-order NS with a zero at 0.9 using an 8-bit split capacitor digital-to-analog converter (DAC) and passive capacitors for integration. The proposed architecture is implemented in 180 nm 1P6M CMOS process and achieves an signal-to-noise+distortion ratio (SNDR) of 69 dB with an effective-number-of-bits (ENOBs) of 11.16 occupying an active area of 0.07 mm^2.**

***Index Terms*— Analog-to-digital converter (ADC), noise shaping (NS), successive approximation register (SAR).**

I. Introduction

THE demand for high-resolution analog-to-digital converters (ADCs) is increasing in applications like biomedical, instrumentation, and communication systems. Successive approximation register (SAR) ADCs [1], [2], [3], [4] are widely used in medium-resolution and medium speed applications especially sensor applications. Some works of SAR ADCs in sensors include capacitance measurement [5], SAR temperature-to-digital converter (TDC) [6], and capacitance-to-digital converter (CDC) architecture for capacitive sensors [7]. However, for high-resolution applications, SAR ADCs are limited by thermal noise, capacitor mismatches, and comparator noise. Delta-Sigma ($\Delta\Sigma$) ADCs are preferred for high-resolution applications but they use power-hungry transconductance amplifiers (OTAs) which are not suitable for low-power applications. The noise limitation of SAR ADC and power consumption of $\Delta\Sigma$ ADCs [8], [9], [10], [11] can be mitigated by using noise-shaping SAR ADCs (NS-SAR) [12], [13], [14], [15], [16], [17] which use oversampling and residue voltage integration to provide NS. NS ADCs push the quantization noise, comparator noise, and DAC mismatches to higher frequencies and uses oversampling to reduce the in-band noise. This approach reduces the effect of variation of these nonidealities of an SAR ADC, achieving high resolution with low power consumption and area [18]. Typical SAR ADCs use $(N + 1)$ bit cycles to digitize N bits, where N is the resolution of the ADC. However, to achieve NS, NS-SAR ADCs require extra clock cycles for residue voltage integration. Earlier works in NS-SAR ADCs used two extra cycles for residue voltage integration [13].

This article proposes an NS-SAR ADC that: 1) does not require op amps for residue voltage integration, i.e., fully passive NS (FPNS); 2) achieves a first-order NS with a zero at 0.9; and 3) requires only one extra clock cycle for NS, thereby achieving higher speed and high-resolution.

This article is organized as follows: Section II gives an overview of NS-SAR ADCs, Section III discusses the proposed NS-SAR, Section IV discusses the effect of various nonidealities on the proposed ADC performance, Section V discusses circuit design details of a few key blocks, Section VI summarizes the measurement results, and Section VII concludes this article.

II. Overview of NS-SAR

Primitive NS techniques use a sample-and-hold circuit along with an integrator after the final DAC residue has been decided by the comparator [12]. The sample-and-hold circuit is used to hold the residue voltage for some clock cycles and then the residue voltage is integrated to provide NS as shown in Fig. 1(a). The sample-and-hold circuit is usually implemented using a capacitor (C_R) and a switch. The capacitor is charged to the residue voltage and then the switch is opened to hold the voltage. The capacitor is then connected to the integrator to provide NS. However, the presence of the integrator prevents the kT/C_R noise of the residue sampling capacitor (C_R) to be shaped. Thus, C_R needs to be sized large enough to reduce the kT/C_R noise. To prevent this, one of the earliest works in NS-SAR ADC proposed by Fredenberg and Flynn in [12] used a cascade of a two-tap finite impulse response (FIR) filter

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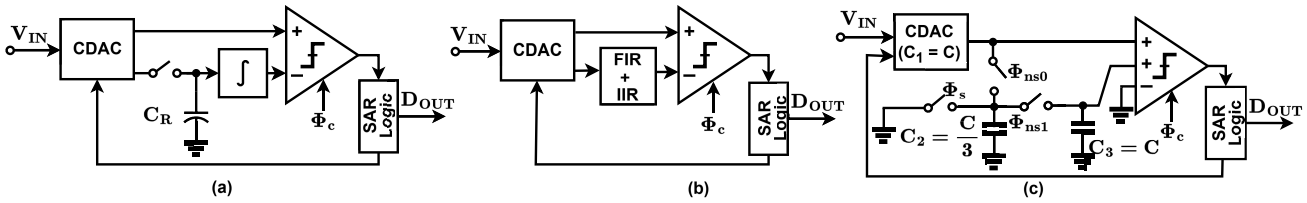

Fig. 1. NS architectures. (a) Sample-and-hold circuit. (b) Cascade of FIR and IIR filter. (c) Passive NS.

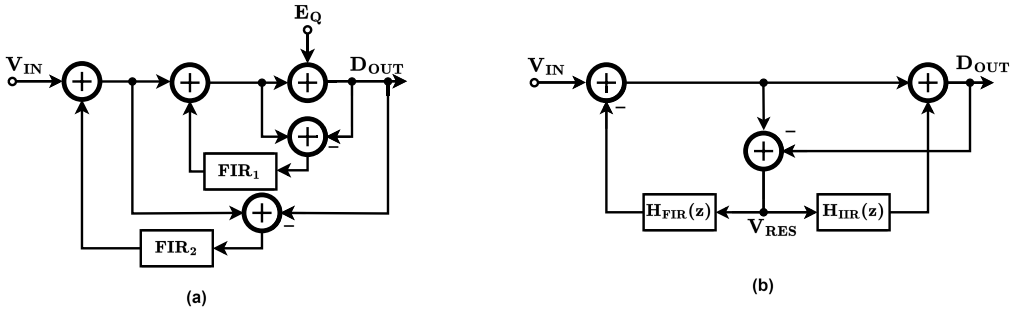

Fig. 2. SFG of NS architectures. (a) Cascade of two second-order NS. (b) EF-CRFF structure.

and an integrator as a loop filter to achieve NS as shown in Fig. 1(b). The residue voltage after all the bits have been obtained is passed through this cascade of filters and then summed with the feed-forward input which is finally given to the comparator. The FIR filter is implemented using a pair of two capacitors and the integrator is an infinite impulse response (IIR) filter implemented using single stage op amp with a feedback capacitor to integrate the output of the FIR filter. An asynchronous clocking is used for sampling and bit cycling of the SAR ADC to reduce power consumption.

The FPNS first introduced in [13] is an op-amp-free topology that shapes the quantization noise using passive integrators as shown in Fig. 1(c). The architecture integrates the residue voltage using only one switch and two capacitors and realizes a noise transfer function (NTF) zero at 0.75. The zero location is given by a ratio of capacitors and is insensitive to process–voltage–temperature (PVT) variations. This NS-SAR ADC requires minimal modification to the conventional SAR ADC architecture and shapes the quantization noise, comparator noise, and DAC noise. When the switch Φ_{ns0} is closed after all the bit cycling has happened, the capacitor C_2 is connected to C_1 and carries a voltage of 0.75 V_{res}. In the next cycle, the switch Φ_{ns0} is opened and Φ_{ns1} is closed. The capacitor C_2 is connected to C_3 in this cycle, allowing charge to be transferred from C_2 to C_3 thereby realizing passive NS. The voltage across C_3, given by V_{int}, is then fed to the comparator. However, passive integration only allows a fraction of the noise voltage to be integrated which is taken care of by considering a gain in the integrated signal path. The capacitors C_1 and C_2 are a fraction of the total capacitive DAC (CDAC) capacitance, so the voltage at the input of the comparator needs to be amplified for effective NS. This is done by sizing the input transistors of the comparator accordingly. This architecture requires two extra clock cycles for integration which is a limitation for high-speed applications.

Fig. 2(a) shows the signal flow graph (SFG) of a cascaded NS-SAR ADC architecture, proposed in [14] which uses a cascade of two second-order NS filters to realize a fourth-order NS with similar power and area as a second-order NS architecture. The overall NTF of the ADC is the product of the two sub-NTFs. Cascading of the NTF provides the flexibility to independently control the zero location of the two sub-NTFs which in turn reduces the sensitivity of the NTF to PVT variation. Each stage of the ADC receives the shaped noise from the previous stage and applies shaping of the current stage before passing it to the next stage. The noise requirement of the first stage is less stringent as it gets shaped by the next stage which reduces power and area.

Fig. 2(b) shows a fourth-order floating-inverter amplifier (FIA)-based integrator with error-feedback and cascaded resonator feedforward structure (EF-CRFF) proposed in [15]. The use of this highly efficient filter has helped them achieve a high dynamic range (DR) with a low oversampling ratio (OSR) of 5. Using low OSR for NS-SAR requires a higher order stable NTF which would give complex zeros in the NTF and improve the signal-to-quantization noise ratio (SQNR). Complex zeros have been generated using CRFF which is robust against process variations as the location of zeros is set by a ratio-based parameter. This work uses a second-order EF and CRFF architecture with noise dominating amplifier being in the EF path resulting in the thermal noise of the CRFF getting shaped by second-order transfer function. The CRFF requires low-loss integrators, hence FIAs are used instead of conventional switched capacitor amplifiers leading to low-input referred noise.

III. Proposed Architecture

The proposed NS-SAR ADC architecture achieves first-order NS using conventional SAR ADC with only one extra clock cycle (Φ_{ns}) and two sampling capacitors to sample

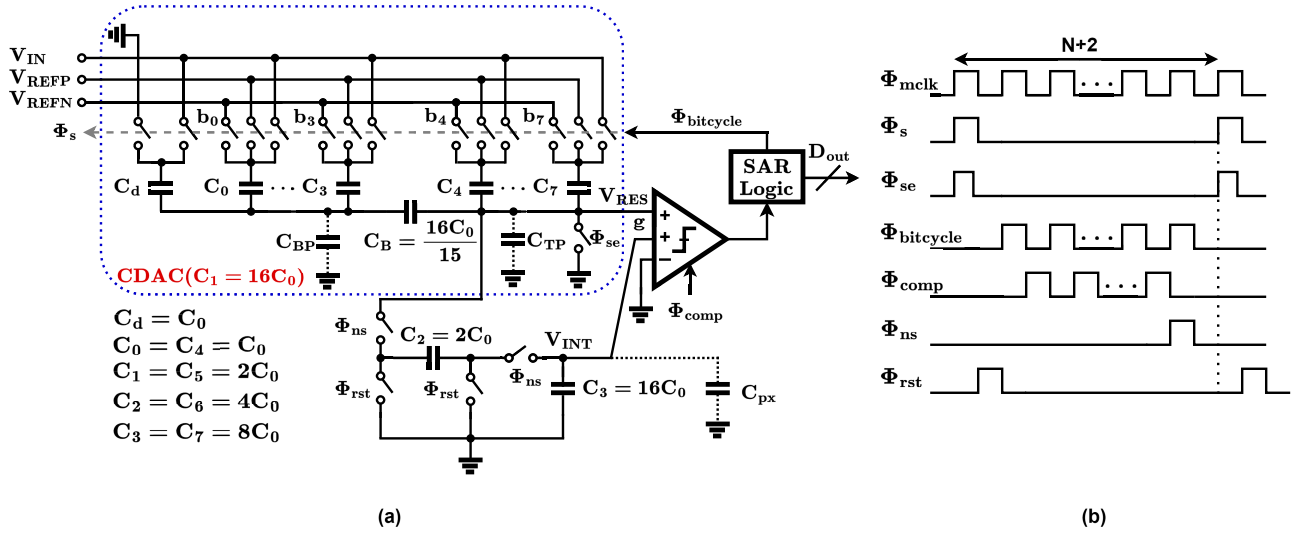

Fig. 3. (a) Architecture. (b) Timing diagram of the proposed NS-SAR ADC.

and integrate the final residue voltage. The architecture is shown in Fig. 3(a) and the timing diagram is shown in Fig. 3(b) for an N-bit NS-SAR ADC. SAR ADC requires $N+1$ cycles for digitizing N-bits. One extra cycle is needed for sampling and integrating the residue voltage after the final bit cycling clock, hence $N+2$ extra cycles are needed for digitizing N bits. The residue voltage after the final bit cycling is passed through the capacitors C_2 and C_3 where C_2 is the attenuation capacitor and C_3 is performing the integration. The voltage on C_3 is then added with the feed-forward residue voltage and given to the comparator. For an 8-bit SAR, the CDAC is implemented using an 8-bit split capacitor DAC whose residue voltage for the kth input sample and nth bit-cycling clock is given in the following equation:

$$V_{\mathrm{RES}}(k,n) = \frac{\zeta}{\gamma}\left[-V_{\mathrm{IN}}(k) + \frac{\beta(k,n)}{\zeta}V_{\mathrm{REF}}\right] \tag{1}$$

where γ, ζ, and β are given the following equations, respectively:

$$\gamma = C_{\mathrm{MSB}} + C_B + C_{\mathrm{TP}} - \frac{C_B^2}{C_{\mathrm{LSB}} + C_B + C_{\mathrm{BP}}} \tag{2}$$

$$\zeta = C_{\mathrm{MSB}} + \frac{C_B C_{\mathrm{LSB}}}{C_{\mathrm{LSB}} + C_B + C_{\mathrm{BP}}} \tag{3}$$

$$\beta(k,n) = \frac{\sum_{i=0}^{3} b_i(k,n)C_i}{C_{\mathrm{LSB}} + C_B + C_{\mathrm{BP}}}C_B + \sum_{i=4}^{7} b_i(k,n)C_i. \tag{4}$$

The LSB capacitor bank, $C_{\mathrm{LSB}} = C_d + C_0 + C_1 + C_2 + C_3$, the MSB capacitor bank, $C_{\mathrm{MSB}} = C_4 + C_5 + C_6 + C_7$, C_d is the dummy capacitor of value C_0 which is the unit capacitance, C_{BP} and C_{TP} are the parasitic capacitances on the left and right side of the bridge capacitor, respectively,[1] and $b_i(k,n)$ for $i = 0$ to 7 are the 8 bits that are being set during bit-cycling, with b_7 being the MSB and b_0 being the LSB. For e.g., for kth sample during the first bit-cycling phase, Φ_{bitcycle}, when $n = 1$ we have $b_7(k,1) = 1$ and $b_i(k,1) = 0$ for $i = 0$ to 6. The comparator then makes a decision with the rising edge of Φ_{comp} based on the residue voltage given by (1). If the comparator output is 1, then the MSB, $D_7 = 1$ else, $D_7 = 0$. In the next bit-cycling phase, $b_7(k,2) = D_7$, $b_6(k,2) = 1$, and $b_i(k,2) = 0$ for $i = 0$ to 5. Based on the comparator decision which happens with the rising edge of Φ_{comp}, D_6 is obtained. This process is repeated until all the bits are resolved, i.e., D_5 to D_0. Thus, the digital output D_{OUT} is given by the following equation:

$$D_{\mathrm{OUT}} = \sum_{i=0}^{7} w_i D_i \tag{5}$$

where w_i are the weights with which the digital outputs are combined. Ideally, $w_i = 2^{i-8}$, however, the capacitor mismatch results in the weights given by the following equation:

$$W_i = \begin{cases} \dfrac{1}{\zeta}\cdot\dfrac{C_i}{C_{\mathrm{LSB}} + C_B + C_{\mathrm{BP}}}\cdot C_B, & \text{for } 0 \le i \le 3 \\ \dfrac{C_i}{\zeta}, & \text{for } 4 \le i \le 7. \end{cases} \tag{6}$$

The sampling and integration of the residue voltage are done in the same clock cycle (Φ_{ns}), thus enhancing the speed of the ADC. The voltage sampled on C_3 (after all the N-bits have been cycled) during the clock cycle Φ_{ns} is given by the following equation:

$$V_{\mathrm{INT}}(k) = \alpha V_{\mathrm{RES}}(k) + (1-\alpha)V_{\mathrm{INT}}(k-1) \tag{7}$$

where $\alpha = C_1C_2/(C_1C_2 + C_2C_3 + C_1C_3)$. The z-domain representation of (7) is given by the following equation:

$$V_{\mathrm{INT}}(z) = \frac{\alpha}{1-(1-\alpha)z^{-1}}V_{\mathrm{RES}}(z). \tag{8}$$

From (8), it can be seen that a fraction of the residue voltage is integrated and added with the feed-forward residue voltage thereby degrading the NS performance. To mitigate this,

[1] C_{BP} is the parasitic capacitance which includes the top-plate parasitics of the LSB capacitor bank and bottom-plate parasitics of the bridge capacitor. C_{TP} is the parasitic capacitance seen by the comparator which includes the top-plate parasitics of the MSB capacitor bank and the bridge capacitor.

a gain, g, is provided to (8) and added with the feed-forward residue voltage. The final residue voltage given to the comparator for each input sample k, is given by the following equation:

$$\begin{aligned} V_{\text{RES},F}(k) &= V_{\text{RES}}(k, N-1) + gV_{\text{INT}}(k-1) \\ &= Q(k) + V_{N,\text{COMP}}(k) \end{aligned} \tag{9}$$

where $Q(k)$ is the quantization noise and $V_{N,\text{COMP}}(k)$ is the comparator noise. Substituting the expression of $V_{\text{RES}}(k,n)$ from (1), the final residue voltage at the input of the comparator is given by the following equation:

$$\begin{aligned} V_{\text{RES},F}(k) = \frac{\zeta}{\gamma}\left[-V_{\text{IN}}(k) + \frac{\beta(k, N-1)}{\zeta}V_{\text{REF}}\right] \\ + gV_{\text{INT}}(k-1). \end{aligned} \tag{10}$$

Taking the z-transform of (9) on both sides, the residue voltage is given by the following equation:

$$V_{\text{RES}}(z) = \text{NTF}(z) \cdot V_N(z) \tag{11}$$

where $\text{NTF}(z)$ and $V_N(z)$ are given by the following equations, respectively.

$$\text{NTF}(z) = \frac{1-(1-\alpha)z^{-1}}{1-[(1-\alpha)-g\alpha]z^{-1}} \tag{12}$$

$$V_N(z) = Q(z) + V_{N,\text{COMP}}(z). \tag{13}$$

The final output of the ADC is given by the following equation:

$$D_{\text{OUT}}(z) = V_{\text{IN}}(z) + V_{\text{RES}}(z). \tag{14}$$

From the z-domain transfer function of (11), it can be seen that the NTF has a zero at $(1-\alpha)$ and a pole at $[(1-\alpha)-g\alpha]$. To obtain a zero at $z = 0.9$, α is chosen to be 0.1, and thus the NS capacitances $C_2 = C_1/8$ and $C_3 = C_1$, where $C_1 = 16C_0$ is the total CDAC capacitance. The value of g is such that the NTF is stable for the above capacitances and the range comes out to be $10 \leq g \leq 18$. A gain, $g = 10$, is chosen for the design, resulting in $D_{\text{OUT}}(z)$ as given by the following equation:

$$D_{\text{OUT}}(z) = V_{\text{IN}}(z) + \frac{1-0.9z^{-1}}{1+0.1z^{-1}}\left[Q(z) + V_{N,\text{COMP}}(z)\right]. \tag{15}$$

Fig. 4 shows the NTF comparison of some of the previous work and the proposed architecture. The NS of previous work is mainly limited by the zero location being far away from $z = 1$. The proposed architecture has a zero location at $z = 0.9$ thereby achieving lower in-band noise.

A. Variation of SNDR With Gain (g) and OSR

The SNDR of an ADC is given by the following equation, where P_{signal} is the power of the signal and P_{ibn} is the power of the in-band noise:

$$\text{SNDR} = P_{\text{signal}} - P_{\text{ibn}}. \tag{16}$$

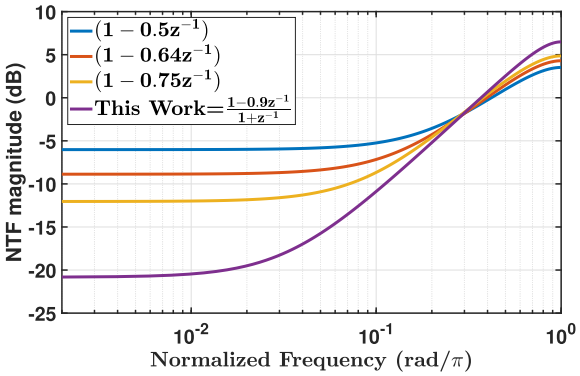

Fig. 4. NTF comparison of previous work in and proposed architecture.

The power of the in-band noise is given by the following equation, where Δ is the quantization-step of the quantizer, also referred to as least significant bit (LSB):

$$P_{\text{ibn}} = \frac{\Delta^2}{12\pi}\int_0^{\frac{\pi}{\text{OSR}}} |\text{NTF}(e^{j\omega})|^2 d\omega. \tag{17}$$

Substituting $z = e^{j\omega}$ in the expression of $\text{NTF}(z)$ in (12), the integrand of (17) is given by the following equation, where $\beta = [g\alpha - (1-\alpha)]$:

$$\left|\text{NTF}(e^{j\omega})\right|^2 = \frac{1-2(1-\alpha)\cos(\omega) + (1-\alpha)^2}{1+2\beta\cos(\omega)+\beta^2}. \tag{18}$$

Substituting $\alpha = 0.1$, which ensures that the zero is at $z = 0.9$, in (18), the power of the in-band noise is given by the following equation which results in P_{ibn} as given in (20), as shown at the bottom of the next page (ref. Appendix):

$$P_{\text{ibn}} = \frac{\Delta^2}{12\pi}\int_0^{\frac{\pi}{\text{OSR}}} \frac{(180\cos(\omega) - 181)d\omega}{(180-20g)\cos(\omega) - g(g-18) - 181}. \tag{19}$$

As mentioned earlier,[2] $g = 10$ is the minimum value of g that ensures stability of the NTF. Substituting $g = 10$ in (20) the P_{ibn} is given by the following equation:

$$P_{\text{ibn}} = \frac{\Delta^2}{12\pi}\left[\frac{2180}{99}\tan^{-1}\left(\frac{9\tan\left(\frac{\pi}{2\text{OSR}}\right)}{11}\right) - \frac{9\pi}{\text{OSR}}\right]. \tag{21}$$

Substituting (20) in (16), the SNDR variation with gain, g, for an OSR of 32 is obtained and shown in Fig. 5. The SNDR increases from 84.70 to 89.44 dB for an OSR of 32 when the gain, g, increases from 10 to 18. Circuit-level simulations also show a similar trend for SNDR, i.e., SNDR increase from 84.56 dB to 88.75 dB when the gain is increased from 10 to 18 for an OSR of 32.

The variation of SNDR with both gain and OSR is shown in Fig. 6.

From (21), it can be seen that for every doubling of the OSR, the SNDR increases by 8 dB as shown in Fig. 7, where the SNDR increases from 52.46 to 90.47 dB when the OSR is increased from 1 to 32 for a gain of 10.

[2]A larger value of g would result in a bigger and higher power design as discussed in Section V.

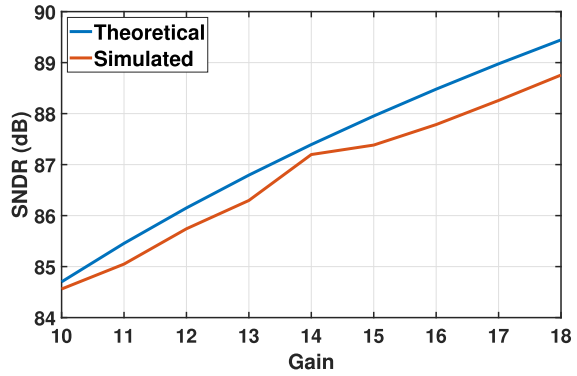

Fig. 5. Variation of SNDR with gain for and OSR of 32 (theoretical is (16) with P_{ibn} as per (20) and simulated is circuit level simulation).

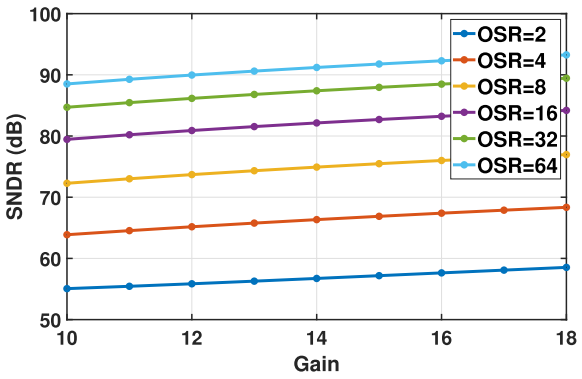

Fig. 6. Variation of SNDR with gain and OSR (theoretical).

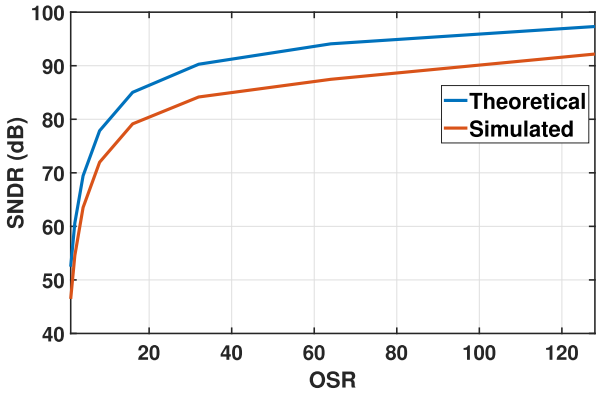

Fig. 7. Variation of SNDR with OSR.

IV. Analysis of Various Nonidealities

In this section, the effect of various nonidealities like thermal noise, capacitor mismatch, preamplifier gain, and parasitic capacitance on the performance of the proposed FPNS-SAR ADC is discussed.

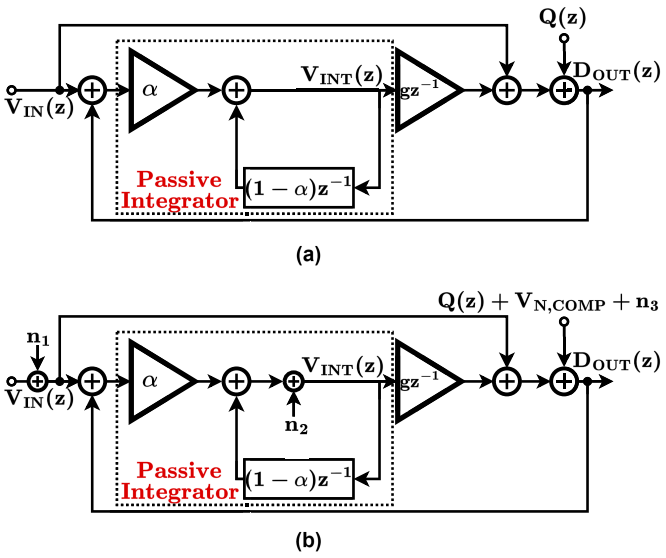

Fig. 8. (a) SFG of the proposed NS-SAR ADC. (b) SFG with noise due to nonideal effects of the proposed NS-SAR ADC.

A. Noise Analysis

The noise analysis of the proposed architecture is done by considering the noise sources in the ADC. Two noise sources are considered, the input sampling noise ($n_1 = kT/16C_0$) which is directly added to the input, and the noise (n_2) generated due to the sampling of the residue voltage on C_3 given by $n_2 = \alpha kT/C_3$, where $\alpha = 0.1$. The signal flow diagram (SFD) of the proposed architecture is shown in Fig. 8(a) where the V_{RES} is passed through the passive integrator and then added with the input to give the final digitized output. The noise due to the nonideal effects of the proposed architecture is shown in Fig. 8(b). The sampling noise n_2 is stored in C_3 during the clock cycle Φ_{ns}, and for a zero at $z = 0.9$, $n_2 = 0.1n_1$. The quantization noise, comparator noise, and CDAC noise (n_3) are shaped by the NTF and given by the following equation:

$$D_{\text{OUT}} = V_{\text{IN}} + n_1 + gz^{-1}n_2 + \frac{1-(1-\alpha)z^{-1}}{1+[g\alpha-(1-\alpha)]z^{-1}} \times \left[Q(z) + V_{N,\text{COMP}}(z) + n_3\right]. \quad (22)$$

From (22), n_1 and n_2 are directly added to the output and hence should be minimized by proper sizing of transistors and capacitors while designing. To reduce this noise, C_1 and C_3 are chosen to be large enough with $C_1 = C_3 = 16C_0$.

B. Effect of Capacitance Mismatch

One of the nonidealities in ADCs is mismatches in the CDAC capacitors which changes the weights given by (6)

$$P_{\text{ibn}} = \frac{\Delta^2}{12\pi}\left[\frac{g(18g+38)\tan^{-1}\left(\frac{\sqrt{g^2-38g+361}}{\sqrt{g^2+2g+1}}\tan\left(\frac{\pi}{2\text{OSR}}\right)\right)}{(g-9)\sqrt{g^2-38g+361}\sqrt{g^2+2g+1}} - \frac{9\pi}{(g-9)\text{OSR}}\right] \quad (20)$$

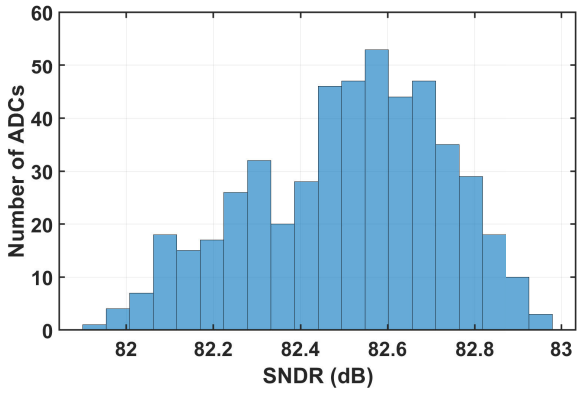

Fig. 9. Histogram of SNDR with 3σ CDAC capacitor mismatch of 0.4%.

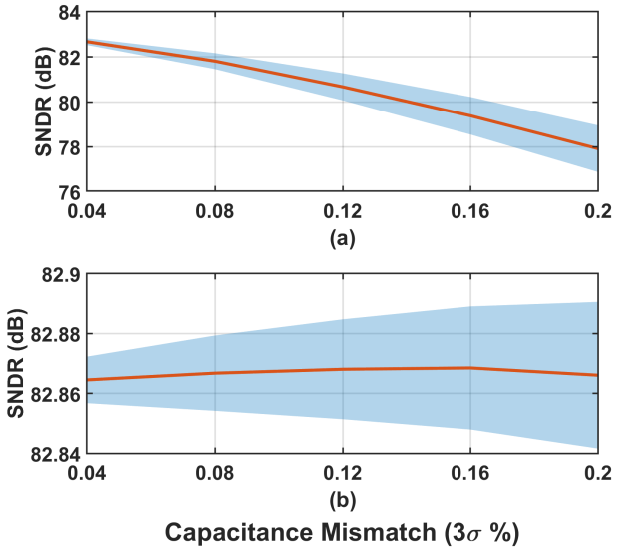

Fig. 10. Mean and standard deviation of SNDR with mismatch in (a) CDAC capacitors and (b) NS capacitors. (The solid line shows the mean of SNDR and the blue shade shows the standard deviation of SNDR.)

with which the digital weights are combined as per (5). If the bits of the ADC are combined with binary weights, there is degradation in the SNDR. It can be seen that the SNDR degrades with an increase in the capacitor mismatch and it degrades by almost 1.6 dB for a 3σ variation of 0.4% [ref. Fig. 9]. Degradation of SNDR will also lead to a reduction in the ENOB of the ADC.

The mean and standard deviation of the SNDR for an OSR of 32 for different values of capacitor mismatch in CDAC is shown in Fig. 10(a). The NS capacitors C_1, C_2, and C_3 will also have mismatch among them. The mean and standard deviation of the SNDR with different values of capacitor mismatch in the NS capacitors is shown in Fig. 10(b), which shows that the SNDR of the ADC degrades by only 0.6 dB, a value that can be ignored. The NS capacitors change the amount of voltage being integrated thereby affecting α. As α is a ratio of capacitors, the mismatch therefore has little impact on SNDR.

C. Effect of Gain Variation

The NTF of the proposed architecture is dependent on the gain g which is multiplied by the integrated residue voltage V_{INT}. Variation in the gain g will result in variation in the NS performance of the ADC. The gain g is dependent on the sizing of the input transistors of the comparator [ref. Section V] and can be changed by changing the size of the transistors. The variation in NTF and spectrum of the ADC due to gain variation is shown in Figs. 11 and 12, respectively.

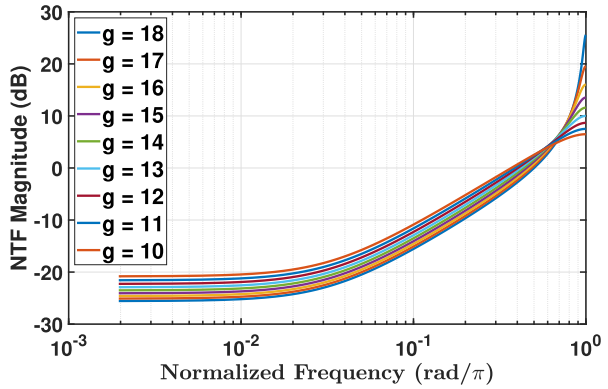

Fig. 11. Effect of gain variation on the NTF of the proposed NS-SAR ADC.

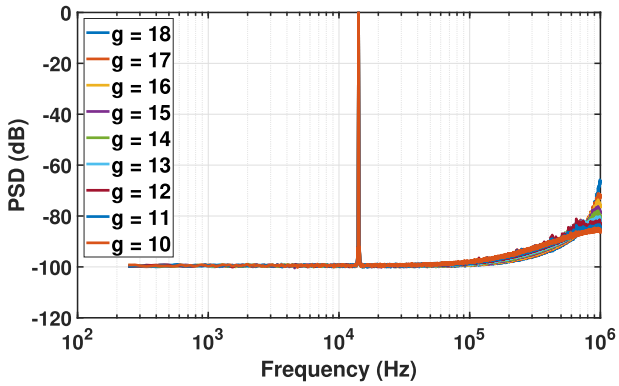

Fig. 12. Effect of gain variation on the spectrum.

As the gain, g, increases, the noise at high frequencies gets amplified while the noise at lower frequencies is attenuated more. A similar effect can be seen on the spectrum as well.[3] It can be seen that the shaping of the noise in the spectrum is similar to the NTF plot. Although a larger gain, g, is preferable, it comes at the cost of additional power and area as the comparator transistors need to have larger size [ref. Section V]. Thus, a trade-off between the power consumption and the NS performance is required while designing the ADC. As the SNDR remains almost the same for different gain settings, a gain $g = 10$ is chosen to minimize design complexity and power consumption.

D. Effect of Parasitic Capacitance

The top-plate and bottom-plate parasitics of the capacitors in the CDAC significantly affect the performance of the NS-SAR especially because the CDAC is a split CDAC. There are two parasitic capacitances considered on either side of the bridge capacitor in the CDAC given by C_{TP} and C_{BP} as shown in Fig. 3. Capacitor C_{TP} appears as a scaling factor in the

[3]To obtain the spectrum with a clean noise-floor fast fourier transform (FFT) averaging of 500 FFTs has been done.

equation of V_{RES} in (1) and thus does not have any effect on the SNDR of the ADC but the SNDR reduces with an increase in C_{BP} as it could lead to weights becoming super-binary as discussed below.

To ensure that the weights are *sub-binary* [19], the condition stated in the following equation must be satisfied:

$$W_K \leq \sum_{i=0}^{K-1} W_i + W_0 \tag{23}$$

where W_i is given by (6).

For the LSB weights (W_0 to W_3) to be *sub-binary*, the condition is given by the following equation:

$$W_K = \frac{1}{\zeta} \cdot \frac{C_K}{C_{\text{LSB}}+C_B+C_{\text{BP}}} \cdot C_B \leq \frac{1}{\zeta} \cdot \frac{\sum_{j=0}^{K-1} C_j + C_0}{C_{\text{LSB}}+C_B+C_{\text{BP}}} C_B$$
$$\Rightarrow C_K \leq \sum_{j=0}^{K-1} C_j + C_0. \tag{24}$$

Similarly, for the MSB weights (W_4 to W_7) to be *sub-binary*, the condition is given by the following equation:

$$W_K \leq \frac{1}{\zeta} \cdot \frac{C_{\text{LSB}}}{C_{\text{LSB}} + C_B + C_{\text{BP}}} C_B + \frac{1}{\zeta} \cdot \sum_{j=4}^{K-1} C_j$$
$$\Rightarrow C_K \leq \frac{C_{\text{LSB}}}{C_{\text{LSB}} + C_B + C_{\text{BP}}} C_B + \sum_{j=4}^{K-1} C_j. \tag{25}$$

The above expression puts a lower bound on the bridge capacitor to ensure that the weights are *sub-binary* in the presence of parasitic capacitance C_{BP} resulting in

$$C_B > \frac{16}{15} C_0 + \frac{C_{\text{BP}}}{15}$$
$$\Rightarrow C_B > C_{B,\text{ideal}} + \frac{C_{\text{BP}}}{15} \tag{26}$$

where $C_{B,\text{ideal}}$ is the ideal bridge capacitor value given by the following equation:

$$C_{B,\text{ideal}} = 16/15 C_0. \tag{27}$$

The condition in (26) ensures that all the weights with which the bits are combined are *sub-binary*.

For an 8-bit ADC with $C_0 = 10$ fF, the values of C_{TP} and C_{BP} are equal to 1.5 and 3.73 fF, respectively. Table I shows the effect of C_B on the weights, where it is clear that the weights are *super-binary* for $C_B = C_{B,\text{ideal}}$ and *sub-binary* for $C_B = 1.05 \cdot C_{B,\text{ideal}}$. The LSB weights are always *sub-binary* as the capacitors are binary weighted, so the condition of (24) is always satisfied. However, the MSB weights will be *sub-binary* if (26) is satisfied as seen in Table I for $C_B = 1.05 \cdot C_{B,\text{ideal}}$.

A parasitic capacitance $C_{\text{BP}} = 5$ fF for $C_0 = 10$ fF and $C_B = 16/15 C_0$ gives rise to harmonics in the output spectrum of the ADC and degrades the SNDR as seen in Fig. 13(a) as the weights become *super-binary*. The weights can be ensured to be *sub-binary* if $C_B > 16/15 C_0 + C_{\text{BP}}/15$. These harmonics can be removed [ref. Fig. 13(b)] by combining the bits of the ADC with exact weights by calibration[4] and ensuring that bridge capacitor satisfies (26). A larger bridge capacitor will reduce the full scale of the signal thereby reducing the SNDR but the drop in SNDR can be ignored for most practical applications.

TABLE I
EFFECT OF C_B ON THE WEIGHTS

Weights	$C_B = C_{B,ideal}$	$C_B = 1.05 \cdot C_{B,ideal}$
W_1	0.0038	0.0039
W_2	0.0076	0.0079
W_3	0.0152	0.0158
W_4	0.0304	0.0317
W_5	0.0626	0.0624
W_6	0.1252	0.1248
W_7	0.2504	0.2496
W_8	0.5008	0.4992

• Gray shaded ⇒ *super-binary*.

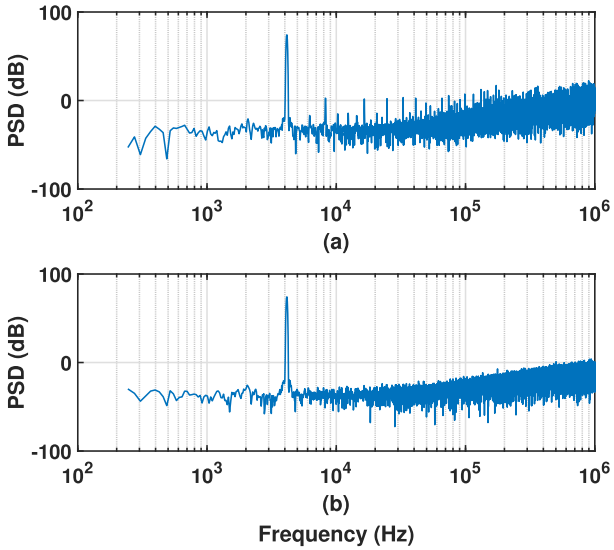

Fig. 13. Effect of parasitic capacitance on the spectrum (a) with *super-binary* weights and (b) with *sub-binary* weights.

V. CIRCUIT DESIGN

The proposed NS-SAR ADC uses an 8-bit CDAC implemented using a two-section split capacitor DAC with a unit capacitance of $C_0 = 50$ fF and a total effective capacitance of $C_1 = 16C_0$ for the sampling network. The LSB capacitor bank consists of four capacitors and a dummy capacitor with a total capacitance of $16C_0$ while the MSB capacitor bank consists of four capacitors with total capacitance of $15C_0$. The bridge capacitor being used between the LSB and MSB capacitor bank has a capacitance that ensures *sub-binary* weights.[5] The capacitors used in the NS filters are $C_2 = C_1/8 = 2C_0$ and $C_3 = C_1 = 16C_0$. The residue voltage is passed through a 4-input preamplifier followed by a 2-input comparator with a

[4]In case the weights are *super-binary*, combining the bits using the calibrated weights, i.e., exact weights, would still result in harmonics and SNDR degradation.

[5]Postlayout extracted simulations were performed to obtain C_B that ensures *sub-binary* weights.

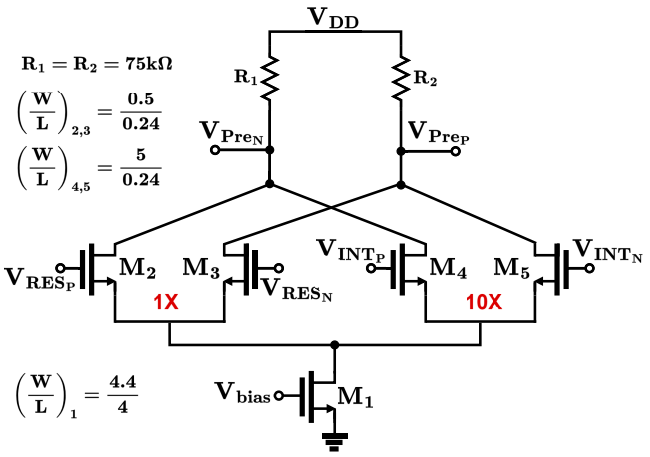

Fig. 14. Design of preamplifier with relative gain.

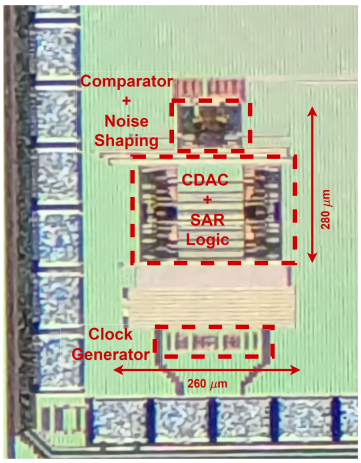

Fig. 15. Die photograph of the proposed ADC.

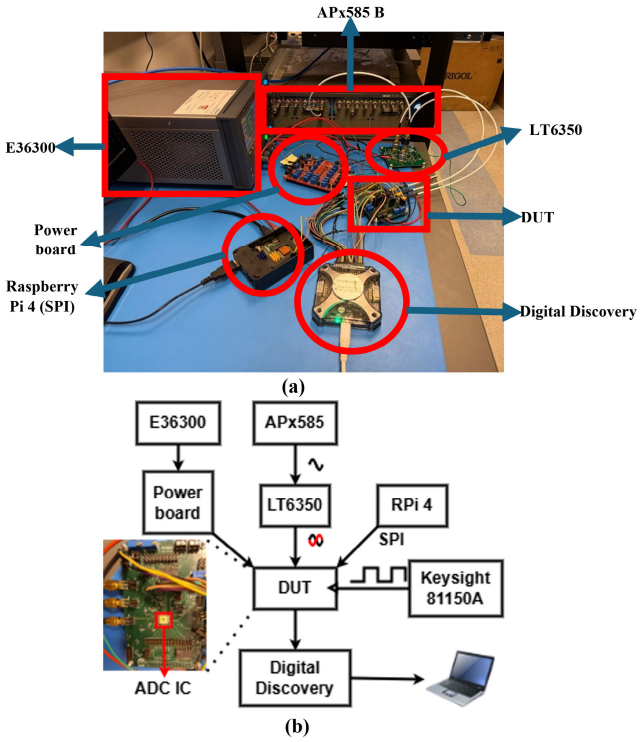

Fig. 16. (a) Test-setup. (b) Block diagram of the test-setup.

relative gain of 10 in the integrated signal path to achieve the desired NS. A gain of 10 is achieved by sizing one of the input transistors ten times compared to the other. Postlayout simulations were carried out to ensure that the weights were *sub-binary* and close to powers of 2 with approximately 10-bit accuracy.

One of the fundamental blocks in the design of the NS-SAR ADC is the comparator which is based on the strong ARM latch topology with fast response time while consuming zero static power and producing full-swing outputs. The comparator design has three parts: a preamplifier, a Strong-ARM latch, and an SR Latch.

1) Preamplifier: The preamplifier is a 4-input differential amplifier whose inputs come from the sampling capacitors array of the ADC and the integrated signal path. The use of a preamplifier before the latch reduces the input size requirement of the latch by a factor of gain squared. So, a gain of 10 dB has a tenfold reduction in the input size of the transistors. The preamplifier is designed using a differential pair of input transistors M_2–M_5 and resistive load R_1–R_2 as shown in Fig. 14. The input common range (ICMR) of the preamplifier is decided from the voltages in the top plate of the capacitors in the CDAC. To achieve a relative gain of 10 in the integrated signal path, the input transistors have been sized ten times compared to the input transistors of the residue path.

2) Strong-ARM Latch: The Strong-ARM latch is a 2-input latch that is used after the preamplifier. The Strong-ARM latch is designed using a differential pair of input transistors with two cross-coupled inverters, a tail transistor, and four switches for precharging [23]. The circuit operation starts by precharging the outputs to V_{DD} and then the input transistors are turned on to provide the output. In the regeneration phase, the equivalent circuit of the cross-coupled inverters gives a natural response of the form $e^{(t/\tau_{reg})}$ where τ_{reg} is the regeneration time constant [24].

3) SR Latch: The Strong-ARM latch produces invalid outputs for half the clock cycle. To avoid incorrect interpretation of comparator voltages by the subsequent stages, the latch is followed by a set-reset (SR) latch which changes its value after the Strong-ARM latch output has settled. The SR latch is designed using a differential pair of input transistors with two cross-coupled inverters in which the input transistors are sized larger than P-channel metal oxide semiconductor (PMOS) transistors of cross-coupled inverters to avoid changing its output with changes in the voltages of the inverters.

VI. Measurement Results

The proposed first-order FPNS architecture has been implemented in the 180-nm 1P6M CMOS process. Fig. 15 shows the die photo of the prototype ADC with an active area of 0.07 mm^2.

Fig. 16(a) shows the test-setup and Fig. 16(b) shows the block diagram of the test-setup. A clean sine wave is generated

TABLE II
COMPARISON OF THE PROPOSED ADC WITH OTHER WORKS

	[13]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]	[33]	[34]	**This Work**
Technology (nm)	130	65	65	65	180	180	180	180	65	130	65	**180**
Order	1	4	3	1	1	1	2	2	3	1	2	**1**
OSR	8	128	5 ≈ 6	16	64	32	8	10	8	32	16	**32**
BW (kHz)	125	24	3760	62.5	0.04	2	0.625	25	625	2	625	**31.25**
Resolution (bits)	10	8	9	10	10	10	7	9	10	10	9	**8**
F_s (MHz)	2	6.14	43	2	0.00512	0.128	0.01	0.5	10	0.128	20	**2**
SNDR (dB)	74	94.10	68.50	77.30	88	78.80	65	73.70	84.80	82.6	79.3	**69**
ENOB (bits)	12	15.34	11.08	12.55	14.33	12.80	10.50	11.95	13.79	13.42	12.88	**11.16**
Power (μW)	61	68	460	13.5	20	74	0.09	16.50	119	40.8	113.02	**110**
Area (mm^2)	0.13	0.02	0.08	0.03	0.28	0.25	0.12	0.087	0.04	0.2	0.354	**0.07**
FoM_s (dB)	167.12	179.58	167.62	173.96	151.01	153.12	163.42	165.50	182	160	176.73	**153.5**

TABLE III
DIFFERENCE OF THE MEASURED SNDR FROM THEORETICAL SNDR FOR FIRST-ORDER NS

	Expression	[27]	[13]	[28]	[29]	[33]	**This Work**
Technology (nm)		65	130	180	180	130	**180**
Resolution (Nbit)		10	10	10	10	10	**8**
OSR		16	8	64	32	32	**32**
$SNDR_{Nbit\text{-}Ny}$ (dB)	6.02Nbit + 1.76	61.96	61.96	61.96	61.96	61.96	**49.92**
$SNDR_{NNS\text{-}OSR}$ (dB)	6.02Nbit + 1.76 + 10 log_{10}OSR	74	71	80.02	77.01	77.01	**64.97**
$SNDR_{NS\text{-}OSR}$ (dB)	6.02Nbit+1.76+xdB	81.6	79.96	115.96	106.96	106.96	**82**
$SNDR_{measured\text{-}OSR}$ (dB)		77.3	74	88	78.8	79.3	**69**

x dB is the improvement in SNDR per doubling of OSR which is dependent on the NTF. For zero at $z = 1$, the SNDR improvement is 9 dB per doubling of OSR.

using APx585 B audio analyzer[6] with a THD of 107 dB. The differential input signals for the ADC is generated using a single-ended to differential ADC driver (LT6350)[7] which converts the single-ended input of low amplitude (900 m$V_{pp,diff}$) from the audio analyzer (to minimize second and third harmonics from the generator) to a low-impedance differential output of 1.8 $V_{pp,diff}$.

The power supply and reference voltages (V_{refp} = 1.35 V and V_{refn} = 0.45 V) of the ADC are externally supplied using Keysight bench-top triple power supply (E36300).[8] The digital control voltages to the chip were given using Raspberry Pi 4[9] and the digital output of the ADC was acquired using Digilent Digital Discovery Kit.[10]

The ADC operates from a supply voltage of 1.8 V and samples at 2 MHz with an OSR of 32 for a bandwidth (BW) of 31 kHz. Fig. 17 shows the spectrum of the ADC for a sine wave input of 11.111 kHz with a peak-to-peak differential amplitude of 1.72 V. The ADC achieves an SNDR of 69 dB with an ENOB of 11.16 bits for an amplitude of 99% of full scale.

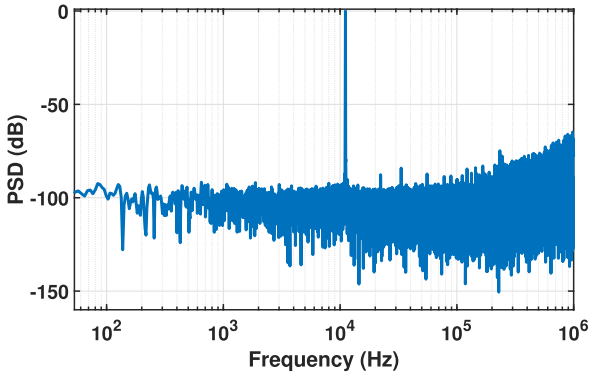

Fig. 17. Spectrum of the ADC for a sine wave input.

Comparison of the proposed work with previous work is summarized in Table II. The ADC has a higher BW, higher sampling frequency of 2 MHz, and smaller area of 0.07 mm^2 when compared to other works in the same technology while consuming a power of ≈110 μW, thus achieving a Schreier FoM of 153.5 dB. Table III shows the difference of the measured SNDR and the theoretical SNDR for first-order NS across various works, both with and without NS. $SNDR_{Nbit\text{-}Ny}$ is the SNDR of the ADC at

[6]https://www.ap.com/analyzers-accessories/apx58x
[7]https://www.analog.com/en/products/lt6350.html
[8]https://www.keysight.com/us/en/products/dc-power-supplies/bench-power-supplies/e36300-series-triple-output-power-supply-80-160w.html
[9]https://www.raspberrypi.com/products/raspberry-pi-4-model-b
[10]https://digilent.com/reference/test-and-measurement/digital-discovery/start?srsltid=AfmBOoofsJ4bosrIwngcqnS6SzU3Fjt-jb8mjgOFiVbIGAsBJxJ7PUT

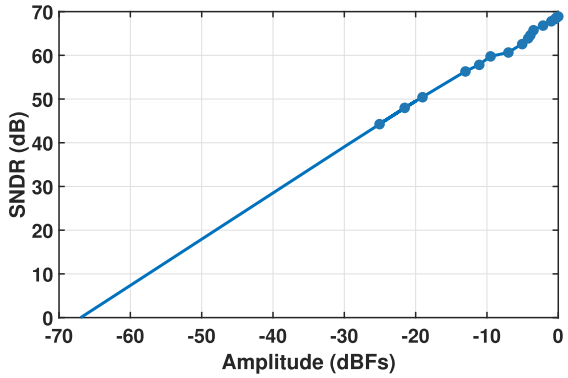

Fig. 18. DR of the proposed NS-SAR ADC.

Nyquist, $\text{SNDR}_{\text{NNS-OSR}}$ is the SNDR of the ADC with no NS at the OSR, $\text{SNDR}_{\text{NS-OSR}}$ is the SNDR of the ADC with NS at the OSR, and $\text{SNDR}_{\text{measured-OSR}}$ is the measured SNDR of the ADC at the OSR. $\text{SNDR}_{\text{NS-OSR}}$ is calculated using the expression 6.02Nbit + 1.76 + x dB where x is the improvement in SNDR per doubling of OSR which is dependent on the NTF. From Table III, it can be seen that NS improves the SNDR by a maximum of 7.98 dB compared to the same ADC without NS for same OSR. Ideally, the SNDR of the ADC with NS for a given NTF and OSR should be higher as shown in $\text{SNDR}_{\text{NS-OSR}}$. The difference between SNDR with and without NS in the proposed work at an OSR of 32 is 4.03 dB, which is consistent with other works. Even with a moderate 4.03 dB improvement in SNDR, NS SAR ADCs are preferred as they minimize the effect of SNDR degradation of the ADC with increasing nonidealities, i.e., increasing capacitor mismatch and increasing comparator noise when compared to SAR ADCs without noise-shaping for the same OSR [18]. The DR of the proposed NS-SAR ADC is shown in Fig. 18. The ADC achieves a DR of 69.5 dB for a differential full scale of 1.8 V_{pp}.

VII. Conclusion

An 8-bit first-order noise-shaping SAR ADC with an improved noise-shaping architecture has been proposed. The effect of various nonidealities on the performance of the ADC has been discussed in this article. It is shown that mismatches in the noise-shaping capacitors have a negligible effect on the SNDR of the ADC. The effect of gain variation on the NTF and spectrum has also been shown. A gain of 10 is chosen for this work to reduce power consumption and area. The ADC achieves an SNDR of 69 dB with an ENOB of 11.16 bits for an amplitude of 99% of full scale. The ADC has a BW of 31.25 kHz, a sampling frequency of 2 MHz, and an area of 0.07 mm^2 while consuming a power of ≈110 μW. The ADC achieves a Schreier FoM of 153.5 dB. The proposed ADC has been compared with other works and has been shown to have a higher BW, higher sampling frequency, and smaller area while consuming a lower power in the same technology node. The proposed ADC has been shown to have a 4.03 dB improvement in SNDR due to NS. The proposed ADC can be used in applications where high resolution and low power consumption are required.

Appendix

The derivation of in-band noise power as a function of gain and OSR is presented which results in (20). Substituting the values of $\alpha = 0.1$, which ensures that the zero is at $z = 0.9$, in (18), we get

$$|\text{NTF}(e^{j\omega})|^2 = -\frac{180\cos(\omega) - 181}{20(g-9)\cos(\omega) + g^2 - 18g + 181}. \tag{A.1}$$

The in-band noise power, P_{ibn}, is given by (17), where the integrand is given by (A.1). The numerator of (A.1) is $(180\cos(\omega) - 181)$ and is denoted by NUM, which is restructured as follows:

$$\text{NUM} = \frac{9}{g-9}\left(20(g-9)\cos(\omega) + g^2 - 18g + 181\right) + \left(-\frac{9\left(g^2 - 18g + 181\right)}{(g-9)} - 181\right). \tag{A.2}$$

Thus, (17) and be written as (A.3), where A and B are given by (A.4) and (A.5), respectively

$$P_{\text{ibn}} = \frac{\Delta^2}{12\pi}\int_0^{\frac{\pi}{\text{OSR}}}(A+B)d\omega \tag{A.3}$$

$$A = \frac{\frac{9\times 20(g-9)\cos(\omega)}{g-9} + g^2 - 18g + 181}{20(g-9)\cos(\omega) + g^2 - 18g + 181} = \frac{9}{g-9} \tag{A.4}$$

$$B = \frac{-\frac{9(g^2-18g+181)}{(g-9)} - 181}{20(g-9)\cos(\omega) + g^2 - 18g + 181}. \tag{A.5}$$

As A is independent of ω, its integral is straightforward. However, obtaining the integral of B requires using certain trigonometric identities to make the integral tractable. Using $\cos(\omega) = (\cos^2(\omega/2) - \sin^2(\omega/2))$, B can be written as follows:

$$B = \frac{\left(-\frac{9(g^2-18g+181)}{(g-9)} - 181\right)\sec^2\left(\frac{\omega}{2}\right)}{\left(g^2 - 38g + 361\right)\tan^2\left(\frac{\omega}{2}\right) + g^2 + 2g + 1}. \tag{A.6}$$

Setting $u = ((g^2 - 38g + 361)^{1/2}/(g^2 + 2g + 1)^{1/2})\tan(\omega/2)$ and $du = ((g^2-38g+361)^{1/2}/2(g^2+2g+1)^{1/2})\sec^2(\omega/2)d\omega$, the indefinite integral $\int(A+B)d\omega$ can be written as follows:

$$X = \frac{9\omega}{g-9} - \frac{2\left(\frac{9(g^2-18g+181)}{(g-9)} - 181\right)}{\sqrt{g^2 - 38g + 361}\sqrt{g^2 + 2g + 1}}\int\frac{1}{u^2+1}du. \tag{A.7}$$

Thus,

$$X = \frac{9\omega}{g-9} - \frac{2\left(\frac{9(g^2-18g+181)}{(g-9)} - 181\right)}{\sqrt{g^2 - 38g + 361}\sqrt{g^2 + 2g + 1}}\tan^{-1}(u)$$

$$\Rightarrow = \frac{9\omega}{g-9} - \frac{g(18g+38)\tan^{-1}\left(\frac{\sqrt{g^2-38g+361}}{\sqrt{g^2+2g+1}}\tan\left(\frac{\omega}{2}\right)\right)}{(g-9)\sqrt{g^2 - 38g + 361}\sqrt{g^2 + 2g + 1}} \tag{A.8}$$

resulting in the in-band noise power, P_{ibn}, as given by (20).

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