Late Breaking Results: Machine Learning Based Reference Ripple Error Suppression in Successive Approximation Register Analog-to-Digital Converters

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ABSTRACT

This work presents a machine learning (ML) technique to suppress reference ripple errors in successive approximation register (SAR) analog-to-digital converter (ADC). Reference voltage ripple due to switching in SAR ADC introduces dynamic error which manifests as spurs in the output spectrum and limits ADC resolution. Conventional techniques to suppress reference ripple require large decoupling capacitor and high-speed reference voltage buffer which consume large area and power. The proposed ML approach uses a supervised technique in which a low-speed 10MHz SAR ADC is used for learning and correcting reference ripple error in a 200MHz SAR ADC. Simulated in 28nm CMOS technology, the proposed ML approach reduces overall ADC power consumption by 4.9x without degrading performance.

KEYWORDS

Machine learning, Analog-to-digital converter, Reference ripple

1 INTRODUCTION

Successive approximation register (SAR) analog-to-digital converter (ADC) is a popular architecture for data conversion due to its high energy-efficiency. At high-speed, performance of SAR ADC is limited by ripples on the reference voltage line that are caused as the digital-to-analog converter (DAC) capacitors are connected or disconnected from the reference voltage line during each conversion step, and manifests as spurs in the ADC output. Conventional techniques try to suppress reference ripple error by connecting large decoupling capacitors to the reference line and using on-chip, high-speed reference buffers that can consume > 10x larger power than the core ADC circuits [1]. Recent works have tried to address this through different techniques such as pre-charged reservoir capacitor [2], dynamic reference regulation [3], charge neutralization [4] and emulating reference ripple with a replica DAC [5]. However, these techniques still need either a large reservoir capacitor, a clean supply voltage or are limited by replica matching.

This work proposes a supervised machine-learning (ML) approach to suppress reference ripple error line in high-speed SAR ADCs as shown in Fig. 1. The proposed technique uses a low-speed SAR ADC to create ground truth and learn ripple induced error in the high-speed SAR ADC biased with the low-speed reference buffer. The error estimated by the ML model is then digitally canceled from the high-speed SAR ADC output. This technique offers the following key benefits: a) power consumption is significantly reduced since high-speed reference buffer and/or large decoupling capacitor is not required; b) accurate knowledge of reference ripple generation is not needed, thus simplifying the circuit design efforts. The proposed techniques are demonstrated by suppressing reference ripple error in a 10-bit, 200MHz asynchronous SAR ADC using a 10MHz, 12-bit SAR ADC to train the ML model.

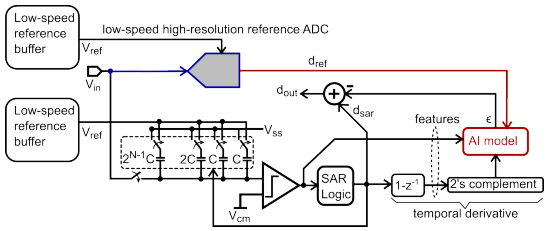

Figure 1: Proposed supervised ML technique to suppress reference ripple in SAR ADC

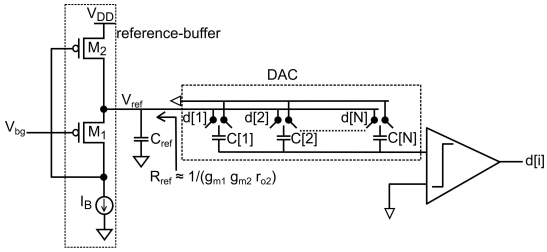

Figure 2: Circuit schematic showing reference buffer driving capacitors in the SAR ADC

2 REFERENCE RIPPLE SUPPRESSION BY ML

2.1 SAR ADC architecture

The SAR ADC architecture used in this work is shown at a high-level in Fig. 1. The 200MHz ADC is an asynchronous 10-bit SAR with 1-bit redundancy and DAC capacitors sized as [$512C_u$ $256C_u$ $128C_u$ $64C_u$ $64C_u$ $32C_u$ $16C_u$ $8C_u$ $4C_u$ $2C_u$ C_u] where C_u is the unit capacitor with value of 0.34fF. The 10MHz reference ADC is a synchronous 12-bit SAR ADC with 1-bit redundancy and DAC capacitors sized as [$2048C_o$ $1024C_o$ $512C_o$ $256C_o$ $128C_o$ $128C_o$ $64C_o$ $32C_o$ $16C_o$ $8C_o$ $4C_o$ $2C_o$ C_o] with the value of C_o as 0.6fF. Both ADCs use bi-directional single-sided switching technique [6]. While the redundant capacitor provides some degree of reference ripple

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error suppression, it is not adequate to fully mitigate the effect of reference ripple as shown in Section 2.3.

Fig. 2 shows schematic of a reference buffer driving the capacitors in SAR DAC. A single-ended schematic is shown for the sake of simplicity even though a fully differential configuration is used for the SAR ADC. A flipped voltage follower (FVF) is used as reference buffer. The FVF accepts a band-gap reference voltage, V_{bg}, as input and outputs the voltage, V_{ref}, that drives the SAR DAC. FVF reduces the output resistance compared to a regular single-transistor voltage follower by gain of common-source amplifier (M_2 in Fig. 2). This ensures that SAR DAC is driven by a very low resistance and thus, capacitors in the DAC can settle quickly.

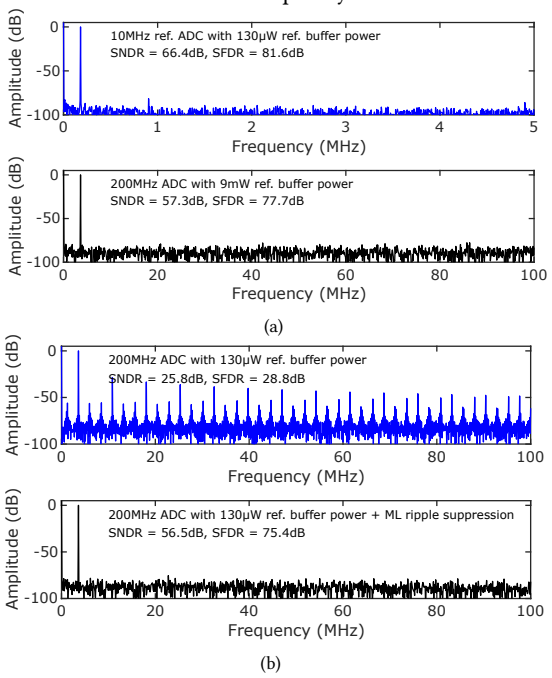

Figure 3: Circuit schematic showing reference buffer driving capacitors in the SAR ADC

2.2 ML for ADC error correction

The key challenges in applying ML to correct errors in ADC are – a) accuracy requirement of error correction, and b) convergence speed. While a 90-95% accuracy of ML algorithms is perfectly acceptable for most applications, ADCs need correction algorithms to have accuracies greater than 99.999% for SNDR> 60dB. However, complex ML models with thousands of trainable parameters cannot be employed to improve accuracy since their power and area consumption will far exceed that of the ADC. The proposed technique uses a circuits-informed approach to extract key features from the ADC output to achieve ML accuracies greater than 99.999%. The ML model uses the current output of the main SAR ADC and its temporal derivative to learn reference ripple error in the main ADC output. All the features used for training the ML model are converted into binary bits which converts all matrix multiplications in the first hidden layer in the ML model to additions and reduces hardware cost. Since reference ripple error is dynamic in nature, the ML training needs to happen continuously in the background. This requires fast convergence of the ML algorithm. The proposed approach uses RMSprop optimizer during backpropagation to update weights of the ML model during training. RMSprop updates learning rate for each model weight adaptively which results in faster convergence than the popular stochastic gradient descent.

2.3 Results

Fig. 3 shows simulation results demonstrating reference ripple suppression using ML. The ML model used is a two-layer neural network - a hidden layer with 10 neurons and tanh activation, and an output layer with 1 neuron that performs linear regression. The ML model is synthesized digitally and consumes 1.1mW power. The 10MHz reference ADC consumes 46μW with 130μW reference buffer for 66.4dB signal-to-noise-and-distortion ratio (SNDR), while the 200MHz main ADC consumes 0.68mW with 9mW reference buffer for 57.3dB SNDR. The SNDR drops to 25.8dB when the 200MHz ADC is biased with 130μW reference buffer. However, the ML model is able to improve SNDR of the 200MHz ADC to 56.5dB with the low-power 130μW reference buffer, thus achieving 4.9x lower power consumption and 4.2x better energy-efficiency (FoM$_w$). The proposed technique achieves better energy efficiency than state-of-the-art SAR ADCs that employ reference ripple error correction as shown in Table 1.

Table 1: Comparison with state-of-the-art

	[7]	[5]	This work	
Process (nm)	65	40	**28**	
Resolution (bit)	11	10	**10**	
Supply (V)	1.2	1.1/1.3	**0.9/1.2**	
Fs (MHz)	100	100	**200**	
Sampling cap (pF)	0.77	1	**0.7**	
Ref. buff. (mW)	0.84	0.31	**0.26**[1]	
Ref. Ripple correction	Ref. Calibration	Replica DAC	**Machine-learning**	
SNDR (dB)	58	57.9	**56.5(with ML)**	**57.3 (w/o ML)**
Power (mW)	2.44	1.4	**2.1(with ML)**[2]	**9.7(w/o ML)**
FoM$_w$(fJ/step)[3]	37.9	26.2	**18.8(with ML)**	**79.1(w/o ML)**

[1]includes power of 2 reference buffer; [2]includes power of ML training and inference; [3]FoM$_w$ = Power/2^{ENOB}/Fs

3 CONCLUSION

This work has demonstrated the potential application of ML into ADC design space and can be extended to digitally correcting other static and dynamic errors in high-performance ADCs.

REFERENCES

[1] Y. Zeng, C.-H. Chan, Y. Zhu, and R. P. Martins, "An Auxiliary-Loop-Enhanced Fast-Transient FVF LDO as Reference Buffer of a SAR ADC," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022, pp. 2660–2664.

[2] M. Liu, A. H. van Roermund, and P. Harpe, "A 10-b 20-MS/s SAR ADC with DAC-compensated discrete-time reference driver," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 417–427, 2018.

[3] J. Lagos, N. Markulić, B. Hershberg, D. Dermit, M. Shrivas, E. Martens, and J. Craninckx, "A 10.1-ENOB, 6.2-fJ/conv.-step, 500-MS/s, ringamp-based pipelined-SAR ADC With background calibration and dynamic reference regulation in 16-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 4, pp. 1112–1124, 2022.

[4] Y.-Z. Lin, C.-H. Tsai, S.-C. Tsou, and C.-H. Lu, "A 8.2-mW 10-b 1.6-GS/s 4× TI SAR ADC with fast reference charge neutralization and background timing-skew calibration in 16-nm CMOS," in *IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2016, pp. 1–2.

[5] Y. Shen, X. Tang, X. Xin, S. Liu, Z. Zhu, and N. Sun, "A 10-bit 100-MS/s SAR ADC With Always-On Reference Ripple Cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 10, pp. 3965–3975, 2022.

[6] L. Chen, A. Sanyal, J. Ma, and N. Sun, "A 24-μW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique," in *IEEE European Solid State Circuits Conference*, 2014, pp. 219–222.

[7] C.-H. Chan, Y. Zhu, C. Li, W.-H. Zhang, I.-M. Ho, L. Wei, U. Seng-Pan, and R. P. Martins, "60-dB SNDR 100-MS/s SAR ADCs with threshold reconfigurable reference error calibration," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 10, pp. 2576–2588, 2017.