A 13.2fJ/step 74.3-dB SNDR Pipelined Noise-shaping SAR+VCO ADC

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ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC) | 979-8-3503-0420-6/23/$31.00 ©2023 IEEE | DOI: 10.1109/ESSCIRC59616.2023.10268692

***Abstract*—This work presents an OTA-free pipelined passive noise-shaping SAR (NS-SAR) + VCO ADC that offers high resolution (>12-bit) with only a 5-bit NS-SAR stage and $4-36\times$ lower sampling capacitor compared to state-of-the-art NS-SARs with similar ENOB. Pipelining the NS-SAR and VCO stage linearizes VCO by reducing its input swing, increases the VCO integration time and its energy efficiency, and improves SFDR of ADC by suppressing frequency dependency of interstage gain. We demonstrate a simple calibration technique to extract interstage gain and track VCO gain accurately in the background. Fabricated in 65nm CMOS, the prototype ADC achieves the best Walden FoM among state-of-the-art passive NS-SAR ADCs in similar technology and consumes 0.12mW with SNDR/SFDR of 74.3/89.1dB at 13.2fJ/step for OSR of 9.**

***Index Terms*—noise-shaping SAR, ring VCO, oversampling ADC, inter-stage gain calibration and pipelined ADC**

I. Introduction

Noise-shaping successive approximation register (NS-SAR) combines advantages of both SAR and $\Delta\Sigma$ and employs either a passive integrator or an active integrator as loop filter. Passive integrator [1], [2] has advantages of avoiding amplifiers at the cost of weak noise-shaping at low oversampling ratio (OSR). Active integrators with open-loop dynamic amplifiers have simple architecture and high energy efficiency [3] but are sensitive to PVT variations that can potentially make the NS-SAR unstable without background gain calibration [3]. Closed-loop dynamic amplifiers are more robust against PVT variations but need complex optimization [4]. Despite recent advances, state-of-the-art NS-SARs still need high resolution SAR quantizer, i.e., at least 10-bit SAR to achieve >12-bit performance at low OSR which brings the additional challenge of driving a large sampling capacitor. Our prior work [5] presented a MASH architecture with NS-SAR as first stage and a ring voltage controlled oscillator (VCO) as second stage to relax capacitor driving requirements. However, the MASH architecture creates a frequency dependent interstage gain that limits suppression of quantization error from NS-SAR at ADC output and reduces SFDR of the ADC. Further, the VCO is used as integrator only when the NS-SAR is not quantizing which limits energy efficiency of the VCO.

We propose a pipelined NS-SAR+VCO architecture that addresses the above challenges and brings the following advantages – 1) the VCO suppresses quantization error and comparator noise of SAR stage which address weak noise-shaping from passive integrator; 2) the NS-SAR resolution is low (5-bit) which relaxes the requirements for driving sampling capacitor; 3) the passive integrator linearizes VCO by limiting its input swing; 4) pipelining suppresses frequency dependence of interstage gain, and improves SFDR by 8dB and ADC energy efficiency by $2\times$ compared to the MASH architecture in [5].

II. Proposed Pipelined NS-SAR+VCO

A. Architecture

The proposed pipelined NS-SAR+VCO architecture and associated timing diagram are shown in Fig. 1. The input signal is sampled during ϕ_s and 5 cycles of SAR conversion follows the sampling phase. After the SAR conversion is over, the residue is dumped on the capacitor C_{intg} which realizes passive integration of the SAR residue during ϕ_{ns0} phase. Thus, the NS-SAR effectively behaves as a feedforward $\Delta\Sigma$ modulator with first-order noise shaping with a signal transfer function (STF) of 1 and noise transfer function (NTF) of $\left[1-(1-a)z^{-1}\right]$ where $a = C_{dac}/\left(C_{dac}+C_{intg}\right)$ and C_{dac} is the SAR DAC capacitance. Direct integration of SAR residue on C_{intg} instead of charge-sharing with a small capacitor before integration [5] reduces kT/C noise of SAR. The trade-off with direct integration is that C_{intg} needs to be larger than C_{dac} to push NTF zero close to dc and ensure adequate in-band noise suppression. While this would necessitate a large C_{intg} in high-resolution NS-SAR ADCs with large C_{dac}, the proposed NS-SAR+VCO ADC uses a low-resolution SAR ADC thus ensuring that C_{intg} is still relatively small. In addition, the pipelined architecture cancels quantization noise in SAR thus relaxing the need for an aggressive NTF. Hence, the ratio of C_{intg}/C_{dac} is set to 3 in this design which results in NTF of $(1-0.75z^{-1})$. The NS-SAR uses a 2-input comparator to add SAR residue and passive integrator output. While a 2-input comparator has higher noise than single input comparator, the pipelined architecture cancels comparator quantization noise and does not affect SNR of the ADC.

The passive integrator output is sent to the VCO for time-domain quantization. Due to pipelining, C_{intg} acts as zero-order-hold for the VCO which performs integration over the entire ADC sampling period except for ϕ_{ns0} as shown in Fig. 1a). This improves SQNR of VCO stage and reduces frequency dependence of interstage gain which is discussed in Section II-B. Fig. 1b) shows the circuit schematic for the second-stage VCO. A seven-stage current-starved ring inverter chain is used as the VCO. At any given time only one of the seven inverters in each VCO stage is undergoing

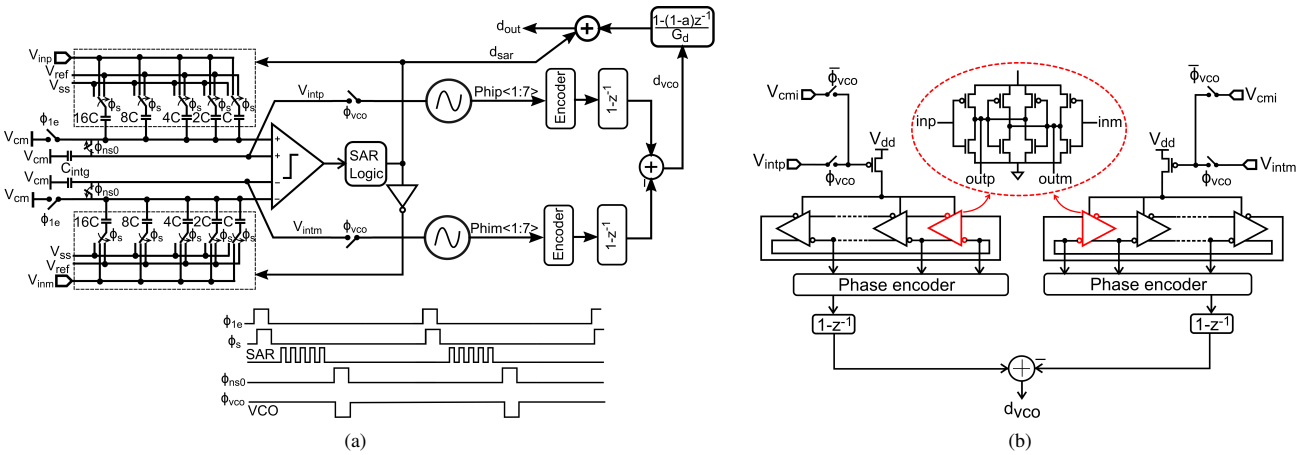


Fig. 1: a) Schematic and timing diagram of the proposed NS-SAR+VCO ADC b) circuit schematic of the VCO stage

transition, rising or falling. Thus, the 7-stage VCO quantizes the phase interval $(0,2\pi)$ into 14 levels corresponding to 7 rising transitions and 7 falling transitions. The quantized phase is in one-hot format that a phase encoder converts to binary word. The binary phase output is digitally differentiated to form the VCO stage output. The VCO output is digitally differentiated with NTF of NS-SAR and combined with the SAR output after scaling by interstage gain to form the overall ADC output.

Fig. 2 shows a simplified mathematical model of the proposed ADC and its transfer functions. kT/C noise in SAR DAC and passive integrator are denoted by n_1 and n_2 respectively, $g = 1/a$ is gain of the integration path in the comparator, Q_1 is quantization noise in SAR, n_3 is thermal noise of comparator, δ represents capacitance mismatch error in SAR DAC, n_4 is VCO input-referred thermal noise, G_{vco} is VCO tuning gain, Q_2 is quantization noise in the VCO and G_d is interstage gain. The ADC has very low sensitivity to g and precise matching/calibration is not needed to accurately set the value of g. After combining the NS-SAR and VCO outputs with the correct interstage gain, noise in the ADC output comprises of second-order shaped VCO quantization noise, first-order shaped VCO thermal noise, and unshaped DAC mismatch error and kT/C noise from the NS-SAR stage which forms the in-band noise floor.

B. Interstage gain

The interface between discrete-time (DT) SAR and continuous-time (CT) VCO introduces reconstruction error when outputs from the two stages are combined. Since the VCO quantizes the passive integrator output over a fraction of the ADC sampling period (during ϕ_{vco} phase in Fig. 1a)), this effectively realizes a passive mixer in front of the VCO as shown in Fig. 3a) [5]. Mixing spreads out frequency spectrum of the passive integrator output and creates multiple copies around harmonics of the ADC sampling frequency f_s. Anti-aliasing in the VCO attenuates the mixer output in higher nyquist bands and hence the sampled VCO output is not a perfect reconstruction of the passive integrator output even if

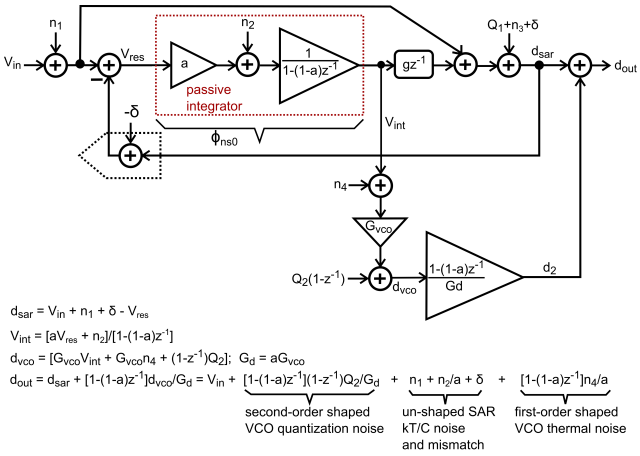


Fig. 2: Mathematical model of the ADC

the VCO was an ideal quantizer. Thus, the interstage gain is frequency dependent and quantization noise from the first stage cannot be completely canceled at the ADC output.

Assuming the passive mixer is controlled by a pulse train $p(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_s t)$, where a_0 is the duty-cycle of ϕ_{vco}, Fig. 3b) plots the interstage gain normalized by G_d for [5] and for this work. For the same ADC sampling frequency, pipelining increases the duty-cycle of ϕ_{vco} by $2\times$ in this work and reduces inter-stage gain variation with frequency by $20\times$ compared to that in [5]. The in-band quantization noise of the NS-SAR stage at the ADC output with an ideal VCO back-end can be written as

$$P_q = \frac{\left[1+(1-a)^2-2(1-a)\right]}{12(OSR)^3}\frac{\Delta^2}{12}\left(\sum_{n=1}\frac{a_n}{n}\right)^2 \qquad (1)$$

where $a_n = \frac{2}{n\pi}\sin\left(\frac{nd\pi}{2}\right)$, and $\Delta^2/12$ is quantization noise power of the 5-bit SAR. Longer duty cycle of $p(t)$ results in more attenuation of the in-band quantization error from NS-SAR stage. Thus, pipelining NS-SAR+VCO attenuates quan-

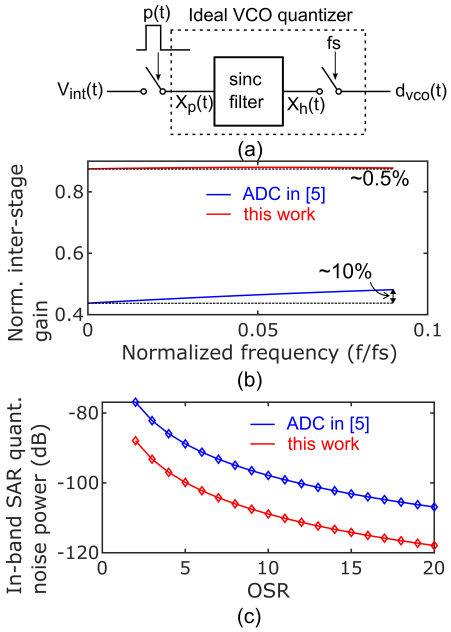


Fig. 3: a) simplified block diagram of passive mixing and ideal VCO back-end quantizer, b) normalized inter-stage gain vs frequency and c) in-band SAR quantization noise power comparison between [5] and this work

tization noise from NS-SAR by more than 10dB compared to the work in [5] as shown in Fig. 3c).

C. ADC calibration

Fig. 4 shows the proposed calibration method that employs a combination of foreground and background techniques. The foreground calibration runs once at chip startup to extract the interstage gain, and the background calibration keeps running during normal operation to track the interstage gain with changes in voltage/temperature. During foreground calibration, the ADC differential input is set to 0, and the NS-SAR output is dominated by its high-pass shaped quantization error due to low-resolution (5-bit) of the NS-SAR, while the VCO output is dominated by the high-pass shaped quantization error from NS-SAR stage scaled by interstage gain. The variance of SAR output can be written as

$$\begin{aligned}\sigma^2(d_{sar}) &= \sigma^2\left(\{1-(1-a)z^{-1}\}Q_1\right)+\sigma^2(n_1)\\ &+ \sigma^2\left(\{1-(1-a)z^{-1}\}n_3\right)+\sigma^2(n_2)/a^2\\ &\approx \sigma^2\left(\{1-(1-a)z^{-1}\}Q_1\right) \qquad (2)\end{aligned}$$

where the in-band quantization noise power of SAR stage dominates the thermal noise sources. Similarly, variance of VCO output after passing through $[1-(1-a)z^{-1}]$ filter, $d_2=[1-(1-a)z^{-1}]d_{vco}$, can be written as

$$\sigma^2(d_2)\approx[G_{vco}a]^2\,\sigma^2\left(\{1-(1-a)z^{-1}\}Q_1\right) \qquad (3)$$

Thus, ratio of variance of filtered VCO output to variance of NS-SAR output gives the square of the interstage gain. The NS-SAR NTF zero location is extracted in the foreground

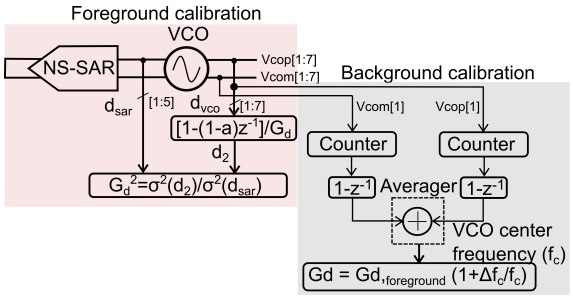


Fig. 4: Foreground and background calibration techniques to estimate and track interstage gain across PVT

using Nedler-Mead optimization. Since the NS-SAR NTF zero is set by ratio of capacitors, background calibration is not required for tracking its location. During background calibration, the ADC operates normally and the 2π-crossing points of the differential VCOs are recorded by counters that operate at rising edges of 1 inverter from each VCO. The counter outputs are differentiated and added together, and temporal average of the sum represents the free-running frequency of the VCOs. Variations in PVT are captured in the temporal average, and the interstage gain is updated in the background by multiplying the interstage gain calculated using foreground calibration with fractional change in VCO frequency as shown in Fig. 4.

III. Measurement Results

The ADC is fabricated in 65nm CMOS process and Fig. 5a) shows the die photo. The ADC consumes 120μW at 18.75MHz operating frequency. The NS-SAR consumes 74.4μW from 1.2V supply while the VCO and background calibration circuit consumes 45.6μW from 0.95V supply. Fig. 5(b) shows the measured SNDR versus input amplitude for OSR of 9. The ADC has a measured dynamic range of 76dB.

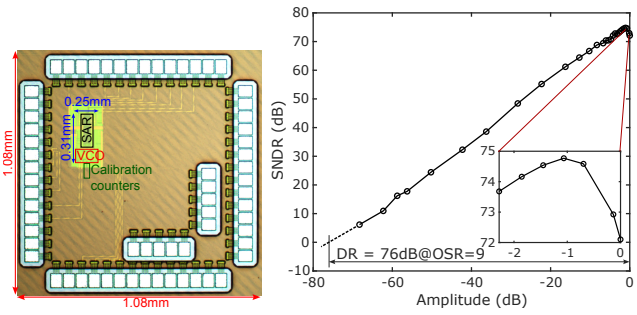
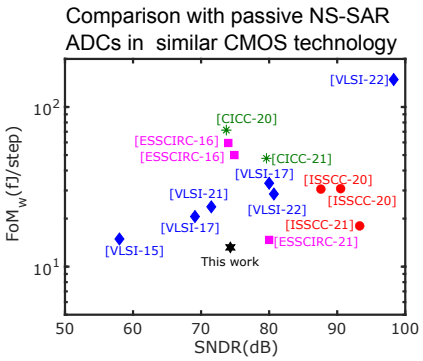


Fig. 5: (a) Die micro-photo (b) ADC dynamic range plot

Fig. 6 shows the measured FFT of the test-chip with 100kHz sinusoidal input. The VCO stage suppresses quantization error tones from NS-SAR by >35dB, reduces in-band noise floor by >25dB and improves SFDR by 8dB compared to [5]. Fig. 7a) and b) show SNDR as a function of input frequency

TABLE I: Comparison with state-of-the-art NS-SAR ADCs

	This work		JSSC' 2021 [5]	ISSCC' 2020 [1]	ISSCC' 2021 [2]	VLSI' 2022 [6]	VLSI' 2022 [7]	ESSCIRC' 2021 [8]
Process	**65nm**		65nm	40nm	40nm	65nm	65nm	65nm
Area (mm^2)	**0.08**		0.04	0.06	0.09	0.13	0.03	0.04
Fs (MHz)	**19**		24	2	5	0.2	2	1
Supply (V)	**1.2/0.95**		1.1/1	1.1	1.1	1	1	1.2
SAR resolution	**5b**		5b	14b	13b	7b	12b	10b
Sampling cap	**1.1pF**		1.1pF	36pF	16pF	–	4pF	2pF
$\Delta\Sigma$-order	**2**		2	1	4	3	2	2
PVT-robust	**Yes**		No	Yes	Yes	–	No	No
Power (μW)	**120**		160	67.4	340	5.2	13.5	7.3
BW (kHz)	**1040**	**235**	1100	40	250	10	62.5	31.25
OSR	**9**	**40**	11	25	10	10	16	16
SNDR (dB)	**74.3**	**82.3**	71.5	90.5	93.3	80.7	77.3	80
FoM_W(fJ/step)	**13.2**	**23.2**	23.3	29.7	18.1	28.5	18	14.3
FoM_S(dB)	**173.7**	**175.2**	169.9	178.2	182	173.5	174	176.3



and SNDR for multiple test-chips at OSR of 9 respectively. Fig. 7c) and d) show SNDR variation with supply voltage and temperature with 100kHz input frequency and OSR of 9 respectively. Reduction in supply voltage reduces ADC SNDR, but background calibration improves SNDR by 11dB at 15% reduction in supply voltage. Background calibration also improves SNDR by 15dB in the temperature range from 40°C-70°C. Table I summarizes performance of the test-chip and compares with state-of-the-art. The proposed ADC achieves the best walden FoM among passive NS-SAR ADCs in similar process and needs only a 5-bit SAR with 1.1pF sampling capacitor compared to 4-36pF needed by state-of-the-art NS-SAR to achieve high ENOB at low OSR. Thanks to the pipelined architecture, the proposed ADC has higher SNDR and 2× better energy-efficiency than [5].

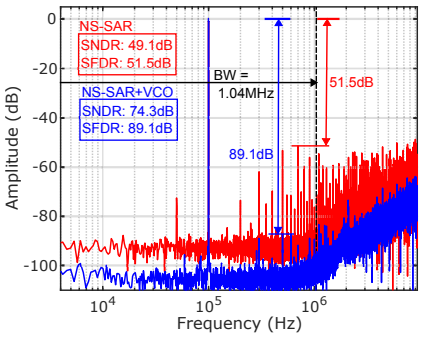


Fig. 6: Measured FFT with 100kHz input

IV. Conclusion

This work has presented a pipelined NS-SAR+VCO ADC that significantly relaxes the challenge of driving large sampling capacitance while improving suppression of in-band quantization noise. Thanks to the pipelined architecture, the proposed ADC achieves the best energy efficiency among high-resolution passive NS-SAR ADCs.

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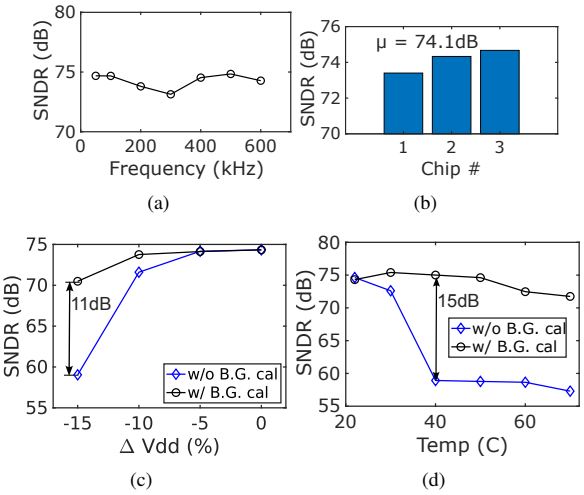

Fig. 7: Measured SNDR a) vs input frequency b) for 3 test-chips c) vs supply voltage with and without calibration d) vs temperature with and without calibration

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