OTA-free 1-1 MASH ADC using Fully Passive Noise Shaping SAR & VCO ADC

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Abstract

We present an OTA-free 1-1 MASH ADC utilizing a fully passive noise shaping (FPNS) SAR as first-stage and open-loop VCO ADC as second stage. The key contribution of this work is to address the challenge of driving large sampling capacitor for high resolution NS-SAR. The proposed architecture reduces resolution of SAR stage and leverages residue attenuation due to passive charge sharing in the FPNS SAR to linearize the VCO. Combining an FPNS SAR with a VCO ADC shapes in-band thermal noise of VCO and SAR comparator at ADC output. Additionally, we demonstrate a computationally inexpensive foreground inter-stage gain calibration algorithm for the proposed ADC architecture. The prototype ADC consumes 0.16mW while achieving an SNDR/DR of 71.5/75.8dB over a 1.1MHz bandwidth and walden FoM of 23.3fJ/step which is the *lowest* in 65nm technology.

Keywords: noise-shaping SAR, ring VCO, oversampling ADC, inter-stage gain calibration and MASH

Introduction

NS-SAR ADCs combine the advantages of both SAR and $\Delta\sum$ and suppresses comparator thermal noise and ADC quantization noise in the signal band. However, state-of-the-art NS-SAR ADCs use 9-11 bit DAC to achieve ~12/13 bit resolution at low OSR, which brings the challenge of driving large sampling capacitor [1-2]. MASH architecture can address this challenge by reducing the sampling capacitor in the first NS-SAR stage. A recent work [3] has presented a 1-2 MASH with NS-SAR ADCs in both stages. The first NS-SAR stage uses active integrator which is re-used to amplify residue of first stage. However, the use of active integrator makes the ADC less scaling friendly and increases overall power consumption of the ADC.

We propose an OTA-free MASH ADC which uses 5-bit FPNS-SAR as first stage and a ring VCO as second stage. The passive integrator output of the SAR stage drives the second stage VCO. Attenuation of passive integrator output due to charge sharing linearizes the VCO for low-resolution SAR which relaxes the driving requirement. Since VCO provides intrinsic amplification, separate inter-stage gain amplification is not needed. We use a fast-convergence digital foreground calibration technique to extract interstage gain precisely.

Proposed Architecture

Fig. 1 illustrates the proposed MASH ADC architecture and timing diagram. The FPNS-SAR acts as coarse quantizer, and the second-stage VCO acts as fine quantizer. The SAR residue is first charge-shared with a small capacitor, C_1=aCdac/(1-a), during $\emptyset ns0$, and then integrated on C_2=Cdac during $\emptyset ns1$ cycles. In this design a=0.25, which results in an NTF of (1-$0.75z^{-1}$) for the SAR stage. The integrated residue (Vint) is fed to the VCO ADC in the second stage. Fig. 2 shows the block diagram of the proposed ADC and its transfer functions. The SAR stage uses multi-path comparator with the passive integration path having a gain of g=1/a. Quantization noise of the ADC is set by quantization noise in the VCO stage and is second-order shaped. Thermal noise of the VCO as well as comparator in the SAR stage are high passed by (1-$0.75z^{-1}$), and the in-band noise floor is set by kT/C noise of the SAR stage, and in particular kT/C noise of C_1.

The 5-bit SAR uses bi-directional single-sided switching technique to reduce switching energy by 86% compared to the conventional SAR. A PMOS gm-stage converts Vint to current for driving the VCO stage. The VCO stage has 7 inverters in which phase output of all the inverters are read-out to form the VCO output. Fig. 3 shows variation in simulated ADC SNDR as the integration path gain, g, is swept from -30% to 30%. The ADC has very low sensitivity to 'g' which obviates the need for precise matching or calibration.

Inter-stage Gain Calibration

The inter-stage gain is set by a(1-a)CpGvco where Cp is the attenuation due to parasitic capacitance at the passive integration node, and Gvco is the gain of the VCO stage. Cp and 'a' are set by ratio of capacitors and has low sensitivity to PVT, while Gvco is highly sensitive to PVT. We use Nedler-Mead technique to perform one-time calibration and extract 'a', and hence, the NTF zero for the SAR stage. To extract Gvco, we use a simple digital calibration technique. As seen from the ADC transfer functions in Fig. 2, if Vin is set to 0, ratio of standard deviation of VCO output to standard deviation of SAR output is a measure of the inter-stage gain. The error in the inter-stage gain calculation is due to thermal noise in SAR and VCO stages and quantization noise Q2 of VCO. Since the SAR has low resolution of 5-bit, its quantization noise Q1 has a larger standard deviation than the other noise components which reduces error in inter-stage extraction. The inter-stage gain calibration needs to be performed with change in VT which can be monitored by observing the VCO frequency over time using a digital counter clocked by 1 inverter in the VCO.

Measurement Results

The proposed ADC is fabricated in 65nm and consumes 160µW from 1.1V supply at 24MHz sampling frequency. Out of 160µW power, the SAR consumes 110µW and the VCO consumes 50µW. Fig. 4 shows the measured 65k point FFT. The overall ADC has 20dB lower in-band noise floor and 24dB better SFDR than the SAR stage. The ADC has an SNDR of 71.4dB at an OSR of 11. Fig. 5 shows the measured SNR/SNDR versus input amplitude. The ADC has a dynamic range of 75.8dB, and the upper limit on SNR is due to increase in noise floor due to capacitor mismatch which is not calibrated in this design. Fig. 6 shows SNDR with and without inter-stage gain calibration as the supply voltage is swept by +/-10%. Fig. 7 shows walden and schreier FoM vs OSR. Fig. 8 shows convergence speed of the inter-stage gain calibration technique without applying any input signal. The gain calibration requires 5000 samples (0.21ms) for convergence. Fig. 9 shows the SNDR of 3 test-chips. The average SNDR is 71.1dB. The die micro-photograph is shown in Fig. 10. Fig. 11 compares graphically walden FoM of the proposed ADC with state-of-the-art oversampling ADCs in 65nm, and with state-of-the-art ADCs with similar bandwidth across technology. The proposed ADC achieves the best walden FoM at 65nm, and the ADC performance can be improved further with technology scaling.

Acknowledgment The authors would like to thank Michael

Berens of NXP Semiconductor, Austin, TX for insightful discussions during the ADC design phase.

References

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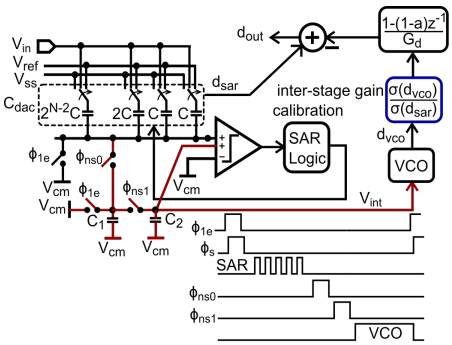


Fig. 1 Proposed 1-1 NS-SAR+VCO

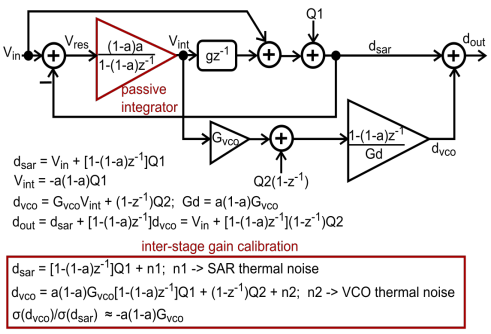


Fig. 2 ADC block diagram and transfer functions

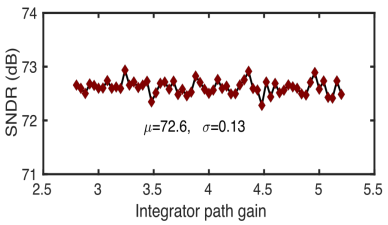


Fig. 3 Simulated SNDR vs integrator path gain

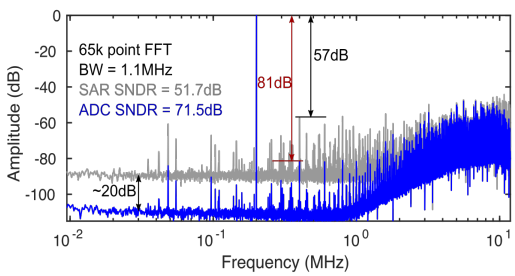


Fig. 4 Measured 65k point FFT

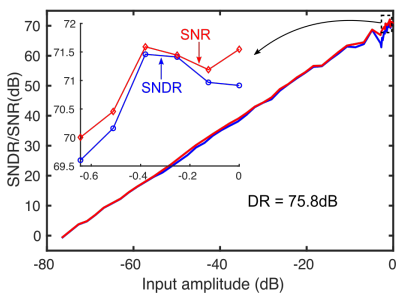


Fig. 5 Measured ADC dynamic range

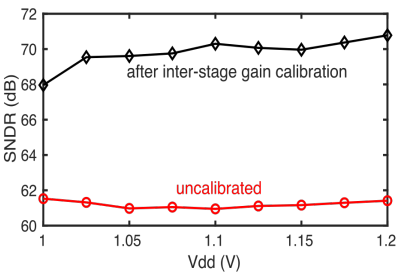


Fig. 6 SNDR with supply variation with and without inter-stage gain calibration

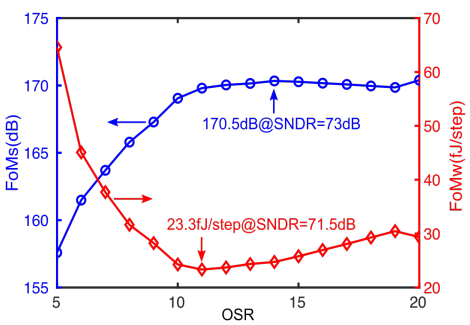


Fig. 7 Schreier and Walden FoM vs OSR

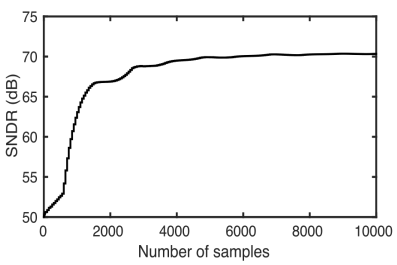


Fig. 8 Convergence speed of inter-stage gain calibration

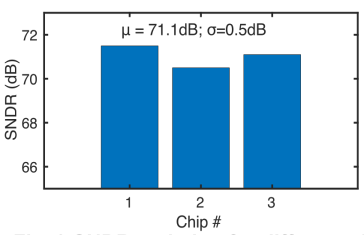


Fig. 9 SNDR variation for different chips

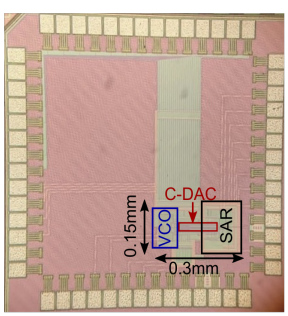
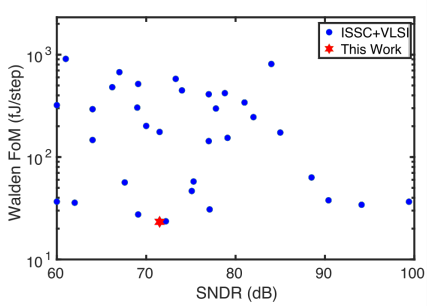


Fig. 10 Die photo



	This work	CICC '20 [3]	CICC '19 [5]	JSSC '19 [6]	VLSI '19 [7]
Architecture	NS SAR + VCO (1-1)	NS SAR Pipeline	NS SAR	CTDSM	SAR Pipeline
OTA	No	Yes	No	Yes	Yes
fs (MHz)	24	83.3	80	500	100
BW (MHz)	1.1	6	2	12.5	12.5
SNDR (dB)	71.5	73.7	73.8	70.4	75.8
DR (dB)	75.8	80	77	73	76.8
Power (mW)	0.16	3.5	0.87	1.16	1.5
FoMw[1] (fJ/step)	23.3	71.7	52.8	17	11.5
FoMs[2] (dB)	169.9	166	167.4	170.7	175
FoMs[3] (dB)	174.1	172.3	170.6	173.3	176
Technology (nm)	65	65	65	40	40
Area (mm²)	0.04	0.11	0.08	0.03	0.06

[1]FoMw = Power/2^ENOB/2*BW ; ENOB = (SNDR-1.76)/6 ;
[2]FoMs = SNDR + 10*log10(BW/Power) ; [3]FoMs = DR + 10*log10(BW/Power)

Fig. 11 Performance comparison with state-of-the-art