Stochastic $\Delta\Sigma$ VCO-ADC Utilizing 4x Staggered Averaging

Sanjeev Tannirkulam Chandrasekaran and Arindam Sanyal
Electrical Engineering Department, University at Buffalo, Buffalo, NY.
Email: {stannirk, arindams}@buffalo.edu

***Abstract*—This work presents a stochastic ring voltage controlled oscillator (VCO) based analog-to-digital converter (ADC) that combines spatial redundancy with staggered averaging to reduce both noise and distortion. Staggered averaging reduces quantization noise more than simple averaging with single clock phase for the same amount of spatial redundancy for VCO-ADCs. 4 continuous-time (CT) second-order VCO based sub-ADCs are run in parallel, and their outputs are sampled with multi-phase clocks followed by averaging to form the overall ADC output. We present behavioral simulation results and measurement results on 65nm CMOS test chip. Measurement results show staggered averaging improves SNR by an average of 7.6dB compared to single ADC. In contrast, simple averaging with 4 sub-ADCs can improve SNR by 6dB. The test chip consumes 0.36mW power and has SNDR of 63dB over 0.5MHz bandwidth.**

I. Introduction

With scaling in CMOS technology and advances in design techniques, non-idealities such as distortion and mismatch are often the limiting factors of data converter performance. While calibration or compensation techniques can suppress distortion and mismatch, a new class of stochastic analog-to-digital converters (ADCs) have emerged that leverage noise statistics and/or mismatch to improve ADC performance metrics. Stochastic ADCs employ spatial or temporal redundancy to extract statistical information on ADC non-idealities and compensate them in digital domain. Hence, stochastic techniques are an attractive solution for improving performance of ADCs in advanced CMOS technologies.

Stochastic ADCs with fast conversion rates usually use spatial redundancy while those with low conversion rates use temporal redundancy. While both spatial and temporal redundancy can suppress noise, an added advantage of spatial redundancy is that it can be employed to leverage intrinsic variations across multiple ADCs to suppress distortion too. [1] proposed a stochastic flash ADC which uses multiple comparators and leverages the gaussian distribution of comparator offsets to linearize the ADC output. [2] proposed a stochastic successive approximation register (SAR) ADC by employing 16 parallel comparators and averaging their outputs to reduce ADC thermal noise. [3] averaged outputs of 8 open-loop ring voltage-controlled oscillators (VCOs) to improve SNDR by 9dB. [4]–[6] used temporal redundancy by firing comparator of SAR ADC multiple times and applied majority voting, bayesian estimation and maximum likelihood estimation techniques respectively on the comparator outputs to improve ADC resolution.

This work presents a stochastic, continuous-time (CT) ADC which uses 4x spatial redundancy and staggered averaging to improve ADC resolution. Compared to simple averaging in which all sub-ADCs are sampled at the same point in time, the sub-ADCs are sampled at different points in time with staggered averaging. While simple averaging and staggered averaging reduce thermal noise by the same amount, staggered averaging leverages pulse-frequency modulated nature of VCO to achieve higher reduction of quantization noise as will be shown later. A second-order $\Delta\Sigma$ VCO-ADC is presented in this work which uses 4x staggered averaging to improve SNDR by 6.9-8.8dB compared to single sub-ADC. The rest of this paper is organized as follows: Section II presents proposed staggered averaging scheme applied to VCO-ADC design, Section III presents measured results on a 65nm test chip, while the conclusion is brought up in Section IV.

II. Stochastic ADC Architecture

Fig. 1 shows circuit schematic and timing diagram for the proposed stochastic ADC. The ADC consists of 4 CT sub-ADCs which are sampled using 4 clock phases $\phi_1 - \phi_4$, each being a 90° phase-shifted version of the previous clock phase. The four clock phases are derived from a master clock which runs at a frequency of $4f_s$, where f_s is sampling frequency of the ADC. The sub-ADC outputs are averaged to form the overall ADC output.

The ADC output, D_o, can be written mathematically as

$$D_o = \sum_{i=1}^{4} D_i^* \sum_k \delta\left(t - kT_s - (i-1)T_s/4\right) \tag{1}$$

where D_i^* denotes the output before sampling for the i-th sub-ADC, and T_s is the sampling period. In frequency domain, the ADC output can be written as

$$D_o(f) = \frac{1}{T_s} \sum_{i=1}^{4} D_i^*(f) \circledast \sum_k \delta\left(f - kf_s\right) e^{-j2\pi f(i-1)T_s/4} \tag{2}$$

where $\circledast$ denotes convolution operation. The key to differentiation between simple and staggered averaging lies in (2). For simple averaging, there is no phase-shift in the frequency contents of the sub-ADCs, while for staggered averaging, frequency contents of the sub-ADCs are phase-shifted before addition. This phase-shifting is particularly relevant for VCO-ADCs and allows greater reduction of quantization noise with staggered averaging than with simple averaging. To understand

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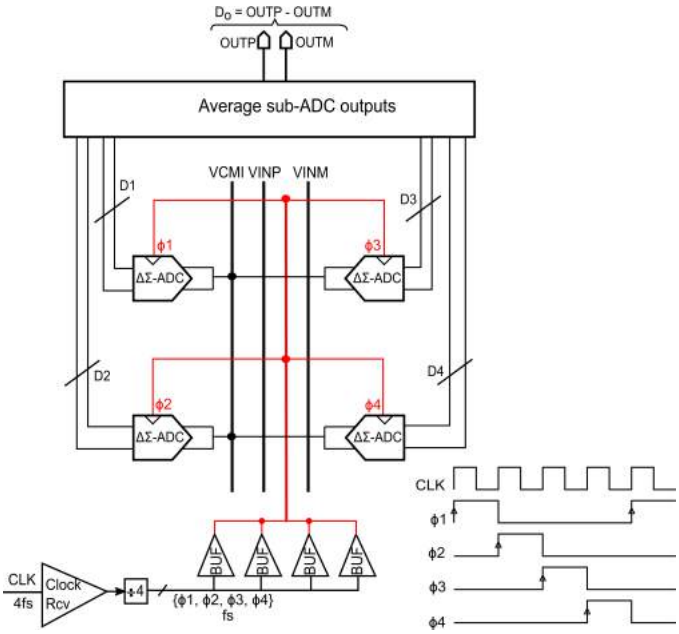

Fig. 1: Schematic of ADC with 4x staggered averaging

why, we need to take a closer look at quantization noise in a VCO.

As shown in [7], a VCO behaves as a pulse-frequency modulator (PFM), and spectrum of VCO output consists of 1) a tone at dc 2) a tone corresponding to the input signal, and 3) modulation side-bands around multiples of VCO center frequency, f_{vco}. Fig. 2 shows an example frequency response of VCO which shows modulation sidebands around integer multiples of f_{vco}. To employ a VCO as an ADC, a common circuit technique is to sample VCO output and pass it through XOR gates. As shown in [7], the XOR gate acts as a pulse-shaping filter with notches at integer multiples of sampling frequency which results in noise-shaping of the PFM sidebands, and gives rise to shaped quantization noise of VCO-ADC.

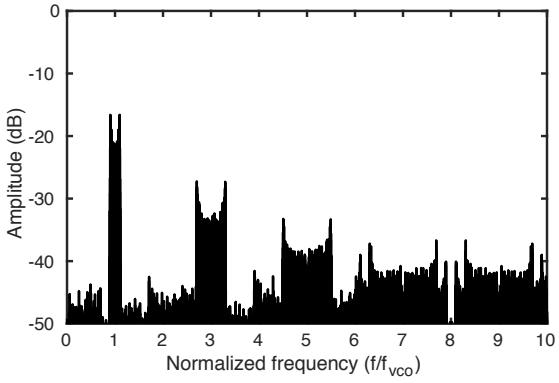

Fig. 2: Spectrum of VCO showing PFM sidebands

When the same input is given to different VCOs and they are sampled using different clock phases, the PFM tones fold into the signal band with different phase shifts for different VCOs. Hence, when the sampled outputs of multiple VCO-ADCs are added together, PFM tones which are close to integer multiples of f_s before sampling are canceled after addition. Setting f_{vco} close to integer multiple of f_s improves SQNR since pulse-shaping filter (usually XOR gates) maximally suppresses quantization tones and maximizes output swing of the VCO [8]. Simple averaging with the same clock phase does not produce different phase shifts for different VCO outputs, and hence, does not reduce quantization noise if all the VCO-ADCs are identical.

Fig. 3 show the mechanism of folding of shaped PFM tones after sampling. For sake of illustration, we consider 3 discrete PFM tones at frequencies of $f_s + \Delta f_1$, $2f_s + \Delta f_2$ and $4f_s + \Delta f_3$ before sampling. After sampling, the PFM tones fold into signal-band but with different amplitudes. If all the sub-ADCs are identical, the PFM tones around f_s and $2f_s$ are canceled but the PFM tone around $4f_s$ folds back into the signal band. In general, for identical sub-ADCs, PFM tones around mf_s, $(m \neq 4k,\ k \in \mathbb{Z})$ will be canceled and the quantization noise of the stochastic ADC due to folding of tones around integer multiples of $4f_s$. In contrast, if the sub-ADC outputs are sampled using the same clock phase, there will be no reduction in quantization noise if the sub-ADCs are identical since quantization noise is a deterministic function of the input signal. In practice, mismatch between the sub-ADCs de-correlate quantization noise from the different sub-ADCs and simple averaging also reduces overall quantization noise.

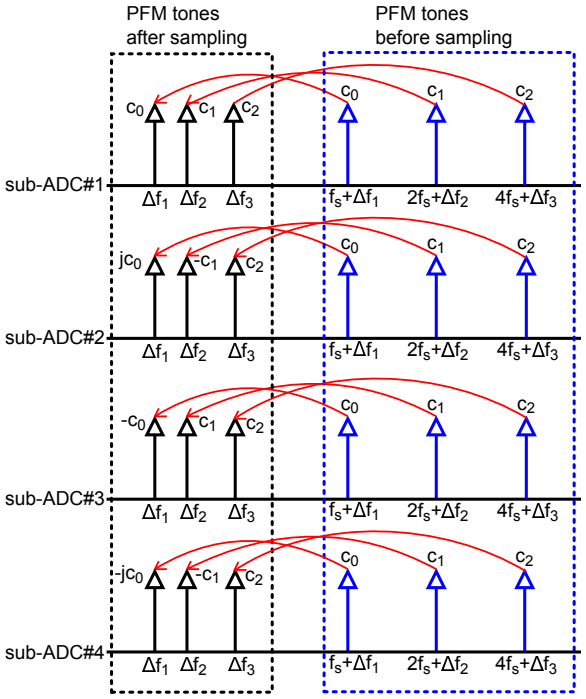

Fig. 3: In-band folding of PFM tones with staggered averaging

Fig. 4 compares SQNR for simple averaging and staggered averaging without and with mismatches between sub-ADCs. 4 second-order VCO based sub-ADCs are used for the simulation. Fig. 4 shows 2^{15} point FFT plots which are averaged 20 times. Without any mismatch between the sub-ADCs, quantization noise from all the sub-ADCs are correlated and

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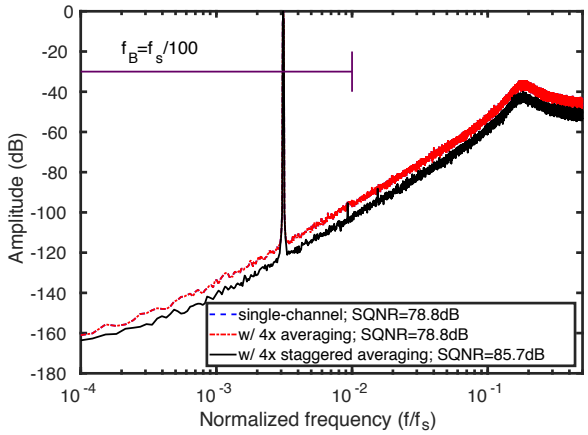
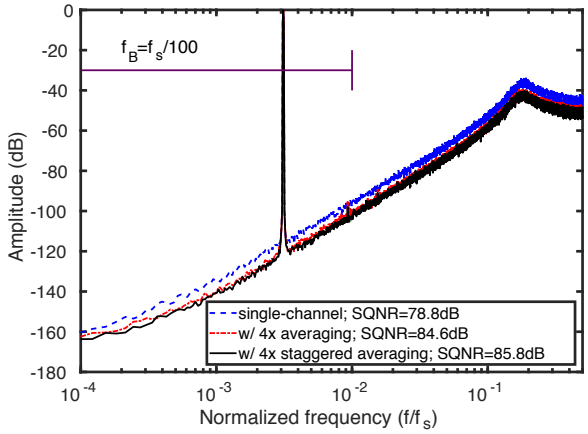
simple averaging does not reduce quantization noise. Hence, as shown in Fig. 4(a), SQNR for single sub-ADC is same as SQNR obtained after averaging outputs of all the sub-ADCs. In contrast, staggered averaging improves SQNR by 6.9dB. With 1% channel mismatch added, the quantization noises from the sub-ADCs are de-correlated and averaging results in 5.8dB improvement in SQNR compared to single sub-ADC, while staggered averaging improves SQNR by 7dB compared to single sub-ADC. Thus, while channel mismatch results in SQNR improvement with regular averaging, staggered averaging still outperforms single-phase averaging. Fig. 5 shows improvement in SQNR obtained through staggered averaging over regular averaging versus number of sub-ADCs. 1% mismatch is assumed between sub-ADCs and the SQNRs reported are mean values from 20 simulations. It can be seen that staggered averaging performs better than simple averaging and the SQNR improvement increases with number of sub-ADCs.



(a)



(b)

Fig. 4: Simulated FFT plots for single sub-ADC, with 4x averaging and with 4x staggered averaging for a) identical sub-ADCs b) 1% mismatch between sub-ADCs

Fig. 6 shows the second-order CT sub-ADC architecture used in this work. The sub-ADC uses two ring VCO integrators in a negative feedback loop to achieve second-order

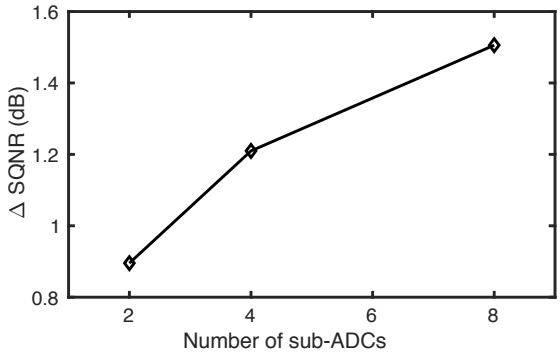


Fig. 5: Improvement in SQNR through staggered averaging over simple averaging versus number of sub-ADCs

quantization noise shaping. Both VCOs consist of 13 ring inverter stages. While the sub-ADC architecture is based on the work in [9], there is an important difference in the current-steering feedback DAC which reduces power consumption by close to 3x compared to the ADC in [9]. The ADC in [9] uses a PMOS current source to bias the first VCO and an NMOS DAC. Instead of using NMOS DAC which sinks current away from the PMOS current source, this work uses a PMOS DAC. Current in the PMOS DAC is re-used for biasing the first VCO, thus reducing sub-ADC current consumption. The input is applied through differential PMOS transconductance stages as shown in Fig. 6. As discussed in [9], center frequency of first VCO is set to $1.3f_s$ to avoid aliasing of its PFM tones in-band while the second VCO's center frequency is set to f_s to maximize the output swing without VCO overloading.

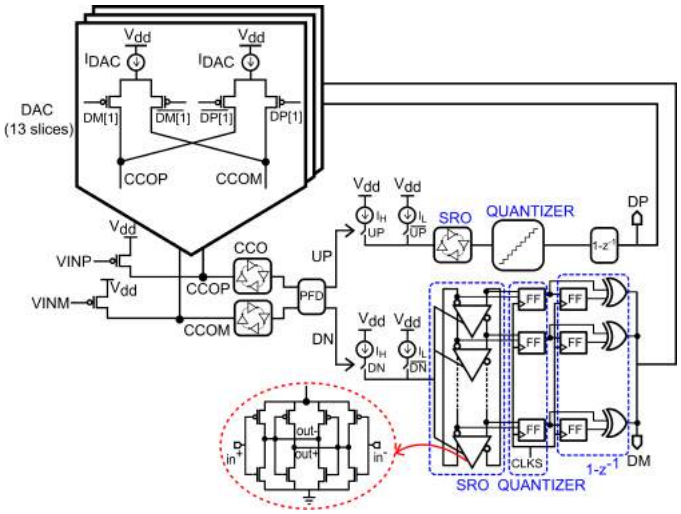


Fig. 6: Circuit schematic of sub-ADC

III. Measurement Results

Fig. 7 shows the micro-photograph of the test chip fabricated in 65nm CMOS process with the sub-ADCs and clock generator highlighted. The area of the core is 0.18mm^2. The ADC runs at 52MHz and consumes 0.36mW power from 0.9V supply. The sub-ADC outputs are averaged off-chip.

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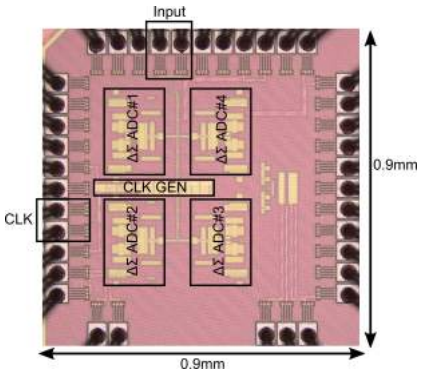


Fig. 7: Die microphotograph of the test chip

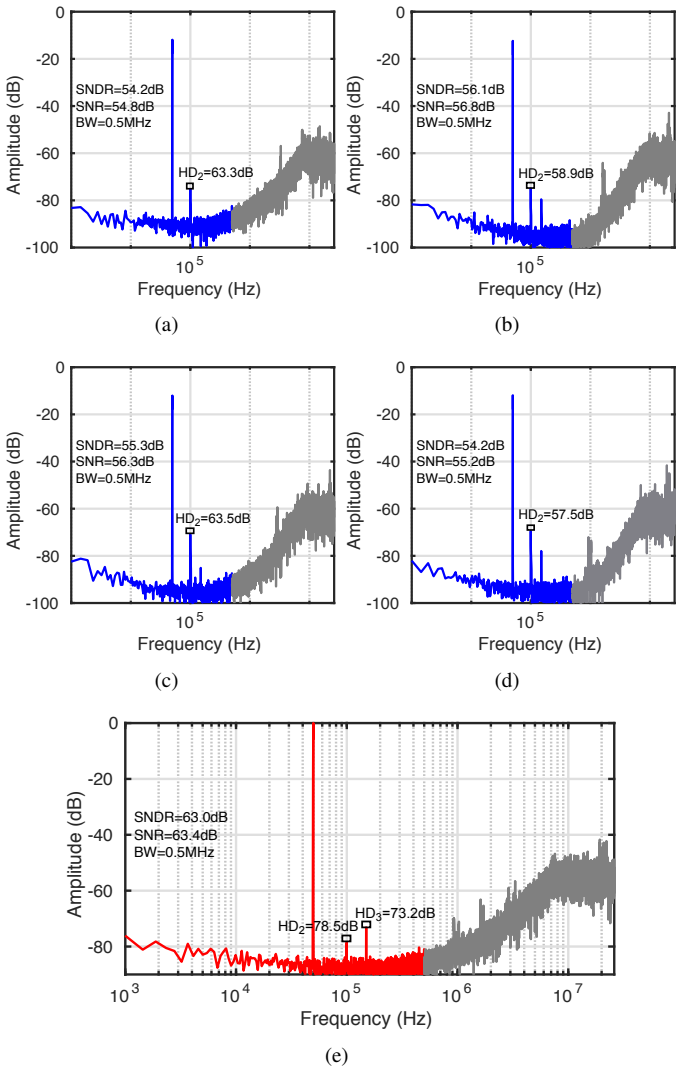


Fig. 8: FFT of a) sub-ADC 1 b) sub-ADC 2 c) sub-ADC 3 d) sub-ADC 4, and e) stochastic ADC

Fig. 8 shows FFT plots for each sub-ADC as well as the overall ADC for a bandwidth of 0.5MHz. Stochastic averaging improves SNDR by 6.9-8.8dB and SNR by 6.6-8.6dB compared to single sub-ADC. In contrast, simple averaging can improve SNR by maximum of 6dB for 4 sub-ADCs. Stochastic averaging also suppresses the second and third harmonics and improves SFDR by more than 10dB compared to the sub-ADCs. Fig. 9 shows SNDR for average sub-ADC and after 4x staggered averaging versus bandwidth. At low bandwidths, thermal noise is dominant and averaging improves SNDR by approximately 6dB. Beyond 200kHz bandwidth, quantization noise starts to dominate, and staggered averaging improves SNDR by close to 8dB.

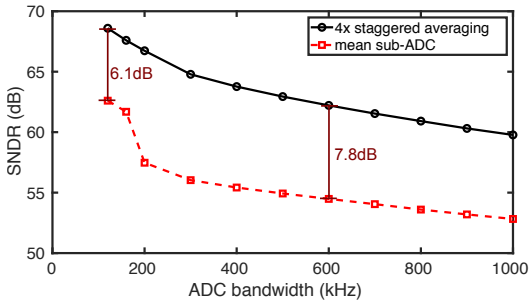
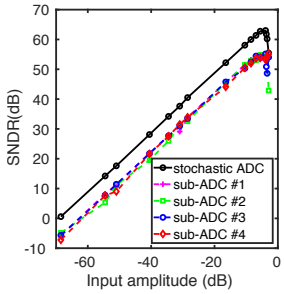


Fig. 9: ADC SNDR versus bandwidth

Fig. 10 shows measured SNDR versus input amplitude for the stochastic ADC and sub-ADCs, as well as summarizes the performance. 4x staggered averaging improves SNDR, SNR and DR by 8.1dB, 7.6dB and 7.7dB respectively compared to average sub-ADC. The SNR improvement is 1.6dB more than the maximum possible through simple averaging.



Supply(V)	0.9
Power(mW)	0.36
Area(mm^2)	0.18
F_s(MHz)	52
BW(MHz)	0.5
SNDR(dB)	63(averaged)
	54.9(sub-ADC)[1]
SNR(dB)	63.4(averaged)
	55.8(sub-ADC) [1]
DR(dB)	65.2(averaged)
	57.5 (sub-ADC)[1]

[1]mean of 4 sub-ADCs

Fig. 10: ADC dynamic range performance summary

IV. Conclusion

This work presents a staggered averaging technique for stochastic VCO-ADCs which uses multi-phase sampling to improve SQNR more than simple averaging. The SQNR advantage of staggered averaging over simple averaging is expected to improve with increase in number of sub-ADCs. The proposed staggered averaging technique is highly digital and simpler to implement than stochastic techniques which requires estimation of inverse gaussian cumulative density function, and the proposed stochastic ADC architecture is very suitable for CMOS technology scaling.

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