Flexible CMOS chip converted by a novel chip transformation process

J. Lai, S. T. Chandrasekaran, A. Sanyal and J.-H. Seo✉

In this Letter, the authors report a flexible CMOS chip converted by a novel chip transformation process. To realise a truly flexible CMOS chip, a two-step etching process was employed in the transformation process: (i) vapour etching to remove inter-dielectric layers followed by polymer encapsulation and (ii) plasma etching to remove the substrate of the chip. The *I–V* results measured after the chip transformation process show a voltage variance of <0.8% compared to the rigid chip. The bending test also revealed very small changes (0.6%) under strain conditions. Their results offer a viable route to use the foundry-fabricated CMOS chip for flexible chips; thus, a high-performance flexible chip can be realised. This technology will enable us to utilise various foundry-processed chips for future flexible applications such as health and environment monitoring, advanced mobile communication systems, and wearable electronics via a simple post-transformation process.

Introduction: Flexible electronics refers to technology that integrates electronic devices on flexible substrates [1]. Most studies in flexible electronics use organic or inorganic electronic devices that are deposited on a flexible substrate to form a flexible circuit, for example, a bottom-up approach [2, 3]. This type of use is due to difficulties in manufacturing flexible chips in commercial foundries. Soft and flexible substrates limit the resolution in the photolithography process, and various chemical processes to deposit and etch the layers that are not compatible with the flexible substrate. As a result of the bottom-up approach in flexible electronics in addition to the aforementioned restrictions in the manufacturing processes, the density of the devices in modern flexible electronics is much lower than foundry-processed chips, thus flexible electronics typically have limited functionality. This limited functionality further limits the development of advanced flexible systems that can be a crucial device type in the upcoming era of internet of things. To overcome this issue, several attempts have been made to realise a flexible chip from rigid foundry-processed chips via post-processing. The most common approaches are back-side etching such as a spalling process to form a thin substrate. Another popular approach is to use a Si-on insulator wafer to separate the top device layer by removing a buried oxide layer via a wet selective etching step [4, 5]. However, these approaches either work only for the full-wafer scale transformation or cause performance degradation by heat, mechanical stress, or chemical damage during the process; thus, they are not practical approaches for reliable chip transformation.

Here, we report a simple but viable approach to transform foundry-processed chips into flexible chips by employing two-step etching processes to remove both a Si substrate and a top inter-dielectric layer. In this way, the inter-dielectric layer can be removed and consequently leave the skeleton of the interconnects. The skeleton of the interconnects simultaneously fills with polydimethylsiloxane (PDMS), a soft elastomeric polymer, to protect and encapsulate the circuit layer. Thus, the flexible chip preserves the original performance of the chip after the transformation process is completed. This was confirmed by monitoring chip performance during the transformation process. The current–voltage (*I–V*) characteristics were traced during the chip-transformation process and showed that the variance in voltage bias was <0.8%. Furthermore, the flexible chip exhibited stable electrical characteristics under uniaxial strain conditions (up to 0.35% of compressive and tensile strains). These findings suggest a reliable chip transformation process. It further suggests that our method had a very small impact on the circuit due to the transformation process.

Experiments: Fig. 1 shows a schematic illustration of the fabrication process to transform the rigid foundry-processed chips into flexible chips. The process started with a hydrofluoride vapour etching to remove the top-side inter-dielectric layer (Fig. 1*a*) and encapsulating it with PDMS to protect the top surface from the following back-side plasma etching in addition to preventing the interconnect metal lines from collapsing during the process. It should be noted that the inter-dielectric layer was not completely removed, but the dense oxide material had become became a sponge-like shape. Thus, the multi-layer interconnections had not collapsed but PDMS slowly flowed and filled the empty spaces to support the circuit structure (Fig. 1*b*). Then, the back-side of the Si substrate was etched using an inductively coupled plasma (ICP) etcher for initial fast etching and a reactive ion etcher for final fine etching (Fig. 1*c*). After backside etching, a thickness of the Si substrate became <5 µm, and then the backside was coated with PDMS to complete the chip transformation process (Figs. 1*d–f*). Fig. 2 compares the top surface of the chip before and after the chip transformation in which there was no visual difference; namely, no noticeable cracks or fractures on the chip were found after chip transformation. While the rigid form of the chip showed a dark colour due to a thick substrate, the colour of the flexible chip became nearly transparent after the chip transformation process due to the removal of the substrate and the top inter-dielectric layer.

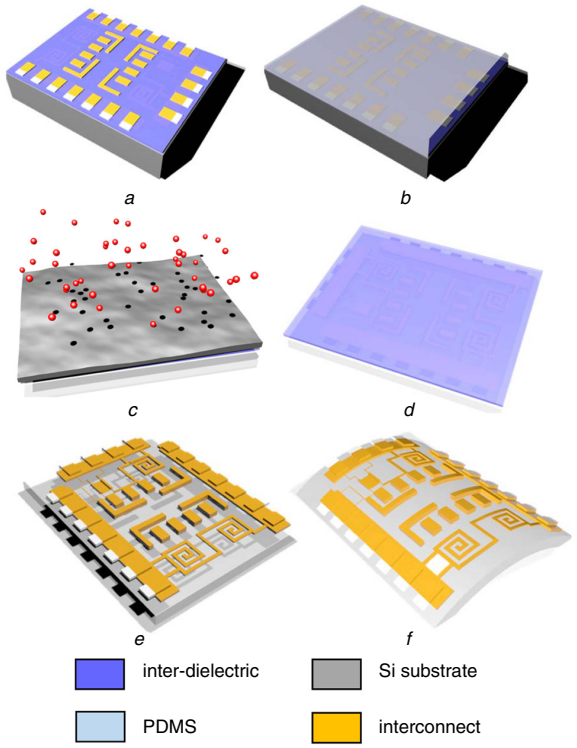

Fig. 1 *Schematic illustration of fabrication process to transform from rigid form of foundry-processed CMOS chip to flexible chip*

a Rigid foundry-processed chip
b Encapsulation of the top-side inter-dielectric layer after the hydrofluoride vapour etching
c Back-side Si etching using a plasma etcher
d-e Encapsulation of the back-side of the chip
f Completion of the flexible chip transformation process

The bias circuit was measured as a test point to track the performance of the chip and check the impact on the circuit during the chip transformation process. Fig. 3 shows the schematic of the circuit used in this experiment. The circuit implements a hardware accelerator for a reservoir-computing-based machine learning algorithm and consists of an input layer, a time-multiplexed reservoir layer, and an off-chip logistic regression layer for processing the reservoir states. The reservoir nonlinearly projects the input signal to a high-dimension that improves the separability of classes in the input data. The time-delayed feedback loop provides memory to the reservoir layer that allows the reservoir to exhibit properties of high-dimensionality using a small number of neurons. The delay in the loop is controlled by the tail-current source that was used as a test point for our experiments to demonstrate the flexibility of the converted chip.

Results and discussions: Fig. 4 shows the test pad that was measured before, during, and after the process. At 0.1 mA of current, the voltage output of the current mirror was 0.632 V. After the inter-dielectric layer removal (step (ii) in Fig. 1), the voltage reading was almost the same to be 0.631 V. After the back-side etching (step (iii) in Fig. 1), the voltage reading was 0.626 V. Therefore, the voltage drop after the chip transformation was 6 mV, which is about 0.8% different than the voltage reading from the rigid chip. We believe that there is a small room to reduce this voltage difference between the chip

transformation steps by modifying the back-side etching process to a less aggressive etching recipe to lower the temperature rise during the ICP etching by increasing the cooling cycles.

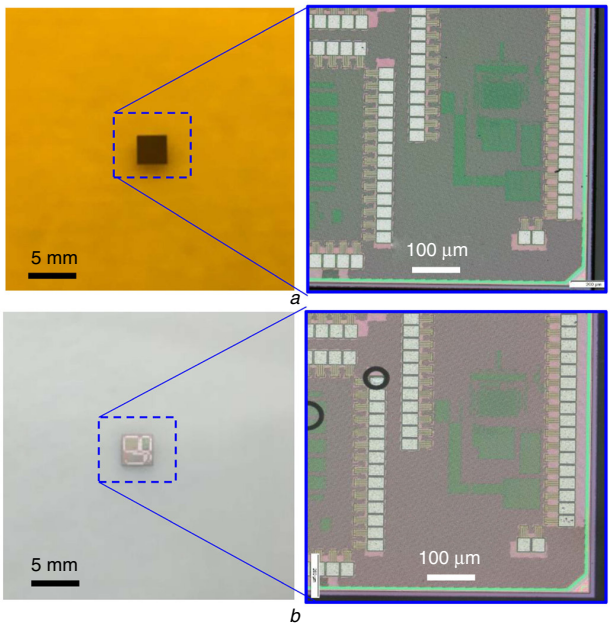

Fig. 2 *Comparison of the optical images. Microscopics on the right side show a microscopic image of the chip*

a Before chip transformation (rigid chip)
b After the chip transformation (flexible chip)

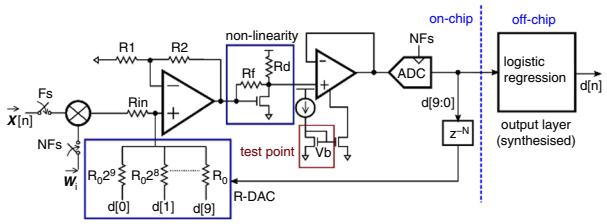

Fig. 3 *Schematic of circuit used in this work and location of test bias circuit that was used for test point*

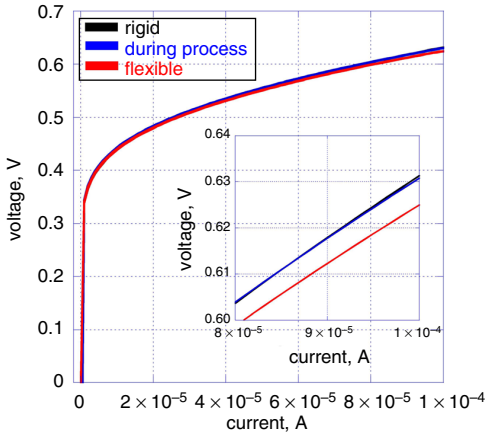

Fig. 4 *I–V characteristics of chip measured from test pad were measured before (black), after (red), and during process (blue)*

After the chip transformation process was complete, the flexible chip was measured under uniaxial strain conditions to monitor the changes in voltage readings due to bending. Figs. 5*a* and *b* show the *I–V* characteristics of the test current mirror under three different bending conditions: namely under 0.1, 0.2, and 0.35% of compressive and tensile uniaxial strains. The *I–V* curves measured under the highest compressive and tensile strain conditions (0.35%) show a similar degree of voltage drop (4 mV), which is about 0.6% difference compared to the voltage reading from the flexible chip at the flat condition. However, the current mirror voltage output returned to the same value (0.626 V) once the flexible chip was re-measured at the flat condition after the initial bending cycle indicating that the voltage reduction is not responsible for the structural damage of the flexible chip by the bending. Rather, the voltage reduction most likely occurred because the electrical properties of the chip such as resistivity and mobility of Si were slightly affected by the strain [6, 7]. It should be noted that the chip was encapsulated with the PDMS layer on both the top and bottom sides. Thus, the flexible chip lies in the strain neutral plane in which the compressive strain and tensile strain on the top and bottom of the chip are cancelled out; thus, the actual strain was nearly zero under bending conditions. In addition, the overall performance degradation from the rigid chip to the flexible chip under the high-strain condition was only about 1.4%. This small difference can be easily offset by digital trimming of the current mirror size and is much less than the variations due to a change in environmental conditions such as voltage and temperature.

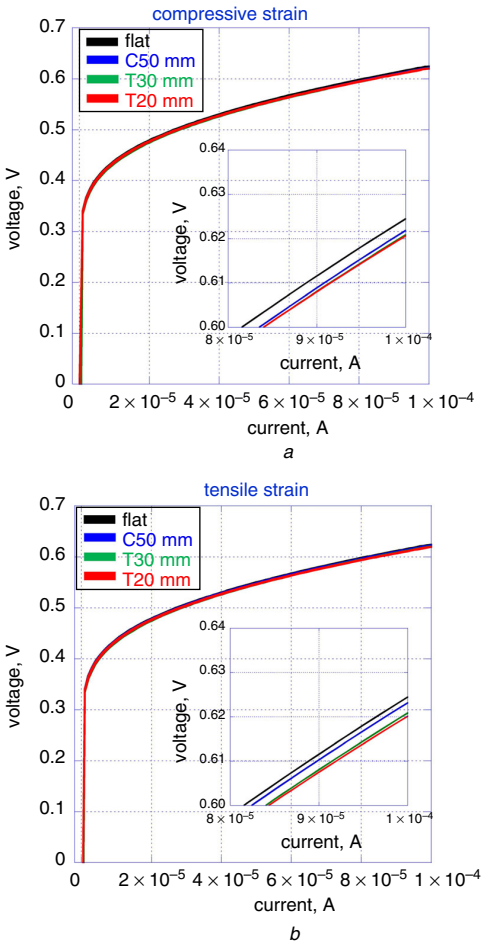

Fig. 5 *I–V characteristics of flexible chip measured under various uniaxial strain conditions. C,T, and numbers in legend denote compressive strain and tensile strain and diameter of metal moulds, respectively*

a I–V characteristic under compressive strain
b I–V characteristics under tensile strain

Conclusion: We report a flexible chip converted from a novel chip transformation process. To realise a truly flexible CMOS chip, a two-step etching process was used in the transformation process: (i) vapour etching to remove inter dielectric layers followed by the polymer encapsulation and (ii) plasma etching to remove the substrate of the chip. The *I–V* results measured after the chip transformation process show a voltage variance of <0.8% compared to the rigid chip. The bending test also reveals very small changes (0.6%) under strain conditions. Our result offers a viable route to using foundry-fabricated CMOS chips for the flexible chip. Thus, high-performance flexible chips can be produced. This technology will enable us to utilise various foundry-processed chips for future flexible applications such as health and environment monitoring,

advanced mobile communication systems, and wearable electronics, by adding a simple post-transformation process.

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One or more of the Figures in this Letter are available in colour online.

J. Lai and J.-H. Seo (*Department of Materials Design and Innovation, University at Buffalo, the State University of New York, Buffalo, NY 14260, USA*)

✉ E-mail: junghuns@buffalo.edu

S. T. Chandrasekaran and A. Sanyal (*Department of Electrical Engineering, University at Buffalo, the State University of New York, Buffalo, NY 14260, USA*)

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