21 fJ/step OTA-Less, Mismatch-Tolerant Continuous-Time VCO-Based Band-Pass ADC

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Abstract—A continuous-time band-pass (BP) delta–sigma (DS) analog-to-digital converter (ADC) is presented in this letter. The proposed BP ADC has four time-interleaved (TI) sub-ADCs that use ring oscillators as phase-domain integrators to achieve second-order noise shaping. The proposed BP-ADC architecture ensures that spurious tones due to mismatch between sub-ADCs fall out of the signal band and also have intrinsic interferer rejection capability. A prototype ADC fabricated in 65-nm CMOS is operated at an IF of 52 MHz. The ADC has SNDR of 63.1 and 59.5 dB at 1.04 and 4.3-MHz bandwidth, respectively. The ADC consumes only 0.36-mW power from a 0.9-V supply and has an energy efficiency of 21 fJ/step improving upon the current state of the art by 3.5×.

Index Terms—Analog-to-digital converter (ADC), band-pass (BP) delta–sigma (DS), time interleaved (TI), voltage-controlled oscillator (VCO).

I. INTRODUCTION

Continuous-time band-pass delta–sigma modulators (CTBPDSMs) are an attractive solution for digitizing RF signals at an intermediate frequency (IF) and reduces the complexity of the receiver chain [1]. Existing CTBPDSMs are conventionally designed using LC [2] or RC-based resonators [1], [3]. LC resonators typically consume large chip area, while RC resonators consume large power due to the use of OTAs. While ring voltage-controlled oscillator (VCO) has emerged as a low-power alternative to the active integrator for low-pass continuous-time (CT) delta–sigma modulators (DSMs) thanks to advanced design techniques and technology scaling, similar VCO-based solutions are still lacking for CTBPDSMs.

In this letter, we present a CTBPDSM which time interleaves four second-order, closed-loop VCO-ADCs to allow band-pass (BP) operation, and consumes only 21 fJ/conversion step. The proposed CTBPDSM does not require calibration for VCO nonlinearity or channel mismatch. Compared to conventional resonator-based BPDSM in which the center frequency is sensitive to variations in loop coefficients, the proposed architecture is immune to shifts in center frequency since the center frequency depends only on the sampling clock frequency and the number of sub-ADCs. The CTBPDSM is implemented in a 65-nm CMOS process and has power consumption of only 0.36 mW. The measurement results demonstrate the feasibility of designing high-energy efficiency CTBPDSMs using ring VCOs. The remainder of this letter is organized as follows. Section II presents the architecture of the proposed BP $\Delta\Sigma$ analog-to-digital converter (ADC) and design details, and measurement results on the prototype are presented in Section III.

II. PROPOSED ARCHITECTURE

A. CTBPDSM Architecture

Fig. 1 shows the high-level architecture and die photograph of the proposed CTBPDSM. Four second-order CT VCO-based sub-ADCs are time interleaved (TI) for generating a BP transfer function [4]. Each sub-ADC runs at $f_s = 52$ MHz, while the overall TI-ADC runs at 208 MHz. While each sub-ADC has an NTF proportional to $(1 - z^{-1})^2$, the TI-ADC has an NTF proportional to $(1 - z^{-4})^2$ since even though the TI-ADC runs 4× faster, the relationship between quantization error of adjacent samples in each sub-ADC is preserved [5]. Thus, the TI-ADC has notches in the NTF at 0, 52 MHz, and 104 MHz. Since each sub-ADC is a CTDSM, the inherent anti-aliasing will reject input signals at 52 and 104 MHz bands. Instead of sampling the input signal, as in [6], the input signal is downconverted through passive mixers driven by 25% duty cycle LO pulses before sending to the sub-ADCs as shown in Fig. 1. The LO pulses required to drive the passive mixers are created by synchronous division-by-4 of a master clock running at 208 MHz. Passive mixing retains the CT nature of the TI-ADC and reduces power consumption as the input buffer does not need to drive sampling capacitors as in DT ADC. The tradeoff with having CT ADC is reduced SNR due to gain attenuation from the passive mixer. Another disadvantage associated with having a mixer in front of ADC is downconversion of signals around multiples of LO to the signal band. The proposed architecture has intrinsic image rejection capability and does not require an image-reject filter as in conventional "mixer-followed-by-ADC" architecture, as will be shown later.

The outputs from each sub-ADC are sampled on rising edges of the LO pulses and combined using a multiplexer to form the overall TI-ADC output. The output of the ith mixer ($i \in [1, 4]$) can be written in the frequency domain as

$$X_i(f) = V_{\text{in}}(f) \circledast S(f)$$
$$= \sum_{k=-\infty}^{\infty} Ac_k[\delta(f - kf_s - f_{\text{in}})]e^{-j\pi(i-1)fT_s/2} \quad (1)$$

where V_{in} is the analog input to the mixer and can be written as $V_{\text{in}}(f) = A[\delta(f - f_{\text{in}}) + \delta(f + f_{\text{in}})]$, $S(f) = \sum_{k=-\infty}^{\infty} c_k\delta(f - kf_s)$ is the frequency response of the LO pulse, and the delay term $e^{-j\pi(i-1)fT_s/2}$ is due to the ith mixer receiving LO pulse delayed by $(i-1)T_s/4$ as shown in Fig. 1. The mixer outputs go on to the sub-ADCs which anti-alias filter the mixer output with second-order sinc function, before quantizing it. The ith ADC output can be written as

$$D_i(f) = X_i(f) \circledast \sum_{m=-\infty}^{\infty} \delta(f - mf_s)e^{-j\pi(i-1)fT_s/2}$$
$$= \sum_m \sum_k Ac_k\delta(f - (k+m)f_s - f_{\text{in}})e^{-j\pi(i-1)fT_s/2}. \quad (2)$$

Fig. 1. Architecture and die photograph of the proposed CTBPDSM.

Fig. 2. Signal-processing view of how the proposed CTBPDSM works. The signals in gray are attenuated/canceled by the architecture.

The sub-ADC outputs have tones at $\{(k + m)f_s + f_{in}\}$. Once the sub-ADC outputs are combined together using a multiplexer, which is equivalent to addition for the discrete-time sampled outputs, all the tones corresponding to $(k + m) \neq 0$ are canceled if the sub-ADCs are perfectly matched, and the input is perfectly reconstructed at the output.

Fig. 2 shows a signal processing view of the ADC operation for $f_{in} = f_s + \Delta f$. The mixing operation creates replicas of the input signal. All the replicas, except those in the baseband, are attenuated by intrinsic anti-aliasing of the CT sub-ADCs, and are shown in gray. After sampling, each sub-ADC has a tone at $f_s + \Delta f$ and a replica at $f_s - \Delta f$. If the sub-ADCs are all perfectly matched, the replicas are canceled. In practice, mismatches between the sub-ADCs limit cancellation of the replica tones. In this design, the ADC bandwidth is set to $f_s \rightarrow f_s + f_B$ such that replica tones due to sub-ADC mismatches fall out of the band. Thus, even in the presence of mismatches between sub-ADCs, the in-band SNDR is not affected and
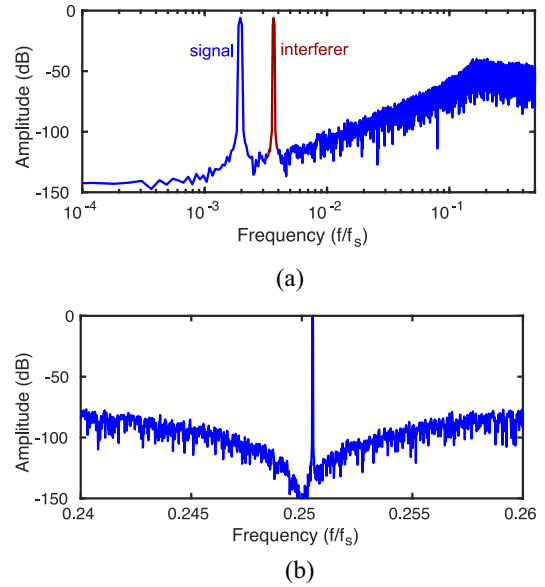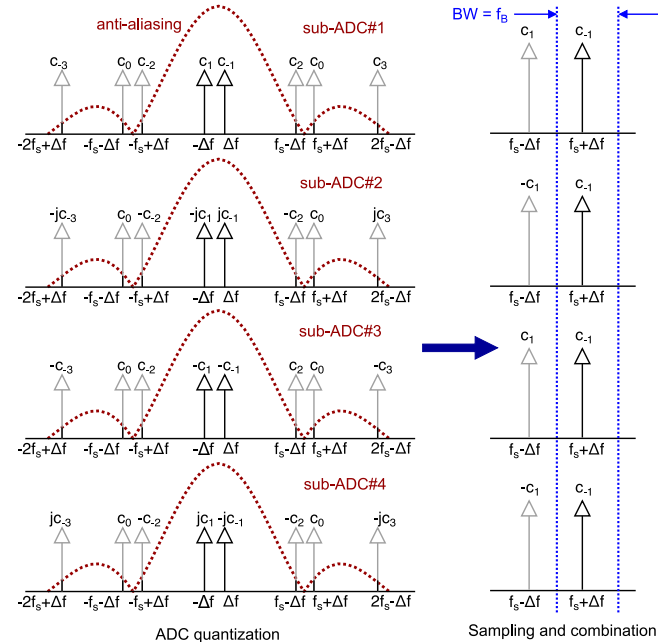

Fig. 3. Simulated FFT of (a) sub-ADC with interferer and (b) CTBPDSM showing intrinsic interferer cancellation.

no calibration/correction is required for mismatch correction unlike in Nyquist TI ADCs. The tradeoff involved in selecting the ADC bandwidth from $f_s \rightarrow f_s + f_B$ instead of $f_s - f_B/2 \rightarrow f_s + f_B/2$ is reduction in SQNR by 12 dB.

For an interferer close to multiples of f_s, the front-end passive mixer will downconvert the interferer to in-band, but the interferer gets canceled once the outputs from the sub-ADCs are combined if all the sub-ADCs are perfectly matched. The intrinsic interference cancellation is shown in Fig. 3. An input signal close to $f_s/4$ and an interferer close to $f_s/2$ are applied to the ADC. The passive mixer downconverts both signal and interferer to the signal band as shown in the FFT plot of single sub-ADC [see Fig. 3(a)]. Once the outputs of the sub-ADCs are combined, the interferer is completely canceled as shown in the FFT plot of CTBPDSM [see Fig. 3(b)]. Mismatches between sub-ADCs will limit interferer rejection, but this can be corrected through foreground gain mismatch calibration of the sub-ADCs.

B. Sub-ADC Circuit

Fig. 4 shows the circuit schematic of a single sub-ADC. The sub-ADC is based on the architecture of VCO-ADC reported in [7]. The sub-ADC consists of two VCO integrators in a single loop which results in second-order quantization noise shaping. The negative feedback loop and multielement DAC reduce the signal swing seen by the first VCO integrator which relaxes the linearity requirement of the first VCO and obviates the need for nonlinearity calibration. The second VCO integrator switches between only two frequencies and, thus, has very high linearity. The voltage input is converted to the current through a pMOS gm-stage as shown in Fig. 4. A pMOS current DAC is used to bias the first VCO integrator unlike an nMOS DAC in [7]. This is because a pMOS DAC reuses the DAC current for biasing the first VCO integrator which saves power compared to nMOS DAC which sinks current away from the VCO. Since SNR of our prior ADC [7] was limited by the thermal noise of the first VCO integrator, we have reduced sampling frequency, and VCO center frequency proportionally, which reduces power while preserving SNR in thermal noise limited regime. Excess loop delay (ELD) is countered through proper design of the VCO tuning gains, and as
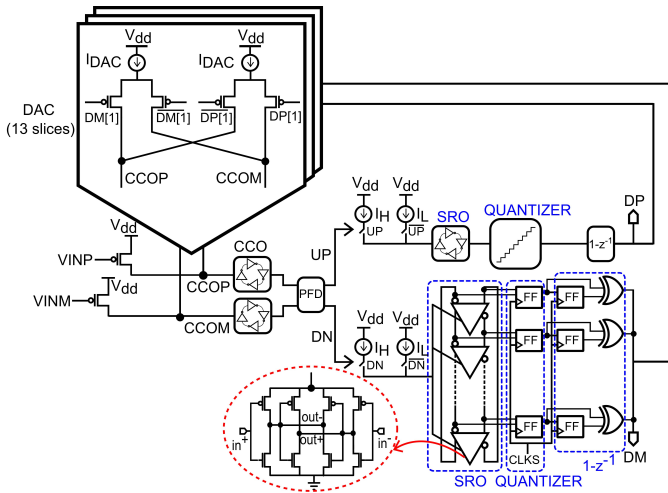
Fig. 4.   Schematic of sub-ADC circuit.

shown in [7], the sub-ADC can tolerate up to 1 sampling period delay without ELD compensation. Compared to existing BP ADCs with OTAs, the sub-ADC has a simple structure with a single DAC and is easier to design in scaled CMOS technologies.

The VCOs in the sub-ADC integrate the input signal for 25% of the sampling period, and for the remaining 75% of the sampling period, the sub-ADC inputs are tied to common-mode voltage. The common-mode voltage is selected to let the VCOs run at a low frequency which saves power and reduces noise during the sub-ADC idle phase. The simulated SNDR is greater than 69 dB as long as the random jitter is less than 10 ps. The post-layout simulated jitter in the clock generator is 8 ps.

III. MEASUREMENT RESULTS

Fig. 5(a) shows the zoomed-in FFT of the CTBPDSM for IF = 52 MHz for input frequencies of 180 and 890 kHz. Replica tones and offset arising due to mismatch between the sub-ADCs fall outside the signal bandwidth (highlighted in black) and the in-band noise floor is shown in the inset. Fig. 5(b) shows measured SNDR versus input frequency. Fig. 6(a) shows measured dynamic range of the CTBPDSM for 52 MHz IF. The ADC has a dynamic range greater than 66 dB. The dynamic range is limited by attenuation and thermal noise from the passive mixer as well as ADC quantization noise. Fig. 6(b) shows the Walden FoM, BP FoM [8], and Schreier FoM versus bandwidth at 52 MHz IF. The best Walden and BP FoM are obtained for BW of 4.3 MHz. The ADC bandwidth can be extended by scaling up the sampling frequency, and power consumption, since the VCO bias currents and DAC current need to be increased linearly with sampling frequency to keep the loop gain unchanged. Since the VCO will run at higher frequency with increased bias current, its thermal noise will increase and the input signal swing needs to increase proportionally to maintain the same SNR. Ultimately, nonlinearity due to increase in input swing will limit the maximum sampling frequency and bandwidth of the ADC. Fig. 7 shows the two-tone test spectrum for the BP ADC with one tone at 220 kHz and another tone at 234 kHz offset from 52 MHz. The measured IM3 components are shown in Fig. 7. Fig. 8(a) shows the measured intrinsic interferer rejection of the proposed ADC. A signal at 52.22 MHz and interferer at 300 kHz, which is 3 dB below the signal, are given as input to the ADC. Both the signal and interferer appear in-band at the sub-ADC, but the interferer is suppressed by 56 dB at the overall ADC output. Fig. 8(b) shows measured interferer rejection
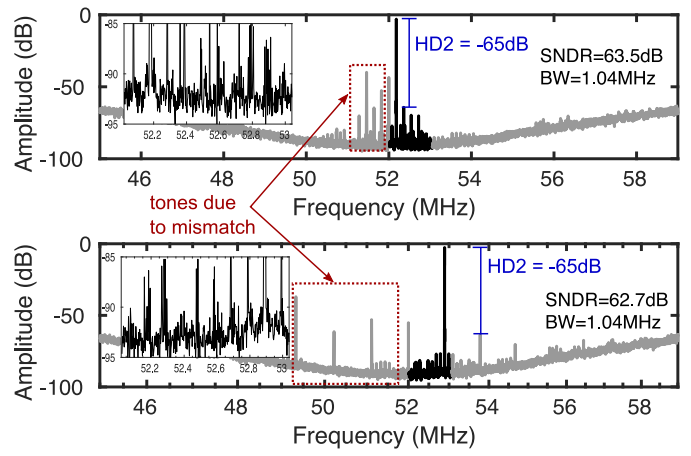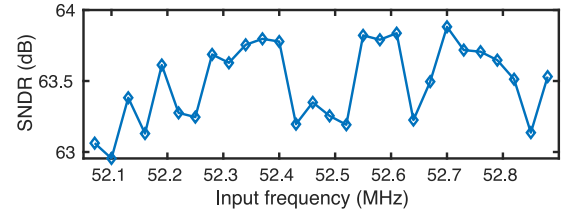
Fig. 5.   (a) Measured 2^{16} point FFTs of CTBPDSM for 180 and 890 kHz inputs and (b) SNDR versus input frequency.
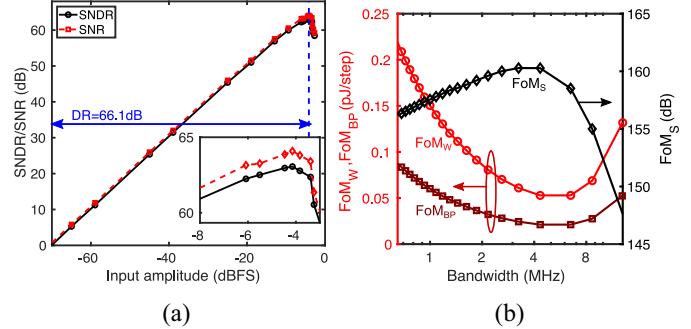

Fig. 6.   (a) Measured DR and (b) FoM versus ADC bandwidth for 52 MHz IF.
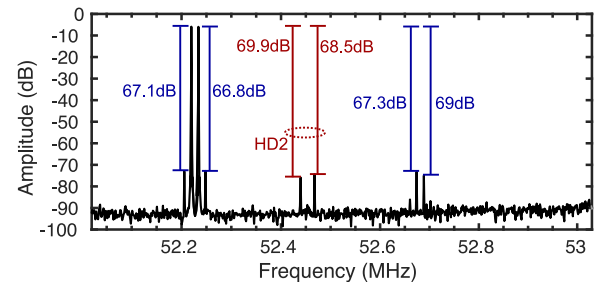

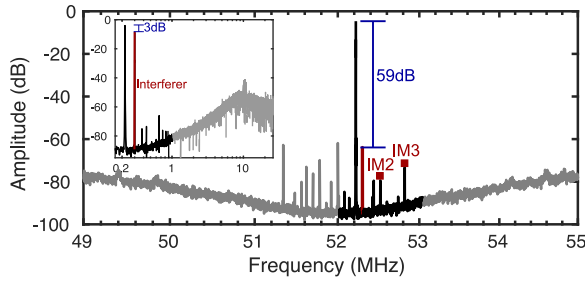Fig. 7.   Measured 2^{16} point two-tone test spectrum.

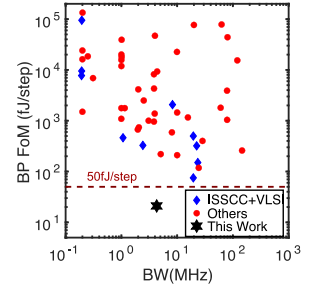ratio (IRR) as a function of interferer frequency with the input fixed at 52.22 MHz.

Table I compares the performance of the proposed ADC with state-of-the-art BP $\Delta\Sigma$ ADCs. The proposed ADC has the lowest power consumption of 0.36 mW thanks to the highly digital and OTA-less nature of each sub-ADC. The proposed ADC has 3.5× better BP energy efficiency FoM$_{\mathrm{BP}}$ compared to state
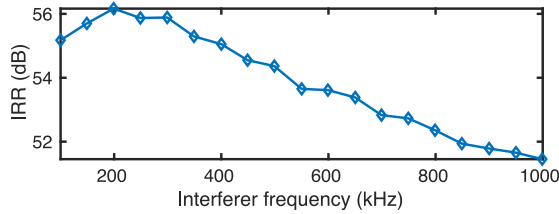
TABLE I
COMPARISON WITH STATE-OF-THE-ART BP $\Delta\Sigma$ ADCs

	Process (nm)	Area (mm^2)	f_s (MHz)	IF (MHz)	Power (mW)	BW (MHz)	SNDR (dB)	FoM$_{BP}$[1] (pJ/step)	FoM$_w$ (pJ/step)	FoM$_s$ (dB)
VLSI'09 [5]	65	0.7	4000	1000	19.6	1	41.5	40	99.4	118.6
ISSCC'12 [2]	40	0.4	3200	750	20	20	70	0.078	0.19	160
JSSC'13 [3]	65	0.55	100	25	13	4	55	1.39	3.46	139.9
RFIC'14 [9]	65	0.39	345	6	6.3	10	63.9	0.22	0.24	155.9
TCAS-I'15 [8]	180	0.55	200	50	2	2	50.2	0.74	1.86	140.2
JSSC'16 [1]	65	0.25	800	200	35	25	69	0.12	0.3	157.5
JSSC'19 [10]	40	0.01	4000	1000	16	100	49	0.14	0.34	146.9
This Work	**65**	**0.18**	**208**	**52**	**0.36**	**1.04**	**63.1**	**0.057**	**0.14**	**157.7**
						4.3	**59.5**	**0.021**	**0.053**	**160**

[1]FoM$_{BP}$ = Power/($2^{ENOB} \times 2$BW)/($1+(6 \times$IF/f_s)) [8]

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Fig. 8. (a) Measured 2^{16} point FFT showing interferer rejection and (b) interferer rejection as function of interferer frequency.

of the art. FoM$_{BP}$ is a modified version of Walden FoM for BP ADCs and takes the ratio of IF to f_s into account [8]. While [2] has higher SNDR and BW, the power consumption of our design is 55× lower than that of [2] which results in better FoM.