8.6fJ/step VCO-Based CT 2^{nd}-Order $\Delta\Sigma$ ADC

Akshay Jayaraj*, Abhijit Das†, Srinivas Arcot* and Arindam Sanyal*
*Electrical Engineering, University at Buffalo, Buffalo, NY 14260, USA.
†Texas Instruments, Dallas, TX 75243, USA.
Email: akshayja@buffalo.edu, arindams@buffalo.edu.

***Abstract*—A purely VCO-based continuous-time (CT), single-loop second-order $\Delta\Sigma$ ADC is proposed in this work. Two ring oscillators are used as integrators to perform second-order quantization noise shaping. The proposed CT ADC does not require additional circuit for excess loop delay compensation. A current-reuse DAC architecture is proposed to simultaneously reduce ADC noise and power consumption. A 65nm prototype consumes 105μW from 1V supply at sampling frequency of 32.6MHz, and achieves a walden FoM of 8.6fJ/step over 2.3MHz bandwidth, which is the best among current CT $\Delta\Sigma$ ADCs.**

***Index Terms*—voltage-controlled oscillator, analog-to-digital converter, delta-sigma, continuous-time ADC**

I. Introduction

Voltage-controlled oscillator (VCO) based analog-to-digital converters (ADCs) are a popular choice for data conversion in advanced CMOS technologies. This is because VCOs are highly digital in nature and can perform simultaneous integration and multi-bit quantization with first-order noise shaping. While VCO-ADC comes with lot of inherent advantages, VCO is highly nonlinear and sensitive to variations in process, voltage and temperature (PVT). Previous attempts to linearize VCO-ADC have embedded the VCO inside a loop with high gain op-amp based loop filter, employed digital calibration of open-loop VCO [1] or used a two-stage architecture [2]. Recent continuous-time (CT) purely VCO-ADCs have used single-loop $\Delta\Sigma$ architecture to suppress VCO nonlinearity and reduce susceptibility to PVT variation [3], [4]. The higher-order VCO-ADCs in [5], [6] have used an open-loop VCO followed by a second-order VCO-based single-loop $\Delta\Sigma$ to achieve third-order quantization noise shaping.

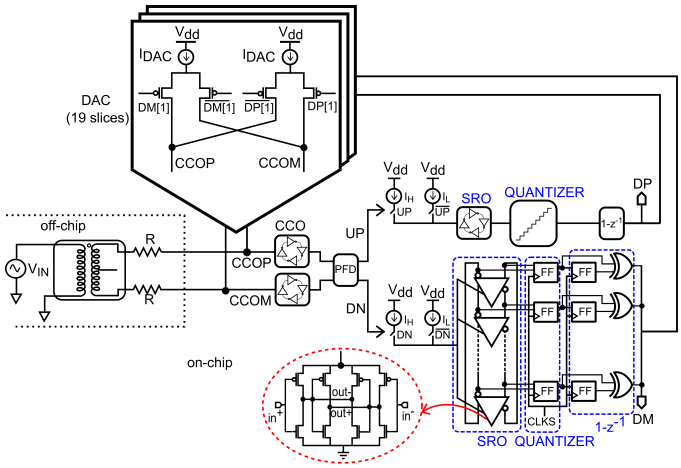
This work presents the first CT $\Delta\Sigma$ VCO-ADC to exhibit *sub-10fJ/step walden FoM*. The second-order ADC consists of two VCO integrators in a feedback loop. While the ADC is based on the modified DPLL architecture reported in [7]–[9], a current-reuse DAC and optimized design methodology is used in this work to reduce walden FoM by $17\times$ compared to our previous prototype [9], and $4\times$ compared to the second-order VCO-ADC in [10]. The rest of this paper is organized as follows: Section II presents the proposed ADC architecture and design optimization methodology, measurement results are presented in Section III and the conclusion is brought up in Section IV.

II. Proposed Architecture

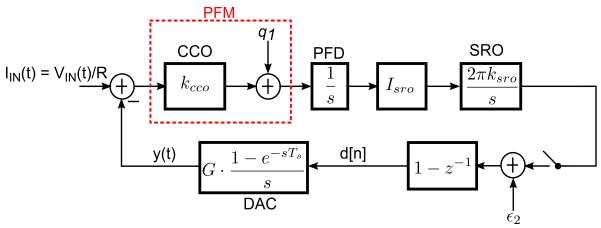
A. ADC Circuit and Model

Fig. 1(a) shows the circuit schematic of the proposed ADC. Analog voltage input, V_{IN}, is converted to current, I_{IN}, through two off-chip resistors, R, before entering the ADC. A tri-state phase/frequency detector (PFD) extracts phase difference of the input current-controlled oscillators (CCOs). The PFD provides two 1-b outputs 'UP' and 'DN' such that the difference in widths of 'UP' and 'DN' pulses encodes the phase difference of the input CCOs. The 1-b 'UP' and 'DN' pulses drive the second CCO integrators such that they switch between only 2 frequencies f_H and f_L corresponding to currents I_H and I_L (see Fig. 1(a)). Hence, the second CCO integrators act as switched ring oscillators (SROs). Since the SROs switch between 2 frequencies, they have very high linearity. Both CCO (first integrator) and SRO are built using a chain of 19 pseudo-differential inverters as shown in Fig. 1(a). Use of dual CCO architecture in combination with pseudo-differential inverter stages reduce even-order distortion and improve common-mode rejection and power-supply rejection [9]. The SRO output is digitally differentiated using XOR gates and unit delay, which implements $1 - z^{-1}$, and fedback to the CCO input using a multi-element current steering non-return-to-zero (NRZ) DAC. Digital differentiation using XOR naturally scrambles the element selection pattern of the DAC such that its static mismatch is first-order shaped.

Fig. 1(b) shows the mathematical model of the proposed ADC. A single-ended model is shown for sake of simplicity. In order to mathematically analyze the ADC, we use pulse-frequency modulation (PFM) [9] model for CCO+PFD which operate in continuous-time. In the PFM model, the CCO acts as a pulse frequency encoder which encodes phase information in rising edges of the CCO output. The PFD integrates the dirac-delta impulses which correspond to the timing instants when CCO phase crosses 2π, and converts the PFM output into a pulse-width modulated output [9]. As shown in [9], the PFM signal contains i) a dc term proportional to CCO center frequency, f_{cco} ii) the input signal multiplied by CCO tuning gain, k_{cco} and iii) distortion terms with modulation side-bands centered around harmonics of f_{cco}. The PFM distortion terms is denoted by q_1 in Fig. 1(b). Since sampling happens immediately after the SRO, the SRO is modeled as a phase domain integrator rather than PFM encoder [9]. The SRO has a transfer function of $2\pi k_{sro}/s$. The feedback NRZ DAC has



(a)



(b)

Fig. 1: (a) Circuit schematic of the proposed ADC (b) mathematical model

a gain of G and I_{sro}=$I_H - I_L$. SRO quantization noise is modeled by ϵ_2. The ADC output can then be written as

$$d = \left[I_{IN}H_1(s)\frac{(1-e^{-sT_s})^2}{(sT_s)^2}\right]^* + \epsilon_2 NTF_2(z) + \left[q_1\frac{H_1(s)}{k_{cco}}\frac{(1-e^{-sT_s})^2}{(sT_s)^2}\right]^* \quad (1)$$

where $H = 2\pi k_{cco}k_{sro}I_{sro}$, $[]^*$ denotes sampling operation and T_s is the sampling period. $H_1(s)$ and NTF_2 are given by

$$H_1(s) = \frac{2HT_s^2}{2 + (GHT_s^2 - 2)\,e^{-sT_s} + (GHT_s^2)e^{-2sT_s}} \quad (2)$$

$$NTF_2(z) = \frac{2(1-z^{-1})^2}{2 + (GHT_s^2 - 2)\,z^{-1} + (GHT_s^2)z^{-2}} \quad (3)$$

It can be seen from (1) that the ADC input and PFM tones are second-order sinc-filtered before sampling. Since the PFM tones are centered around f_{cco}, they can be adequately suppressed by setting f_{cco}=f_s (f_s=$1/T_s$). However, without background calibration, it is hard to ensure f_{cco}=f_s across PVT variations and small drift in f_{cco} will alias PFM tones into signal-band and degrade ADC SNDR [9]. We set f_{cco} to $1.25f_s$ instead such that PFM tones alias mostly out-of-band and does not degrade ADC SNDR.

B. Design Optimization

The design trade-offs between noise, power and bandwidth (BW) for the proposed ADC are tightly coupled through the parameters N, I_{DAC} and T_s which are optimized for maximum energy efficiency. In order to reduce energy consumption, current in the feedback DAC is re-used to bias the first CCO integrator as shown in Fig. 1(a). The PMOS DAC supplies the differential CCOs with currents given by $\{I_{DAC}(N + DP[n] - DM[n])\}$ and $\{I_{DAC}(N + DM[n] - DP[n])\}$ in the n-th cycle. Thus, center frequency of the CCOs, f_{cco}, is set by $N \cdot I_{DAC}$. The proposed current-reuse DAC architecture results in both lower noise and power consumption than the ADCs which use a PMOS current source to bias the CCO and an NMOS DAC for feedback [4], [9], [10]. Since the PMOS current source in [9], [10] contributes to a significant fraction (28%) of overall thermal noise, its absence in the proposed architecture reduces noise. Also, re-using the DAC current for CCO bias reduces current consumption by $N \cdot I_{DAC}$. Thus, the proposed architecture can achieve higher energy efficiency compared to [9], [10].

In order to further increase energy efficiency, we need to reduce thermal noise from CCO and DAC, as well as reduce overall power consumption. Thermal noise from SRO is first order high-pass shaped and is not a significant contributor to overall noise.

Input referred thermal noise due to the DAC is given by

$$\sqrt{\overline{i_{dac,n}^2}} = \sqrt{2}\cdot\sqrt{N\cdot 4kT\gamma g_m\cdot f_B} \quad (4)$$

where g_m denotes transconductance of unit DAC current source, f_B is the ADC bandwidth and the factor of $\sqrt{2}$ in (4) accounts for the differential DACs. g_m is directly proportional to I_{DAC} and the input referred DAC noise increases linearly with $\sqrt{N \cdot I_{DAC}}$.

The input-referred thermal noise due to CCO is given by

$$\sqrt{\overline{i_{cco,n}^2}} = \sqrt{2}\cdot\frac{\sqrt{2DT_s}}{2\pi k_{cco}T_s}\cdot\frac{1}{\sqrt{OSR}} \quad (5)$$

where D is phase diffusion constant given by D=$\mathcal{L}(\Delta\omega)\cdot(\Delta\omega)^2/2$ where $\mathcal{L}(\Delta\omega)$ is the phase noise at an offset frequency of $\Delta\omega$. Input-referred CCO thermal noise is proportional to f_{cco}, and hence, $N \cdot I_{DAC}$.

The input-referred quantization noise is given by

$$\sqrt{\overline{i_{q,n}^2}} = \frac{I_{DAC}}{\sqrt{12}}\cdot\frac{\pi}{\sqrt{5}}\cdot(OSR)^{-5/2} \quad (6)$$

From (4) and (5), it can be seen that reducing $N \cdot I_{DAC}$ reduces ADC input-referred thermal noise. However, reducing $N \cdot I_{DAC}$ alone does not improve SNR since input swing is also reduced proportionally. In addition, reducing $N \cdot I_{DAC}$ reduces the DAC gain, G, which can in turn reduce ADC SNR [9]. Thus, to keep the ADC open-loop gain unchanged, reduction in $N \cdot I_{DAC}$ is accompanied by increase in T_s which further reduces input referred CCO thermal noise (see (5)) as well as ADC power consumption. Hence, reduction in $N \cdot I_{DAC}$ and simultaneous increase in T_s increases ADC energy efficiency. However, for a given ADC bandwidth, T_s cannot be set too high as quantization noise will limit ADC SNR and energy efficiency. To find an optimum ADC sampling frequency, we sweep f_s and scale $N \cdot I_{DAC}$, I_{sro} and input swing by the

same factor as f_s. Fig. 2 shows the ADC input referred thermal noise, quantization noise and SNR as function of f_s for BW of 1.5MHz. Thermal noise is calculated from SPICE noise simulations on DAC and CCO. At low f_s, quantization noise limits ADC SNR, while at high f_s, thermal noise limits ADC SNR. At f_s=32MHz, thermal noise and quantization noise are almost equal. Hence, f_s is set to 32MHz for maximum energy efficiency (walden FoM), and the corresponding $N \cdot I_{DAC}$ is 15μA.

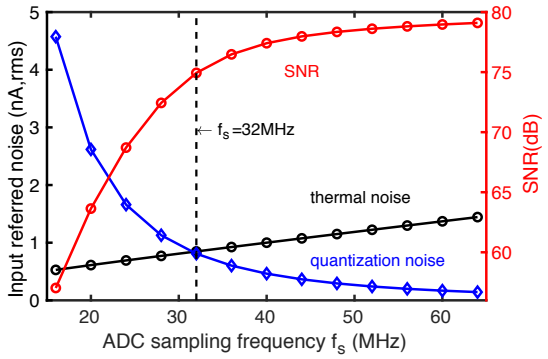


Fig. 2: ADC noise and SNR versus f_s

For a given $N \cdot I_{DAC}$, optimum value of N is decided by quantization noise. If N is very small, in-band quantization noise dominates in-band thermal noise, while for very large N, in-band quantization noise is much smaller than in-band thermal noise. Fig. 3 shows the ADC input referred thermal noise, quantization noise and SNR as function of N for BW of 1.5MHz, f_s=32MHz and input current amplitude of 18.5μA (pk-pk). The product of $N \cdot I_{DAC}$ is kept constant as N is swept. Fig. 3 shows that for N=18, quantization noise and thermal noise are almost equal. We choose N=19 for this design for an SNR of 74.9dB. The current-reuse DAC architecture as well as the optimum choice of N, I_{DAC} and f_s results in 17× better energy efficiency than our first prototype [9].

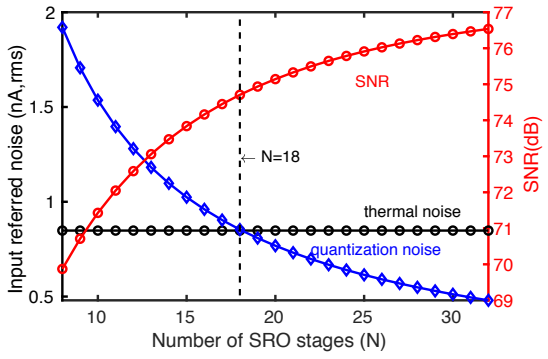


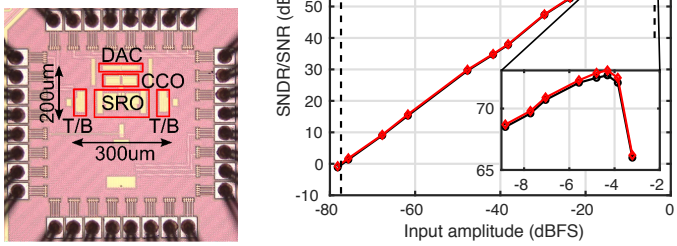
Fig. 3: ADC noise and SNR versus N

Excess loop delay (ELD) in CT $\Delta\Sigma$ ADC can de-stabilize the system by introducing additional poles to ADC transfer function. Typically, ELD is compensated by adding another DAC around the quantizer. For the proposed ADC, ELD is compensated without additional DAC by judiciously selecting the CCO and SRO gains during the design phase. As shown in [9], the CCO and SRO gains are set to ensure that the ADC can tolerate an ELD of upto 1 sampling period even if CCO, SRO gains vary by $\pm 10\%$ due to PVT variations.

III. Measurement Results

A prototype ADC is fabricated in 65nm CMOS process and Fig. 4(a) shows the die microphotograph. The ADC core occupies an area of 0.06mm^2 and runs from a power supply of 1V. The ADC output is converted from thermometer-to-binary (T/B) code before being brought off-chip. I_{DAC} is set to 0.8μA for this design. The ADC consumes 105μW power at f_s=32.6MHz. Fig. 4(b) shows the measured SNR and SNDR versus input amplitude at a BW=1.5MHz. The ADC has a measured dynamic range of 74dB.

Fig. 5 shows the measured ADC spectrum for an input frequency of 50kHz and amplitude of -5dBFS. Analog voltage input is converted into current input through off-chip 6kΩ resistors. The ADC has an SNDR of 72.7dB and SFDR of 81dB for BW=1.5MHz without any calibration.



(a) (b)

Fig. 4: (a) Die micro-photo (b) ADC dynamic range plot

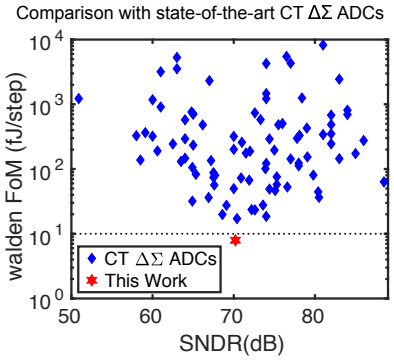
Fig. 6 shows the measured schreier and walden FoM versus BW for the ADC. The ADC achieves 174.2dB schreier FoM at 1.5MHz BW and 8.6fJ/step walden FoM at 2.3MHz BW Fig. 7 shows the measured SNDR of the ADC versus input frequency at BW=1.5MHz. The ADC SNDR varies between 72-73dB as input frequency is varied from 10-100kHz. Fig. 8 shows the measured SNDR for five chips at BW of 1.5MHz across power supply of 0.9-1.1V and temperatures from 0-50C. The ADC maintains high SNDR ($>$ 70dB) across VT corners without calibration.

Table I compares the fabricated ADC with state-of-the-art CT $\Delta\Sigma$ VCO-ADCs with similar bandwidths. The proposed ADC achieves the lowest walden FoM of 8.6fJ/step at BW=2.3MHz and lowest power consumption of 105μW. Thanks to the optimized design procedure, the proposed ADC has high SNDR even at small OSR. The figure next to Table I compares walden FoM of the proposed ADC with state-of-the-art CT $\Delta\Sigma$ ADCs. The proposed ADC has the lowest walden FoM among reported CT $\Delta\Sigma$ ADCs.

TABLE I: Comparison with state-of-the-art CT ΔΣ VCO-ADCs.

	Process (nm)	Area (mm^2)	Fs (MHz)	Power (mW)	BW (MHz)	SNDR (dB)	FoM_w (fJ/step)[1]
JSSC'10 [1]	65	0.075	1300	11.5	5.08	75	246
ESSCIRC'16 [3]	130	0.13	250	1.05	3	70.2	66.2
JSSC'17 [5]	65	0.01	1000	1.5	10	55.1	158
VLSIC'17 [11]	40	0.028	330	0.5	6	68.6	19.8
ASSCC'18 [10]	40	0.086	260	0.91	5.2	69.6	34.7
TCAS–I'19 [9]	65	0.06	205	1	2.5	64.2	150.9
This Work	**65**	**0.06**	**32.6**	**0.1**	**1.5**	**72.7**	**9.9**
					2.3	**70.2**	**8.6**

[1] FoM_w = Power/(2^{ENOB}x2BW)



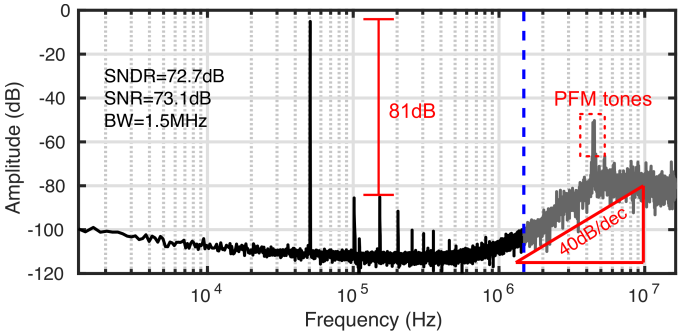


Fig. 5: Measured FFT for 50kHz input

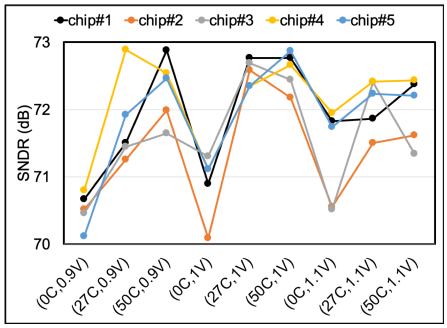


Fig. 8: Measured ADC SNDR across VT corners for 5 chips

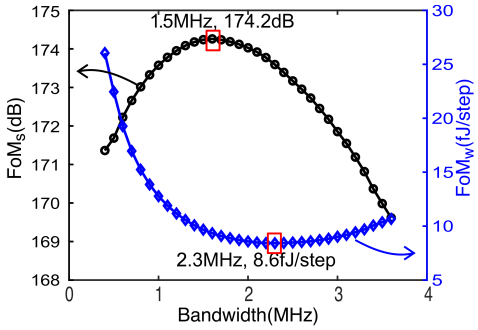


Fig. 6: Schreier and walden FoM vs BW

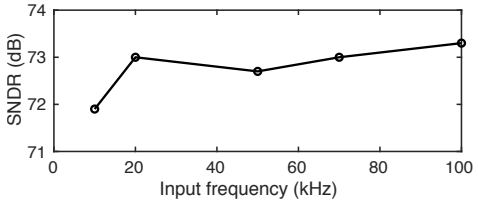


Fig. 7: Measured SNDR vs input frequency

IV. Conclusion

A second-order purely VCO-based CT ΔΣ ADC is presented in this work. A 65nm prototype achieves a walden FoM of 8.6fJ/step which is the lowest among state-of-the-art CT ΔΣ ADCs. Energy efficiency of the ADC is expected to improve further with CMOS technology scaling.

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