

8fJ/Step Bandpass ADC With Digitally Assisted NTF Re-Configuration

Sanjeev Tannirkulam Chandrasekaran¹, *Graduate Student Member, IEEE*,
Gaurav Kapoor, and Arindam Sanyal², *Member, IEEE*

Abstract—In this work we propose a single channel band-pass (BP) SAR ADC with dynamic noise transfer function (NTF) re-configuration. The proposed ADC employs a low-power two-stage architecture. After the SAR finishes quantization, the residue is extracted by firing the comparator multiple times. An estimate of the residue is obtained by employing a maximum likelihood based estimator (MLE). The output of the ADC is obtained by subtracting a delayed version of the estimated residue from the SAR output thus generating a complex NTF with multiple notches in the spectrum. A 65nm ADC prototype achieves 74.1/78dB SNDR/DR over a 101.2kHz bandwidth while consuming 17 μ W from a 1V supply at 2.43MS/s. The ADC core occupies an area of 0.12mm². The ADC achieves 8fJ/c-step bandpass FoM which is 85 \times better than state-of-the-art BP ADCs with similar bandwidth and 8.7 \times better than all reported state-of-the-art BP ADCs.

Index Terms—Complex NTF, band-pass analog-to-digital converter, SAR, NTF re-configuration.

I. INTRODUCTION

BANDPASS (BP) ADCs are a subset of $\Delta\Sigma$ ADCs for which zeros of the noise transfer function (NTF) are distributed from 0 to $f_s/2$ (f_s being the sampling frequency), rather than being concentrated at/near dc as in low-pass (LP) $\Delta\Sigma$ ADC. Thus, BP ADCs exhibit a complex NTF with multiple notches, and they can directly quantize analog signals centered around an intermediate frequency (IF) rather than being converted to base-band. Thus, BP ADCs find applications in low-IF receivers with better immunity against $1/f$ noise than direct down-conversion receivers. Conventional BP ADC architectures employ high-gain OTA based RC/LC resonators to implement the complex NTF [1]–[6]. High gain OTAs are challenging to design in an energy efficient manner at advanced CMOS technology nodes due to simultaneous reduction in both transistor intrinsic gain and supply voltage. The authors in [1] present an active RC resonator based

fourth order continuous-time (CT) BP $\Delta\Sigma$ ADC, while the works of [7]–[9] present active RC resonator based discrete-time (DT) BP $\Delta\Sigma$ ADC. Active RC/LC resonators occupy large silicon area and mismatches in passive components affect location of zeros in the NTF thus leading to variation in the pass-band of the BP ADC. References [5], [6] re-uses a single OTA between two resonators to save power but still has low energy efficiency and suffers from unwanted coupling between outputs of resonators sharing the same OTA. In addition, NTF of the BP ADC cannot be easily re-configured once implemented on silicon. Reference [10] proposed a re-configurable LP/BP $\Delta\Sigma$ ADC by physically re-configuring the circuitry from LP mode to BP mode. However [10] suffers from the same aforementioned drawbacks as it employs an OTA based loop filter. Reference [11] presents a band-pass ADC in which the center frequency can be re-configured by digitally changing the sampling and integrating capacitors, but uses power-hungry OTAs to realize loop filter.

A complex NTF can also be achieved by time-interleaving multiple low-pass $\Delta\Sigma$ ADCs. References [12], [13] presents a 8 \times discrete-time time-interleaved (TI) BP $\Delta\Sigma$ ADC. Each sub-ADC comprises an open-loop ring oscillator (RO) based $\Delta\Sigma$ ADC [14]–[18]. The RO provides inherent integration and quantization thus obviating the need for a high gain OTA. The highly digital nature of the RO ensures it is scaling friendly. However, TI ADCs suffer from timing and gain mismatch among the various channels of the ADC [19]. Hence, TI ADCs require power hungry buffers to meet stringent timing requirements or complex calibration circuitry which are non-trivial to implement. The open loop nature of the RO implemented in [12] also limits dynamic range of the ADC owing to inherent non-linearity of the RO. In addition, tuning gain of an RO also suffers from variations due to process, voltage, and temperature (PVT) and further exacerbates the drawbacks of RO-based TI BP ADC. Reference [20] proposes a similar 8 \times DT TI nyquist RO based ADC using asynchronous counters and on-chip digital calibration circuitry for correcting mismatches present in the channel.

Error feedback (EF) is another technique which can be used to implement a complex NTF. Reference [21] implements a complex NTF using a 4-stage pipelined ADC. Residue from the final stage is delayed by 2 clock cycles and is added to the input of the ADC, thereby generating a $(1 + z^{-2})$ NTF with a notch at $f_s/4$. The 2 cycle delay is derived from the

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Sanjeev Tannirkulam Chandrasekaran and Arindam Sanyal are with the Department of Electrical Engineering, University at Buffalo, Buffalo, NY 14260 USA (e-mail: stannirk@buffalo.edu; arindams@buffalo.edu).

Gaurav Kapoor is with the Department of Electrical Engineering, University at Buffalo, Buffalo, NY 14260 USA, and also with Intel Corporation, Hillsboro, OR 97124 USA (e-mail: gauravka@buffalo.edu).

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implicit half-cycle delay contributed by the multiplying DAC (MDAC) from each pipelined stage. While [21] alleviates the drawbacks encountered in a TI BP ADC, it still requires high gain OTAs for inter-stage residue amplification. The addition of residue is implemented in the analog domain using switched capacitors, and in the presence of capacitor mismatch and OTA gain variation, the NTF of [21] changes to $(1 + k \cdot z^{-2})$ ($k \neq 1$) which can lead to significant degradation of SNR. Reference [21] employs calibration to correct the NTF.

In this work, we present a fully digital and re-configurable BP ADC that addresses limitations of existing BP ADCs. The proposed ADC uses a 10-bit successive approximation register (SAR) as the front-end and a stochastic maximum likelihood estimator (MLE) is used to quantize the SAR residue. A SAR architecture is selected since it is highly digital and has very high energy efficiency for medium resolutions [22], [23]. The MLE output is passed through a finite-impulse response (FIR) filter and subtracted digitally from the SAR output. This results in filtering of SAR thermal and quantization noise by $(1 - z^{-N})/2$ which creates $N/2 + 1$ notches between dc and $f_s/2$ with notches at both dc and $f_s/2$ while also attenuating MLE estimation error in the signal-band. Thus, the combination of nyquist ADC and stochastic estimator results in a BP-ADC. The proposed technique is highly digital, does not require OTAs, is robust against PVT variations, and does not need calibration. In addition, the NTF can easily be reconfigured by simply changing the number of cycles by which the MLE output is delayed before subtraction from SAR output. A test chip is fabricated in 65nm CMOS process and consumes only $17\mu\text{W}$ from 1V power supply while running at 2.43MHz. The test chip has $8.7\times$ better figure-of-merit (FoM) than state-of-the-art BP-ADCs. The rest of this paper is organized as follows: Section II presents the proposed architecture as well as discussion on the various non-idealities, Section III presents measurement results and finally, the conclusion is brought up in Section IV.

II. PROPOSED BAND-PASS ADC ARCHITECTURE

A. ADC Circuit

Fig. 1 shows circuit diagram and mathematical model of the proposed BP ADC. A single-ended model of the ADC is shown for simplicity even though the implemented circuit is differential. A 10-bit SAR ADC is used with bi-directional single-sided switching (BSS) [23], [24] technique that reduces DAC switching energy by 86% compared to conventional SAR switching. Bottom-plate switching is used to reduce signal-dependent charge injection into the capacitive DAC during sampling. A strong-arm latch is used as comparator. The parasitic capacitance at the input of the comparator is denoted by C_p in Fig. 1(a). The analog input V_{in} is sampled onto the capacitive DAC during ϕ_1 . The SAR ADC quantizes the analog input for 10 cycles, and the residue, V_{res} , is available at the comparator input nodes after quantization is complete. Since the ADC thermal noise randomizes V_{res} , if the comparator is fired multiple times, the comparator decisions can be used to form an estimate of V_{res} . There are many stochastic techniques to estimate value of a noisy signal, such

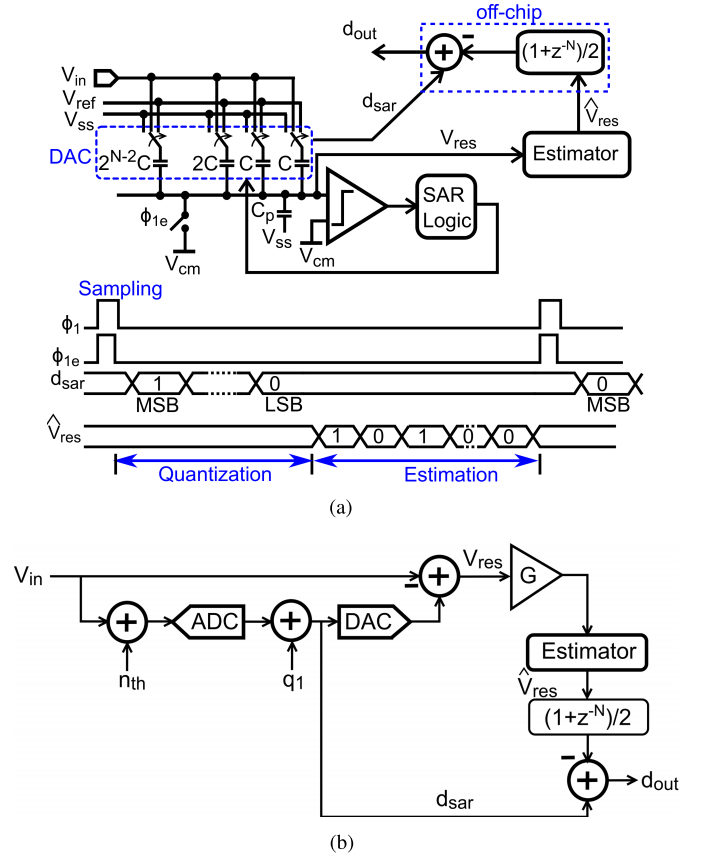


Fig. 1. (a) Circuit and timing diagram of the proposed BP ADC, and (b) mathematical model of the proposed ADC.

as simple averaging, bayesian estimation [25] and MLE with fixed distribution [26]. Both bayesian estimation [25] and the technique of [26] requires prior knowledge of standard deviation of ADC noise to accurately estimate V_{res} . This is a key limitation of these techniques since ADC noise varies significantly over PVT [25]. We use MLE to estimate V_{res} by firing the comparator M times, and using the comparator outputs, $d[i]$ ($i \in [1, M]$), to form an estimate \hat{V}_{res} of the SAR residue, where each $d[i]$ is either ‘0’ or ‘1’. As shown in [27], [28], our technique does not require prior knowledge of comparator noise standard deviation and can estimate V_{res} accurately over voltage and temperature corners. An N -cycle delayed version of \hat{V}_{res} is subtracted from the SAR output, d_{sar} , to form a complex NTF which filters SAR ADC thermal and quantization noise and results in a BP ADC. Details of MLE are discussed in following sub-sections.

Fig. 1(b) shows mathematical model of the proposed ADC. Parasitic capacitance at the comparator input, C_p , forms a voltage divider with the DAC capacitance, C_{DAC} , and attenuates the input swing seen by the comparator. This is modeled by the interstage gain term, G , in Fig. 1(b) and $G < 1$. The SAR output is given by

$$d_{sar} = V_{in} + n_{th} + q_1 \equiv V_{in} + V_{res} \quad (1)$$

where n_{th} is thermal noise of the ADC, and q_1 is ADC quantization noise. kT/C noise for the proposed ADC is $10\times$ smaller than comparator thermal noise. Due to finite C_p ,

MLE forms an estimate of GV_{res} instead of V_{res} . Intuitively, MLE is a statistical technique to determine parameters of a model from its observed values. In our case, we are trying to estimate GV_{res} from the observations $d[i]$. We assume a gaussian distribution for estimating V_{res} since in power-optimized ADC design, thermal noise usually dominates quantization noise. The probability density of observing a single data point $d[i]$ generated from gaussian distribution is given by [29]

$$P(d[i]; GV_{res}, \sigma) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(d[i] - GV_{res})^2}{2\sigma^2}\right) \quad (2)$$

where σ represents the standard deviation of ADC noise. The joint probability density of observing the M data points $d[1]$ through $d[M]$, which is the likelihood function $L(\cdot)$, can then be written as

$$\begin{aligned} P(d[1], \dots, d[M]; GV_{res}, \sigma) &= L(GV_{res} | d[1], \dots, d[M]) \\ &= \frac{1}{\sqrt{(2\pi\sigma^2)^M}} \prod_{i=1}^M \exp\left[-\frac{(d[i] - GV_{res})^2}{2\sigma^2}\right] \end{aligned} \quad (3)$$

The estimate of V_{res} is the value which maximizes the likelihood function and is obtained by setting derivative of the log-likelihood function to zero. Thus, the MLE estimate of GV_{res} is written as

$$\hat{G}V_{res} = -\frac{1}{2} + \sqrt{\frac{1}{M} \sum_{i=1}^M d[i]^2 + \frac{1}{4}} \quad (4)$$

As can be seen from (4), computation of $\hat{G}V_{res}$ does not require knowledge of σ . Instead of computing $\hat{G}V_{res}$ every sampling period, we use an adder to sum all the ' $d[i]$'s and use a look-up table (LUT) to map the sum to pre-computed $\hat{G}V_{res}$ values.

An N -cycle delayed version of $\hat{G}V_{res}$ is subtracted from the SAR output and the overall ADC output is given by

$$d_{out} = d_{sar} - \frac{1 + z^{-N}}{2} \cdot \hat{G}V_{res} \quad (5)$$

where z^{-N} refers to the N clock cycle delay of the quantized residue. From (5) it can be derived that

$$\begin{aligned} d_{out} &= V_{in} + \left(1 - \frac{G}{2-G} z^{-N}\right) \cdot (1 - G/2) \cdot V_{res} \\ &\quad - \frac{1 + z^{-N}}{2} \cdot \epsilon \\ &= V_{in} + NTF_1 \cdot V_{res} - NTF_2 \cdot \epsilon \end{aligned} \quad (6)$$

where ϵ is the estimation error of MLE. As we will show in the following sections, we ensure that $G > 0.96$ through design. NTF_1 in (6) creates notches in ADC transfer function, thus making the ADC band-pass for $N > 2$, while NTF_2 shapes MLE estimation error and lowers its contribution in the signal band. In general, N cycle delay in subtracting MLE output from SAR output creates $N/2 + 1$ notches between 0 to $f_s/2$ in the ADC spectrum. Fig. 2(a) shows NTF_1 and NTF_2 for $N = 4$ for an IF of $f_s/4$. While the ADC high-pass shapes

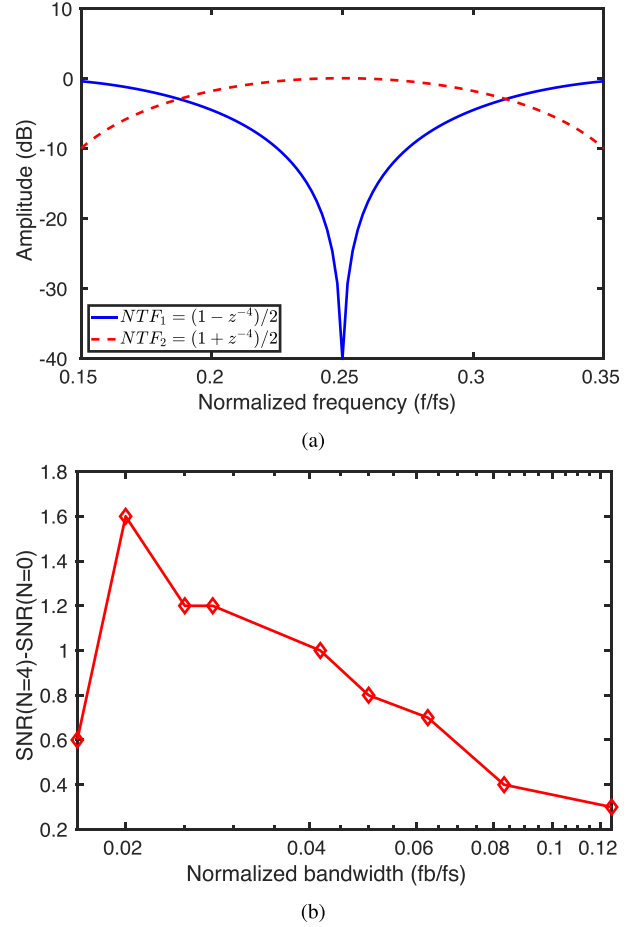
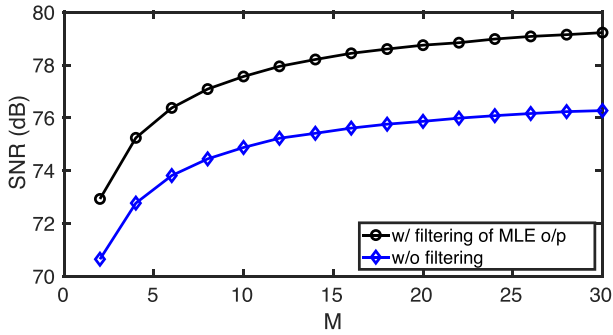


Fig. 2. (a) Simulated NTF_1 and NTF_2 for $N = 24$ (b) SNR improvement vs bandwidth.

V_{res} in the signal band for $N > 2$, V_{res} can be canceled if N is set to 0. However, the proposed technique also reduces MLE estimation error in the signal band. Fig. 2(b) shows the improvement in SNR for $N = 4$ over $N = 0$ as a function of bandwidth. M is set to 18 for this simulation and thermal noise is set to 0.5LSB. The SNR improvement is small for both small and large bandwidths. For small bandwidth, attenuation of MLE estimation error is limited in the signal band, while for large bandwidth, high-pass shaped V_{res} reduces SNR for $N = 4$. The maximum SNR improvement is 1.6dB for a bandwidth of $0.02f_s$. The amount of attenuation at the notch frequencies is set by the MLE error ϵ , and can be improved by increasing M , i.e., there is a trade-off between attenuation at the notch frequencies and speed and power. In practice, for any BP ADC, attenuation at the notch frequencies is limited either by thermal noise or component mismatch, and the proposed technique provides comparable attenuation to existing BP ADCs at much lower power and with the advantage of easy re-configurability of the BP transfer function. Both ADC thermal and quantization noise are band-pass filtered, and the proposed technique improves SNDR significantly more than by averaging alone.

A relevant question is how many times the comparator needs to be fired after SAR quantization for MLE to accurately estimate V_{res} . To answer this question, we perform simulations

Fig. 3. Simulated SNR vs M .

by varying the value of M and recording ADC SNR. N is set to 4 for the simulation. Thus, the ADC has notches at dc, $f_s/4$ and $f_s/2$. A sine-wave input with 0dBFS amplitude and frequency close to $f_s/4$ is used for the simulation. The ADC thermal noise is set to 0.5LSB and the ADC bandwidth is set to $f_s/24$. Fig. 3 shows ADC SNR versus M for an oversampling ratio (OSR) of 12 with filtering of MLE output by $(1+z^{-4})/2$ and without filtering. The SNR increases significantly with M for small M and derivative of SNR with respect to M reduces once $M > 15$. However, according to Cramer-Rao lower bound [29], the SNR will keep increasing asymptotically with M . M is set to 18 for this design.

B. Circuit Non-Idealities

Non-idealities that affect performance of the proposed BP-ADC are a) capacitor mismatch b) gain error c) thermal noise, and d) signal-dependent offset variation. Static element mismatch between capacitors in the DAC adds distortion tones and increases noise-floor of the ADC in the band-pass signal-band. Fig. 4 presents 2^{18} point ADC spectra showing the effect of capacitor mismatch on the BP-ADC performance. We use the same simulation set-up as was used for obtaining SNDR values for Fig. 3 except that M is set to 18. Under these simulation conditions, an ideal 10-bit SAR ADC will have an SNDR of 66.5dB with 10.8dB increase coming from reduction in ADC bandwidth. As can be seen from Fig. 4(a), the ADC has an SNDR of 78.6dB without any capacitor mismatch, which is 12.1dB better than simple averaging. With 1% capacitor mismatch added, the in-band noise floor increases along with spurs around the input tone, and the SNDR is reduced to 67.8dB as shown in Fig. 4(b).

Fig. 5 shows simulated ADC SNDR versus capacitor mismatch. As is expected, the SNDR reduces by almost 25dB for 5% capacitor mismatch. Fig. 5 shows that ADC SNDR can be greater than 70dB as long as capacitor mismatch is less than 0.5%. Based on foundry mismatch data, a 4.8fF unit metal-on-metal (MOM) capacitor is used for the capacitive DAC such that mismatch is less than 0.5%. The total capacitance in each DAC is 2.4pF.

The next non-ideality is gain error arising out of capacitive divider formed due to parasitic capacitance at comparator input and the capacitive DAC. Gain error limits attenuation at the band-pass notches, and more importantly, increases

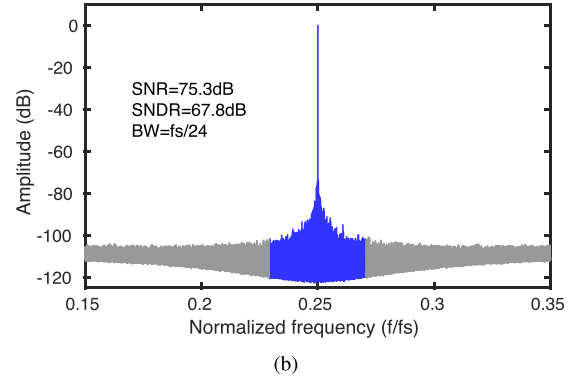
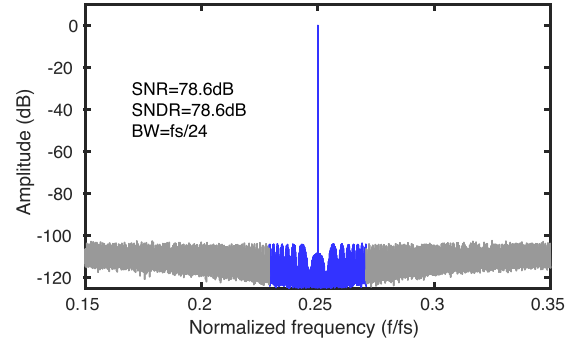
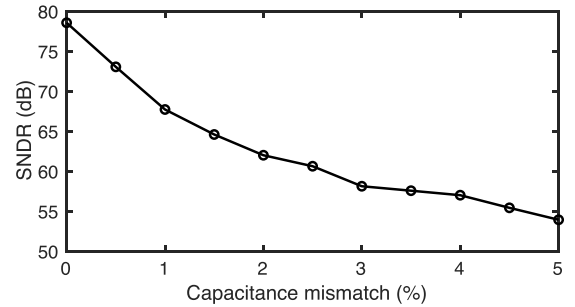
Fig. 4. Simulated 2^{18} point zoomed-in FFT with f_{in} close to $f_s/4$ and 0 dBFS input for (a) no capacitor mismatch, and (b) 1% capacitor mismatch.

Fig. 5. Simulated SNDR versus capacitance mismatch.

in-band noise. For this design, we have used a low-power comparator and post-layout extracted C_p is 3.1% of C_{DAC} . Fig. 6(a) shows simulated ADC SNDR versus G . The simulation conditions are identical to those used for capacitance mismatch simulations, except that no capacitor mismatch is considered for the DAC. Fig. 6(a) shows that the ADC SNDR changes by less than 2dB as long as $G \geq 0.9$. Fig. 6(b) shows 2^{18} point FFT plot for 3% gain error ($G = 0.97$). The ADC SNDR is 78.6dB and does not show any degradation due to gain error. Since, gain error for the proposed ADC is very small, we do not need any calibration to correct for gain error.

Apart from capacitance mismatch and gain error, thermal noise affects ADC performance. Fig. 7(a) plots ADC SNR versus thermal noise standard deviation as well as improvement in SNR due to MLE for same bandwidth. The simulation conditions are identical to those used for capacitance mismatch simulations, except that no capacitor mismatch is considered

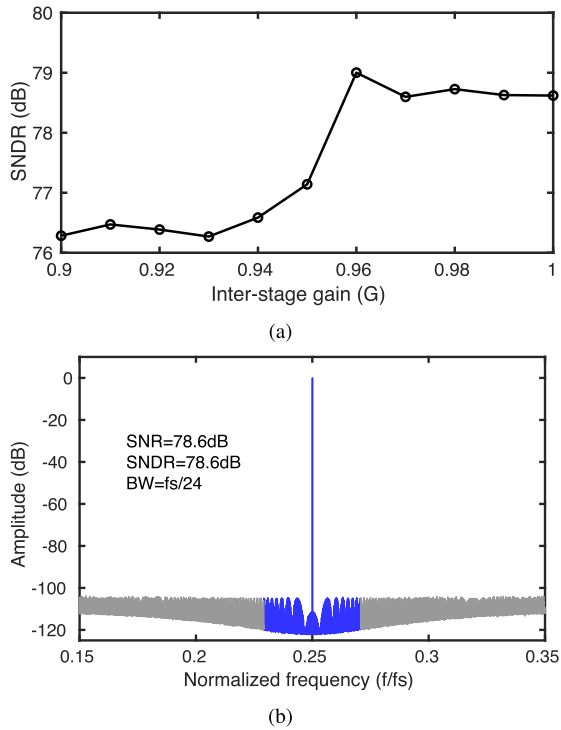
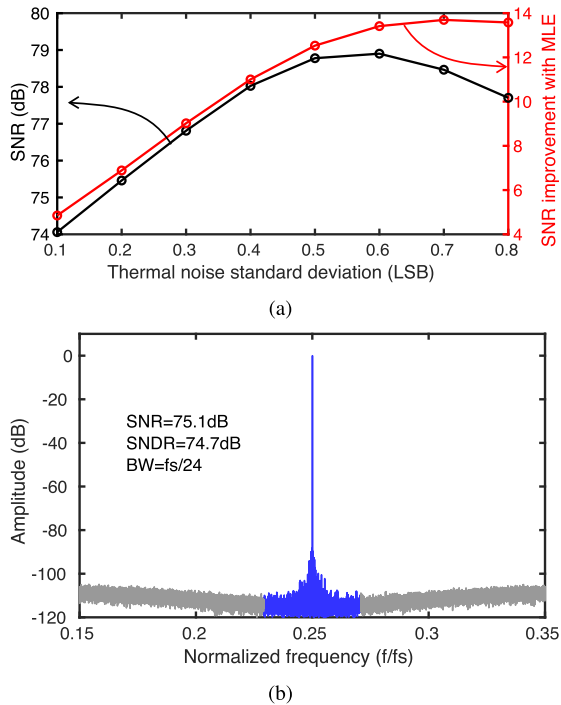
Fig. 6. (a) Simulated SNDR versus G (b) FFT plot for $G = 0.97$.

Fig. 7. (a) Simulated SNR and improvement in SNR due to MLE versus thermal noise (b) FFT plot for 0.8LSB thermal noise.

for the DAC. If thermal noise is too large, ADC SNR reduces as expected. However, if thermal noise is too small, V_{res} is not randomized adequately, and the MLE accuracy is reduced which reduces ADC SNR. The ADC has highest SNR for thermal noise in the region of 0.5-0.6LSB. However, as shown in Fig. 7(b), the SNR improvement due to MLE keeps increasing

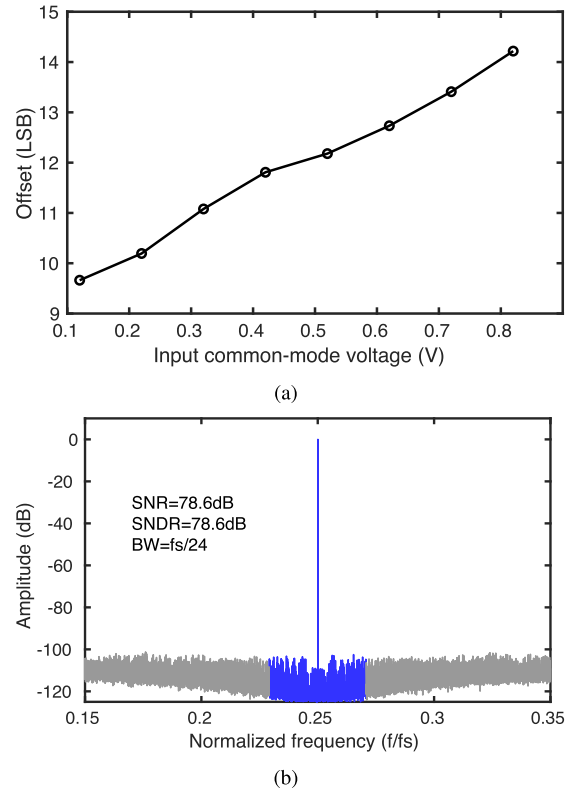


Fig. 8. (a) Measured ADC offset versus comparator input common mode voltage (b) simulated FFT plot with signal dependent offset.

with thermal noise. Fig. 7(b) shows simulated 2^{18} point FFT plot for thermal noise of 0.8LSB.

As shown in [24], common-mode voltage at the comparator input varies from $0.75V_{dd}$ to $0.5V_{dd}$ during SAR conversion. Change in input common-mode voltage also changes the comparator offset [30], thus making the offset signal dependent. Fig. 8(a) shows the measured offset versus comparator input common-mode voltage. The signal dependent offset is added to our SAR behavioral model, and the model is simulated to check the effect of signal dependent offset. Fig. 8(b) shows the 2^{18} point FFT plot. The ADC has a high SNDR of 78.6dB and the ADC performance is not degraded by the signal dependent offset.

C. Choice of Pass-Bands

An interesting aspect of the proposed BP-ADC is how to select the number of pass-bands for a given signal bandwidth. As an example, let us consider an input signal close to $f_s/4$ with a signal bandwidth of $f_s/24$ as in the previous simulations. Both $N = 4$ and $N = 24$ are valid design choices for the BP-ADC. For $N = 4$, the ADC will have 3 notches between 0 and $f_s/2$, while for $N = 24$, the ADC will have 13 notches between 0 and $f_s/2$. Fig. 9(a) and (b) shows 2^{18} point FFT for $N = 4$ and $N = 24$ respectively. Fig. 9 shows that SNDR reduces by 4.4dB when N is increased from 4 to 24 keeping everything else same. The reason for reduction in SNDR is that if N is increased, the in-band noise in each of the pass-bands increases. This is derived mathematically in

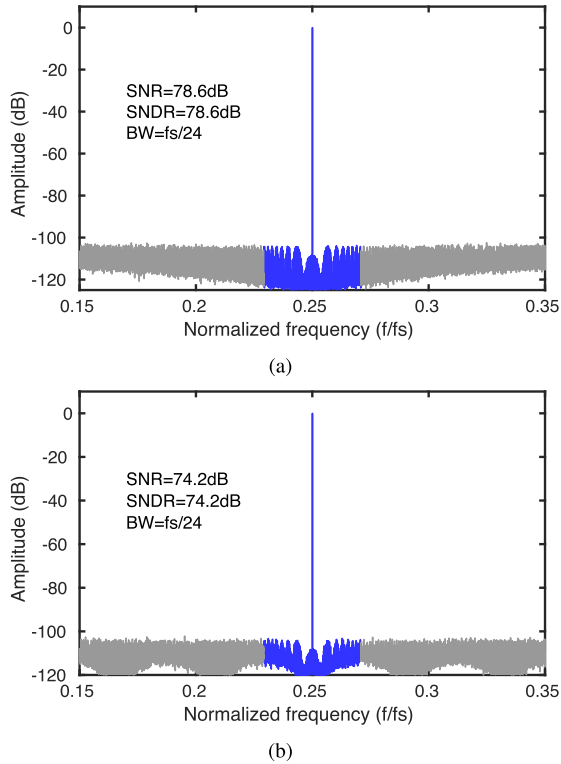


Fig. 9. Simulated FFT plots for (a) $N = 4$ and (b) $N = 24$.

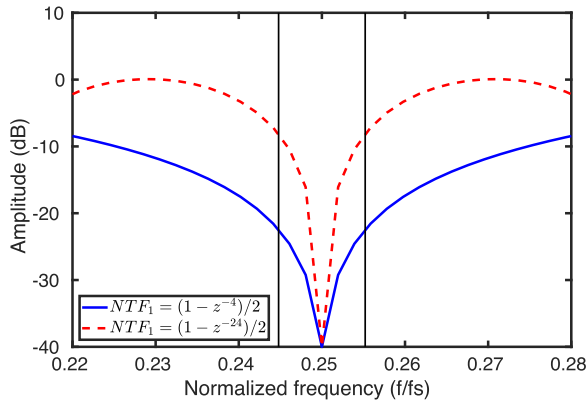


Fig. 10. NTF_1 for different values of N .

the appendix. Fig. 10 shows noise-transfer functions for NTF_1 of $(1 - z^{-4})$ and $(1 - z^{-24})$. It can be seen that in-band noise increases with N .

D. Comparison With Oversampling and Averaging

In addition to stochastic techniques, such as MLE and bayesian estimation [25], SAR ADC noise can also be reduced by other techniques such as oversampling, simple averaging of the comparator decisions $d[i]$, analog scaling of comparator noise and hybrid architectures [31]–[34]. Hybrid noise-shaping architectures reduce SAR noise by either adding a second stage after the SAR or subtracting delayed version of residue signal from SAR output to high-pass shape SAR noise. Recent works have used voltage-controlled oscillators (VCOs) as second-stage of hybrid architecture to improve energy efficiency [31], [32] but requires calibration for interstage gain matching since VCO tuning gain is susceptible to PVT variations.

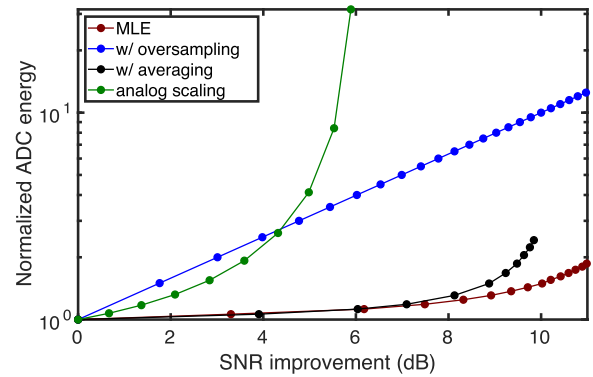


Fig. 11. Comparison of energy versus SNR improvement for different techniques.

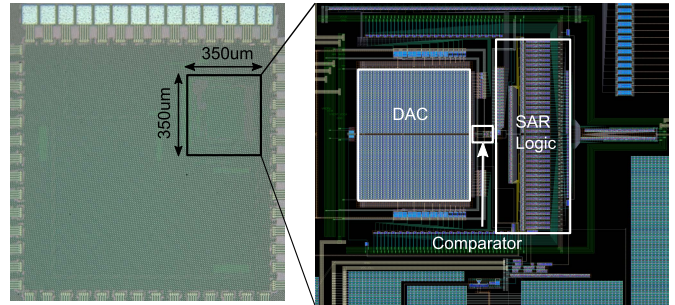


Fig. 12. Chip microphotograph and layout.

Noise-shaping hybrid SAR architectures either require power-hungry OTA to integrate SAR residue [34] or use passive integrator [33] which increases in-band noise. However, different from the other techniques such as oversampling, averaging, analog scaling and stochastic estimation, hybrid SAR architectures require significant additional circuits and greatly increased power consumption to reduce SAR noise. As an example, the VCO in the hybrid ADC of [31] consumes the same power as SAR stage.

Fig. 11 compares energy consumption versus improvement in SNR obtained through MLE, oversampling, averaging of the comparator decisions $d[i]$, and analog scaling for 10-bit SAR ADC with comparator noise σ of 0.5LSB. Analog scaling consumes the most energy since the comparator power increases by $4\times$ for every $2\times$ reduction in comparator noise. Since analog scaling can only reduce comparator thermal noise, the maximum improvement in SNR is limited by quantization noise even if the power consumption is increased to infinity. In contrast, oversampling reduces both thermal and quantization noise. However, oversampling is not energy-efficient since increase in OSR by $4\times$ increases ADC power by $4\times$ but improves SNR by $2\times$. Also, the entire SAR conversion, including sampling, comparison, and DAC switching, has to be repeated 4 times for an OSR of 4. In contrast, averaging and MLE are more energy efficient since they only increase the number of LSB comparisons. However, MLE has an advantage over averaging in that the SNR improvement through averaging is limited since averaging is a biased estimator [25], [29], i.e., if the number of LSB comparisons M is kept on increasing, SNR improvement due to averaging will eventually saturate

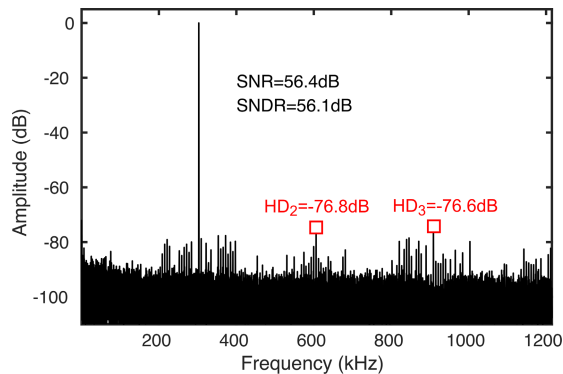
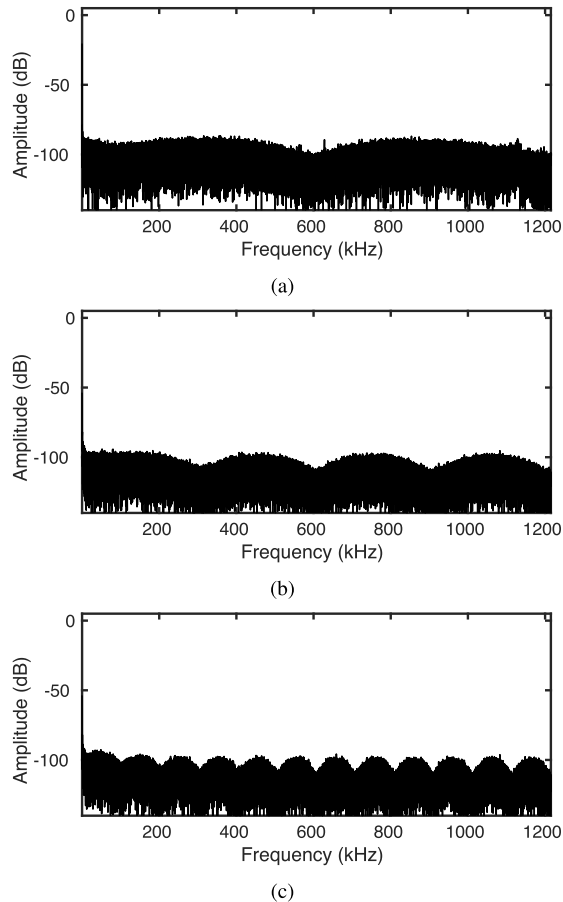


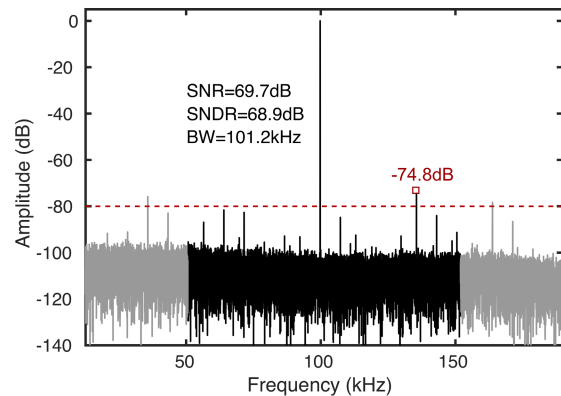
Fig. 13. Measured FFT of SAR ADC output.

Fig. 14. Measured 2^{19} point NTF_1 spectra for (a) $N = 4$ (b) $N = 8$ (c) $N = 24$.

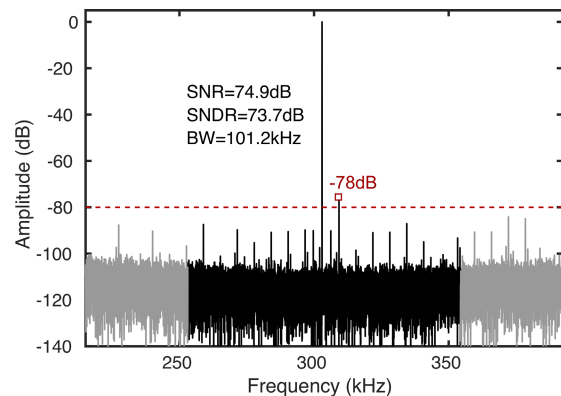
and will limit energy efficiency. On the other hand, MLE is an unbiased estimator and the SNR improvement due to MLE keeps increasing asymptotically with M . Thus, MLE is more energy-efficient than averaging. This can also be seen from Fig. 11.

III. MEASUREMENT RESULTS

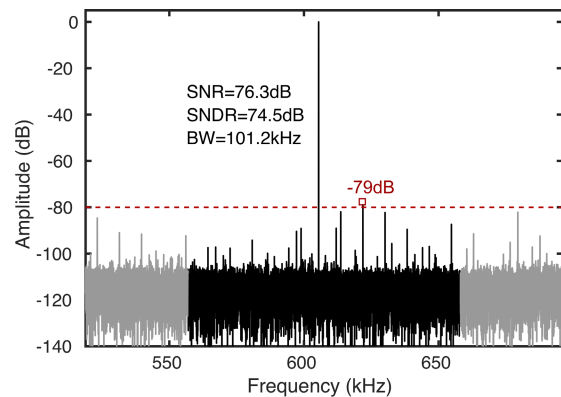
A prototype of the proposed ADC was fabricated in 65nm CMOS. Fig. 12 shows the chip microphotograph, and ADC layout. The ADC core occupies an area of $350\mu\text{m} \times 350\mu\text{m}$. The MLE is implemented off-chip, and consists of an adder to



(a)



(b)



(c)

Fig. 15. Measured 2^{19} point zoomed-in FFT for (a) $f_{in} = 99.8\text{kHz}$ and $N = 24$ (b) $f_{in} = 302.9\text{kHz}$ and $N = 8$ (c) $f_{in} = 605.4\text{kHz}$ and $N = 4$ with 0 dBFS input.

sum the M comparator decision bits, an LUT, and a subtractor to subtract MLE output from the SAR output. Off-chip implementation of MLE allows us to easily check different NTFs. The ADC consumes $17\mu\text{W}$ power, which includes estimated power consumption of adder and subtractor [35] required for combining MLE output with SAR output, while running at 2.43MHz. Fig. 13 shows the measured spectrum of SAR ADC output. The SAR ADC has an SNDR of 56.1dB and SFDR $> 76\text{dB}$.

Fig. 14 shows measured NTF_1 for $N = 4, 8$ and 24. Fig. 15 shows measured FFT of BP-ADC for 99.8kHz and

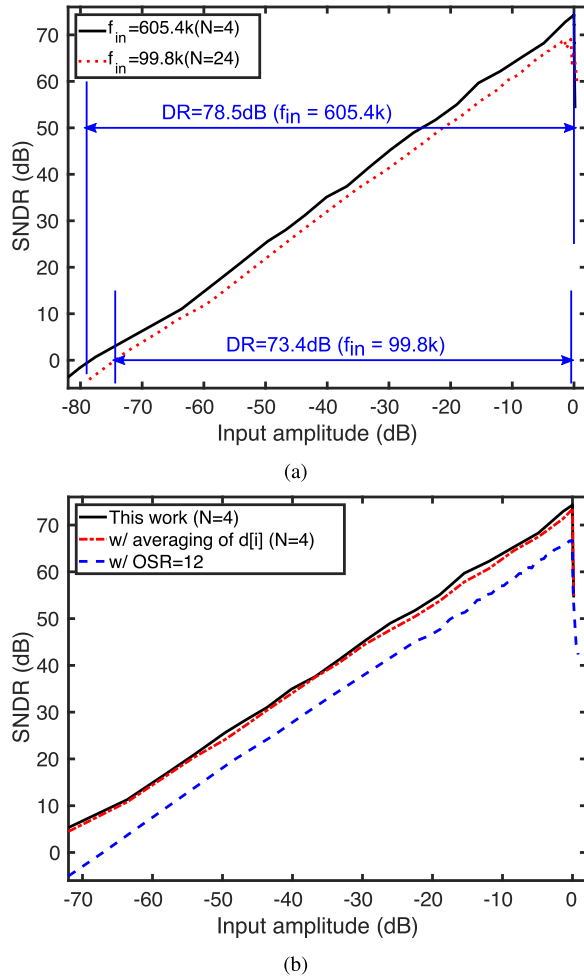


Fig. 16. Measured SNDR vs input amplitude for (a) 99.8kHz and 605.4kHz inputs (b) comparison with SAR ADC with same bandwidth and averaging of LSB comparisons.

302.9kHz inputs. N is set to 24 for 99.8kHz input. As shown in Fig. 15(a), the ADC has an SNDR of 68.9dB over a bandwidth of 101.2kHz. The in-band tones are due to capacitor mismatch. Fig. 15(b) shows ADC spectrum for 302.9kHz input and $N = 8$. The measured SNDR is 73.7dB. Fig. 15(c) shows ADC spectrum for 605.4kHz input and $N = 4$. The measured SNDR is 74.5dB. Fig. 16(a) shows measured SNDR versus input amplitude for 605.4kHz input ($N = 4$) and 99.8kHz input ($N = 24$). The ADC has a dynamic range of 78.5dB for 605.4kHz input and 73.4dB for 99.8kHz input. Fig. 16(b) compares this work with simple averaging of LSB comparisons $d[i]$ and SAR ADC with OSR of 12. Simple averaging results in SNDR values within 1dB of those obtained with MLE while oversampling results in 10-11dB lower SNDR. While for this design averaging of $d[i]$ results in similar performance as MLE, as discussed earlier, in general MLE outperforms simple averaging. Fig. 17 shows results of two-tone test performed with 303kHz and 313kHz inputs for $N = 8$. The measured IM_3 is greater than 68dB.

Fig. 18 shows the measured SNR and SNDR versus supply voltage and temperature. Both SNR and SNDR reduce

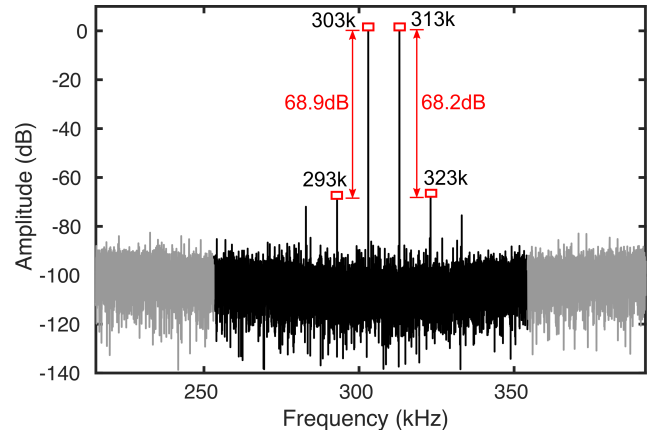


Fig. 17. Measured two-tone test with 303kHz and 313kHz inputs.

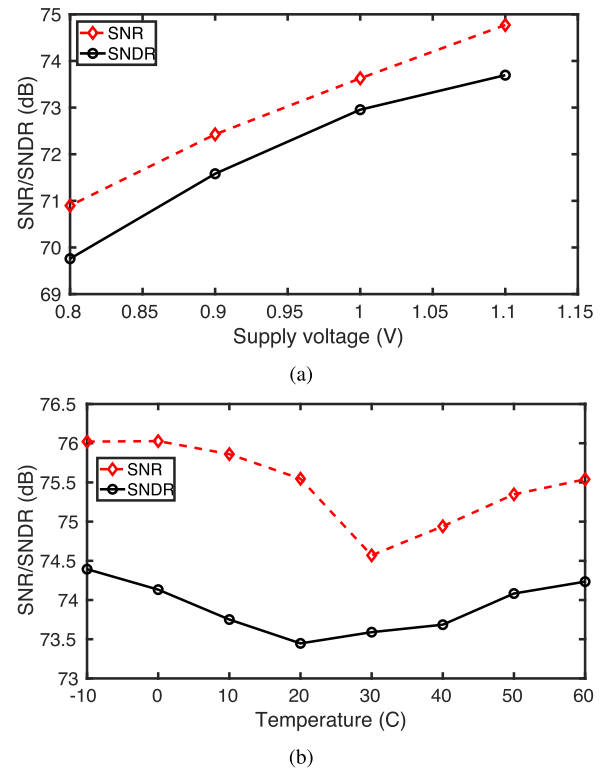


Fig. 18. Measured SNDR and SNR versus (a) supply voltage and (b) temperature.

by almost 4dB as the supply voltage is changed from 1.1V to 0.8V. At low temperatures, thermal noise is lower, and SNR and SNDR are the highest at -10°C . As the temperature is increased, thermal noise increases which lowers both SNR and SNDR. However, once the temperature is around 30°C , increase in thermal noise randomizes V_{res} which improves MLE accuracy and improves both SNR and SNDR. This is also consistent with our simulation result (see Fig. 7(a)) which shows that SNDR increases with thermal noise due to better accuracy of MLE, before dropping once thermal noise exceeds a certain threshold. We expect that if the temperature exceeds 60°C , we will see SNR and SNDR drop again. However, the

TABLE I
COMPARISON WITH STATE-OF-THE-ART BAND-PASS $\Delta\Sigma$ ADCs WITH SIMILAR BANDWIDTH

	Process (nm)	Area (mm ²)	Resonator (\checkmark/\times)	f_s (MHz)	BW (MHz)	Power (mW)	IF (MHz)	SNDR (dB)	DR (dB)	FoM _S (dB) ¹	FoM _{BP} (pJ/step) ²
ESSCIRC'01 [5]	180	0.58	\checkmark	80	0.27	56	20	72	84	151	12.41
JSSC'01 [9]	350	1	\checkmark	42.8	0.2	76	10.7	61	74	138.2	81
JSSC'02 [8]	250	5.6	\checkmark	10	0.25	77	0.57	77.4	-	142.5 ³	18.43
JSSC'03 [6]	350	1	\checkmark	80	0.27	24	20	78	86	156.5	2.65
JSSC'04 [7]	180	1	\checkmark	37	0.2	88	10.7	-	76	139.6	-
JSSC'08 [11]	180	4.5	\checkmark	40	0.31	115	12.6	71	76	140.3	21.5
TCAS-I'17 [21]	55	5.4	\times	250	1.95	103	62.5	85.3	85.3	158	0.68
This Work	65	0.12	\times	2.43	0.1	0.017 ⁴	0.1	68.9	73.4	166.5	0.029
							0.3	73.7	77.6	175.3	0.012
							0.6	74.5	78.5	176.1	0.008

¹FoM_S = DR + 10 log₁₀(BW/Power);

²FoM_{BP} = Power/(2^{ENOB} × 2BW)/(1+(6 × IF/f_s)); ENOB = (SNDR-1.76)/6;

³SNDR used for computing FoM_S as DR not provided;

⁴Includes 0.34μW estimated power of adder and subtractor used in MLE [35]

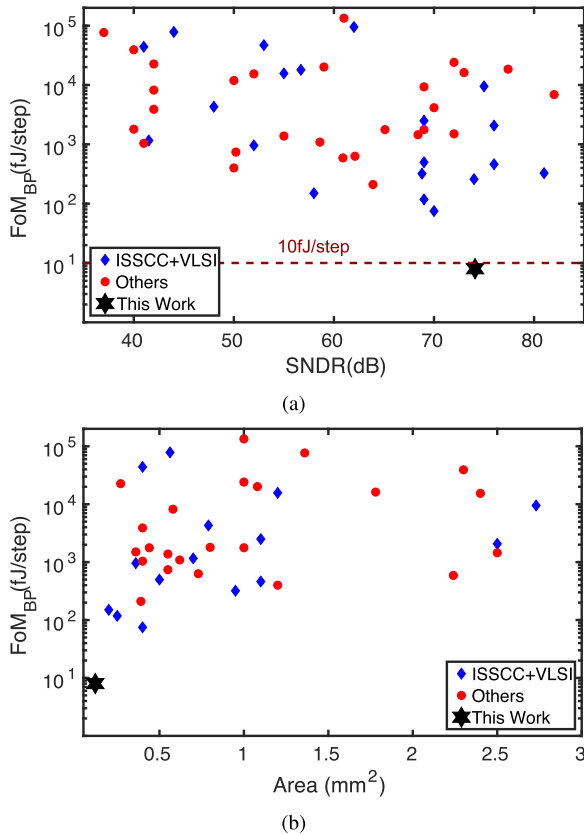


Fig. 19. Comparison of ADC FoM across (a) SNDR and (b) area.

temperature had to be limited to 60°C to avoid damaging plastic components on the test-board.

Table I compares our BP ADC with state-of-the-art BP ADCs with similar bandwidth. Thanks to the highly digital and

OTA-less architecture, the proposed ADC consumes the lowest power of 17μW. To compare energy-efficiency of different BP ADCs, we have used the BP figure-of-merit (FoM) [3] which is similar to the well known walden FoM but takes the ratio of IF to sampling frequency into account. The proposed ADC has the lowest BP-FoM of only 29fJ/step for 100kHz IF and 8fJ/step for 600kHz IF. While this prototype has been designed for low IF, due to the highly digital nature of the proposed ADC, it is expected that the ADC will retain similar energy efficiency when designed for higher IF. Fig. 19 compares BP FoM of the proposed ADC versus SNDR and area with state-of-the-art BP ADCs [36]. It can be seen from Fig. 19 that the proposed ADC has the best energy efficiency and lowest area while having competitive SNDR.

IV. CONCLUSION

This work has presented a SAR band-pass ADC based on stochastic estimation of SAR residue. The proposed architecture alleviates the drawbacks associated with existing BP ADCs such as low energy efficiency, limited scalability, channel mismatch and lack of NTF re-configurability. In contrast, the proposed BP ADC comprises a single channel that is OTA free, consumes low power, has a compact implementation with dynamic NTF re-configurability and achieves more than 5× improvement in energy-efficiency compared to existing state-of-the-art BP ADCs. While the current ADC is designed for low IF and low bandwidth, due to its highly digital nature, speed of the proposed architecture can be increased proportionally with power while maintaining the same energy efficiency. Due to its highly digital nature, the proposed architecture can easily be ported into more advanced technologies to improve speed or reduce power.

APPENDIX

The SAR residue, V_{res} , is shaped by the filter $(1 - z^{-N})/2$. Assuming V_{res} has flat power spectral density (PSD) given by PSD_{vres} , the in-band noise power due to SAR thermal and quantization noise is given by

$$\begin{aligned} P_n &= \int_{-f_B/2}^{f_B/2} PSD_{vres} \cdot \frac{1}{2f_s} \left| (1 - z^{-N}) \right|^2 df \\ &\approx \int_{-f_B/2}^{f_B/2} PSD_{vres} \cdot \frac{1}{2f_s} \left[2\pi \frac{Nf}{f_s} \right]^2 df \\ &= \frac{\pi^2}{48} \cdot N^2 \cdot PSD_{vres} \cdot \frac{1}{OSR^3} \end{aligned} \quad (7)$$

where OSR denotes oversampling ratio. As can be seen from (7), increasing the number of delay taps, N , increases noise power. Thus, for a given signal bandwidth and sampling frequency, minimum value of N should be selected to maximize SNDR.

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Sanjeev Tannirkulam Chandrasekaran (Graduate Student Member, IEEE) received the B.Tech. degree in electronics and instrumentation from SASTRA University, Thanjavur, India, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering from the University at Buffalo, Buffalo, NY, USA. He has held internship positions with Mythic-AI, Austin, TX, USA, and a GE Global Research, Niskayuna, NY, USA, where he was involved in mixed-signal IC design. His research interests are geared towards developing scalable energy-efficient circuits for the IoT applications with a focus on data converters and Edge-AI. He was a recipient of the 2019 MWSCAS Student Participation Grant and the 2019 CICC Student Travel Grant Award. He currently serves as a Reviewer for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (TCAS-I) and the IEEE SOLID-STATE CIRCUITS LETTERS (SSC-L).



Gaurav Kapoor received the B.E. degree from PES University, Bengaluru, India, in 2016, and the M.S. degree in electrical engineering from University at Buffalo, NY, USA, in 2019.

In summer 2018, he was an Intern with the Analog/Mixed Signal Design Group, Macom Technology Solutions, Santa Clara, CA, USA, designing clock buffers to drive high-speed SERDES. He is currently a Device Engineer with the Technology Development Group, Intel Corporation, Hillsboro, OR, USA. His research interests include analog circuit design, mixed-signal security circuits, and data converters.



Arindam Sanyal (Member, IEEE) received the B.E. degree from Jadavpur University, India, in 2007, the M.Tech. degree from The Indian Institute of Technology, Kharagpur, in 2009, and the Ph.D. degree from The University of Texas at Austin, in 2016.

He was a Design Engineer worked on low jitter PLLs at Silicon Laboratories, Austin, TX, USA. He is currently an Assistant Professor with the Electrical Engineering Department, The State University of New York at Buffalo. His research interests include analog/mixed signal design, bio-medical sensor design, analog security, and on-chip artificial neural networks.

Dr. Sanyal was a recipient of the National Science Foundation CISE Research Initiation Initiative (CRII) Award in 2020, the Intel/Texas Instruments/Catalyst Foundation CICC Student Scholarship Award in 2014, and the Mamraj Agarwal Award in 2001.