A Fractional-*N* PLL With Space–Time Averaging for Quantization Noise Reduction

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***Abstract*— This article presents a space–time averaging technique that can realize instantaneous fractional frequency division, and thus, can significantly reduce the quantization error in a fractional-*N* phase-locked loop (PLL). Spatial averaging can be achieved by using an array of dividers running in parallel. Their different division ratios are generated by using a fractional $\Delta\Sigma$ modulator (DSM) and a dynamic element matching (DEM) block. To reduce the divider power, this article also proposes a way to achieve spatial averaging using only one divider and phase selection. A prototype 2.4-GHz fractional-*N* PLL is implemented in a 40-nm CMOS process. Measurement results show that the proposed technique reduces the phase noise by 10 and 21 dB at the 1- and 10-MHz offset, respectively, leading to a reduction of the integrated rms jitter from 9.55 to 2.26 ps.**

***Index Terms*— $\Delta\Sigma$ modulator (DSM), data-weighted averaging (DWA), dynamic element matching (DEM), fractional-*N* PLL, frequency synthesizer, phase noise, phase-locked loop (PLL), quantization noise reduction.**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in modern electronic systems for clock generation [1]–[4], frequency synthesis [5]–[8], clock and data recovery [9]–[12], and phase or frequency modulation [13]–[16]. Compared with integer-*N* PLLs, fractional-*N* PLLs have finer frequency resolution, wider bandwidth, and faster settling time [17], [18], but they suffer from the quantization noise, whose root cause is that a standard frequency divider can only divide by an integer. One common way to suppress the quantization error is to lower the PLL bandwidth, however at the cost of slower settling time and increased oscillator noise.

There have been many works over the past two decades on reducing the quantization noise without sacrificing the PLL bandwidth. An analog approach is to use a digital-to-analog converter (DAC) or a digital-to-time converter (DTC) to cancel the quantization error [19]–[27]. However, the DAC or DTC needs to be highly accurate and robust against process, voltage, and temperature (PVT) variation. This often leads to increased chip area, power, and design complexity. Another analog approach is to use phase interpolation (PI) [28]–[33], but it suffers from phase mismatch and is also sensitive to PVT variation. Recently, a finite-impulse-response (FIR) filtering technique is proposed [34]–[37]. Being highly digital, it is PVT robust and calibration free. Nevertheless, it cannot reduce the quantization error within the FIR filter bandwidth. To sufficiently suppress the quantization error, a large number of FIR filter taps are required, which result in increased hardware complexity and power consumption [37].

This article presents a highly digital, PVT-robust, and calibration-free technique that can significantly reduce the quantization noise over the entire frequency range. It is based on a new concept of *spatial averaging*, which is realized by using an array of dividers, phase/frequency detectors (PFDs), and charge pumps (CPs) [38]. If the divider array is considered as a whole, an *instantaneous* fractional frequency division is realized. In this way, the quantization step of the $\Delta\Sigma$ modulator (DSM) can be a truly fractional number, rather than an integer in a conventional fractional-*N* PLL. As a result, the quantization error is much smaller. While the original *spatial averaging* technique requires a large number of dividers, this article proposes a method that requires only one divider, leading to substantially reduced power and hardware cost compared to [38]. A prototype 2.4-GHz fractional-*N* PLL is implemented in a 40-nm CMOS process. Measurement results show that the in-band and out-of-band phase noise is reduced by 10 and 21 dB, respectively. The integrated rms jitter is reduced from 9.55 to 2.26 ps, which is almost the same as the case when the PLL runs in the integer-*N* mode. These results clearly prove the effectiveness of the proposed technique. In addition to the aforementioned merits, the proposed

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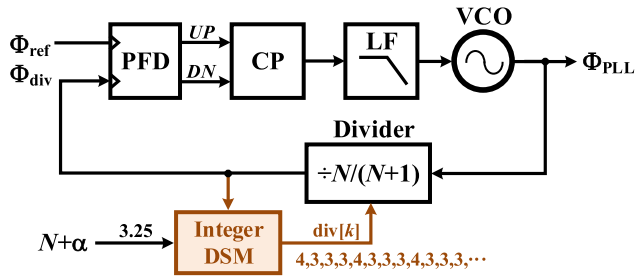

Fig. 1. Block diagram of a conventional fractional-*N* PLL.

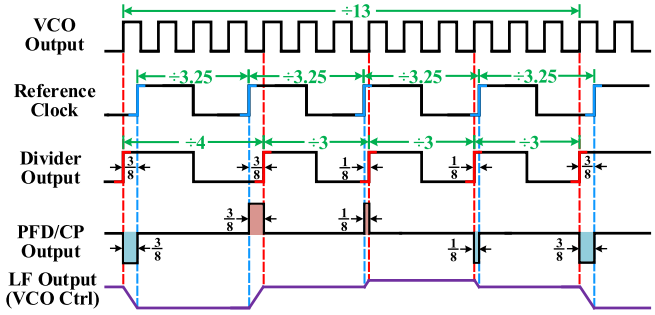

Fig. 2. Time-domain waveform of a conventional fractional-*N* PLL.

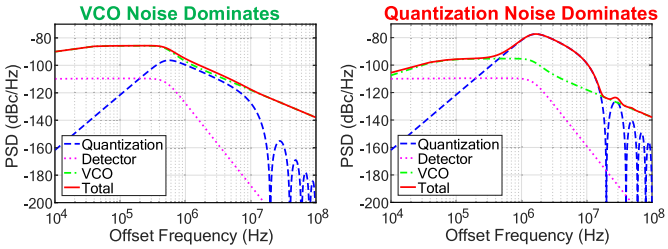

Fig. 3. Quantization noise effects with (a) narrow PLL bandwidth and (b) wide PLL bandwidth.

space–time averaging (STA) technique is compatible with other quantization noise reduction techniques. For instance, it can be combined with the FIR filtering technique for further suppression to the quantization error at higher frequencies.

This article extends [39] and is organized as follows. Section II reviews the conventional fractional-*N* PLL. Section III presents the proposed STA PLL. Section IV describes the approach to achieve spatial averaging with a single divider and phase selection. Section V shows the implementation of the prototype PLL. The measurement results are given in Section VI. Section VII draws the conclusion.

II. Review of Conventional Fractional-*N* PLL

Before presenting the proposed technique, let us first review a conventional fractional-*N* PLL as shown in Fig. 1. Because the divider can only divide by an integer, the fractional division ratio $N + \alpha$ has to be converted to a sequence of integer numbers using a DSM with an integer step, so that the long-term *time average* of the instantaneous division ratio div[k] is equal to $N + \alpha$. Mathematically speaking, we have

$$\lim_{K\to\infty} \frac{1}{K} \sum_{k=1}^{K} \text{div}[k] = N + \alpha. \tag{1}$$

However, at any time instance k, div[k] is unequal to $N + \alpha$. Their difference is the *quantization error* of the fractional-*N* PLL [17], which results in increased output phase noise.

For example, to realize the division ratio of 3.25, the divider is set to divide the VCO output by 3 for 75% of the time and by 4 for 25% of the time. Hence, via time averaging, the integer divider acts like a fractional divider providing a fractional division ratio of 3.25. However, at any given time instance, the division ratio is not 3.25, but 3 or 4, resulting in the quantization error. Fig. 2 shows the time-domain waveform. The divider output frequency matches the reference clock frequency over time averaging across 13 VCO cycles. However, the rising edge of the divider output (marked in red) does not align with the rising edge of the reference clock (marked in blue). This phase error produces pulses at the PFD output, whose widths are marked with fractional numbers normalized to the VCO period. These pulses cause a nonzero net charge injected into or taken away from the loop filter through the CP. The resulting ripples modulate the VCO output frequency, increasing phase noise. Additionally, as this example shows, the division ratio pattern can repeat, especially when a low-order DSM is used. This can generate fractional spurs. To reduce these spurs, one can add dither in the DSM to break the periodicity [40] or use additional techniques, such as the probability mass redistributor (PMR) [41], to suppress fractional spurs.

Fig. 3 shows the power spectral density (PSD) of the PLL output phase noise with different bandwidth settings. The quantization error is high-pass shaped by the DSM. As shown in Fig. 3(a), a narrow PLL bandwidth (e.g., 500 kHz) can effectively suppress the quantization error, but it leads to increased VCO phase noise and slower settling. In contrast, as Fig. 3(b) shows, a wide PLL bandwidth (e.g., 1.5 MHz) reduces the VCO phase noise and accelerates the settling, but its phase noise is dominated by the substantially increased quantization error. Thus, it is highly desirable to develop techniques to reduce the quantization error for wideband PLLs.

III. Proposed STA PLL

The initial idea of the proposed STA technique was published in our early work [38], in which a specific case was discussed briefly. In order to clearly demonstrate the advantages of this technique, in this section, we will first introduce the general architecture and the detail operation of the proposed STA technique and then provide the loop response and noise analyses.

A. Architecture of Proposed STA PLL

Fig. 4 shows the block diagram of the proposed PLL architecture. Different from the conventional architecture in Fig. 1, the new architecture uses an array of dividers, PFDs, and CPs to achieve *spatial averaging* for quantization error reduction. The divider, the PFD, and the CP arrays can be considered

TABLE I
VECTOR DIVISION RATIO PATTERN IN FIG. 5

Division Ratios	Time Instance				Time Averaging $(\sum_{j=1}^{4} \mathrm{DivN}_i[k+j])/4$
	$k+1$	$k+2$	$k+3$	$k+4$	
DivN_1	4	3	3	3	3.25
DivN_2	3	4	3	3	3.25
DivN_3	3	3	4	3	3.25
DivN_4	3	3	3	4	3.25
Spatial Averaging $(\sum_{i=1}^{4} \mathrm{DivN}_i[k])/4$	3.25	3.25	3.25	3.25	3.25

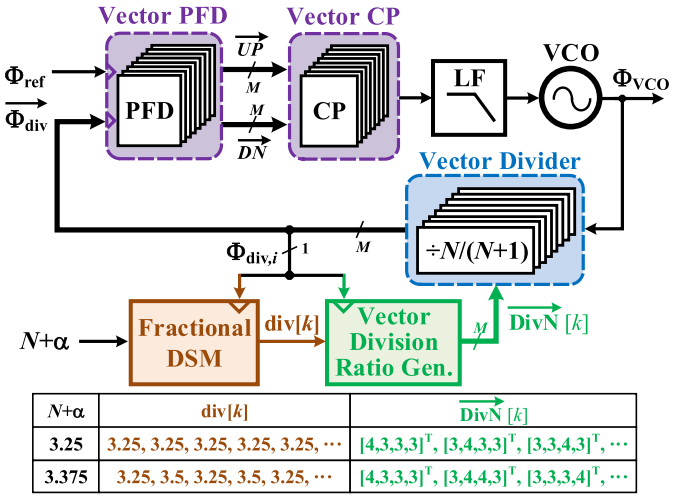

Fig. 4. Block diagram of the proposed STA PLL.

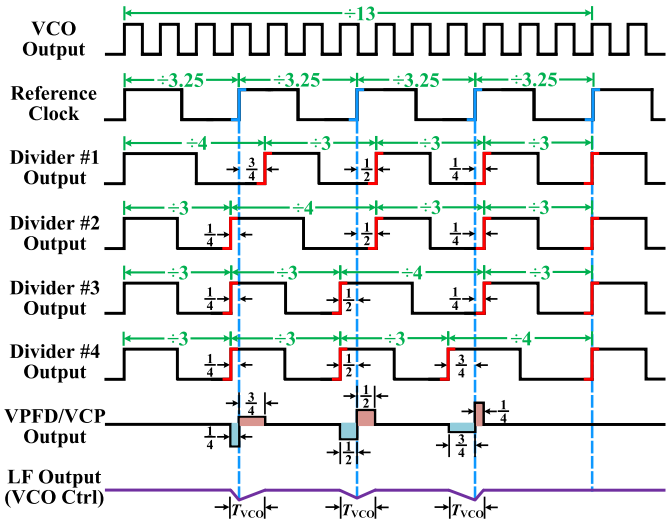

Fig. 5. Time-domain waveform of the proposed STA PLL.

as vector blocks, i.e., a vector divider, a vector PFD, and a vector CP. The single slice of each vector block together forms a channel, and all M channels operate concurrently and independently.

The key to the proposed PLL architecture is how to properly control the vector divider. This task is accomplished by the vector division ratio generator. It converts the fractional division ratio $\mathrm{div}[k]$ to a vector division ratio $\overrightarrow{\mathrm{DivN}}[k]$, each element of which corresponds to the instantaneous integer division ratio of a divider slice. In addition, a *fractional* DSM is applied to generate $\mathrm{div}[k]$ from the division ratio $N+\alpha$. The operation of these two blocks will be explained in detail later.

B. Fractional Frequency Division by Spatial Averaging

To understand how spatial averaging works, let us take a look at an example shown in Fig. 5. The division ratio $N+\alpha$ is again 3.25, and the number of slices, M, is set to 4.

Table I summarizes the vector division ratio pattern of the four dividers in Fig. 5. Note that although the division ratio pattern is different for every divider, the time averaging of the division ratio for any divider #i over four adjacent reference clock periods is $(\sum_{j=1}^{4} \mathrm{DivN}_i[k+j])/4 = 3.25$. Thus, each divider works like the only divider in a conventional fractional-N PLL. This ensures that the output frequency of every divider is the same, which is a prerequisite for the proposed PLL architecture to work.

The most important feature of the proposed architecture, which is also easy to see from Fig. 5 and Table I, is that during any reference clock period, we have one divider dividing by 4 and three dividers dividing by 3. As a result, the spatial average of the division ratios is $(\sum_{i=1}^{4} \mathrm{DivN}_i[k])/4 = 3.25$ for any reference clock period k. In other words, if we consider these four dividers as a whole, it is equivalent to a truly fractional divider with the *instantaneous* division ratio of 3.25. Note that this is achieved *not* by time averaging but by *spatial averaging* among the four dividers. In this way, as shown in Fig. 5, even though the rising edge of any individual divider may not align with the rising edge of the reference clock (marked with the blue dashed lines), the arithmetic mean of the rising edges of the vector divider is always at the blue dashed lines. Taking the leftmost blue dashed line as an example, the rising edge of the divider #1 lags that of the reference clock by $3/4\ T_{\mathrm{VCO}}$, while the rising edges of the dividers #2–#4 lead it by $1/4\ T_{\mathrm{VCO}}$, where T_{VCO} is the VCO output period. As a result, the average output rising edge of the vector divider is aligned with that of the reference clock.

To implement spatial averaging in circuits, we need to add up the outputs of the vector divider. It is nontrivial to directly realize averaging in the time domain. Instead, this article uses the vector PFD and the vector CP to average the vector divider output in the charge domain, as shown in Fig. 4. To make sure that the PLL loop dynamics is unchanged, each CP slice consumes $1/M$ of the CP current used in the conventional

PLL, so that the total CP current remains the same, leading to the same PLL transfer function. This way, we have

$$\frac{1}{M}\sum_{i=1}^{M}\mathrm{DivN}_i[k] = \mathrm{div}[k] \tag{2}$$

which is the basic concept of spatial averaging in the proposed PLL architecture.

The output waveforms of the vector PFD/CP and the loop filter are also shown in Fig. 5. Although ripples still appear at the loop filter output due to the phase misalignment between each single divider output and the reference clock, the amplitude of the ripples is significantly reduced compared to that in Fig. 2. This decreases the phase noise, as well as relaxing the linearity requirement of the CP, the loop filter, and the VCO. The areas of positive and negative pulses in the vector PFD output are the same, which results in *zero* net charge injected to the loop filter during every reference clock period. Hence, the width of each ripple is only one T_{VCO}, which is much smaller than that in the conventional fractional-N PLL in Fig. 2. Thus, the ripples in the proposed architecture are at much higher frequencies and can be substantially attenuated by the PLL loop dynamics.

C. Time Averaging for Arbitrary Fractional Division Ratios

With $M = 4$, the proposed spatial averaging technique can accurately produce the division ratio of not only 3.25 but also 3.5 and 3.75. 3.5 can be realized by having two dividers performing divide-by-3 and the other two performing divide-by-4. 3.75 can be achieved by having one divider performing divide-by-3 and the rest three performing divide-by-4. Generally speaking, with an M-channel spatial-averaging architecture, any fractional division ratio in the form of $N + j/M$ can be realized by having j dividers performing divide-by-$(N + 1)$ and the rest $(M - j)$ dividers performing divide-by-N, where j is an integer and $j \in [0, M - 1]$.

There remains one question to answer: what if $N + \alpha$ cannot be written in the form of $N + j/M$? For example, $N + \alpha = 3.375$ and $M = 4$. Clearly, spatial averaging alone is insufficient. To address this issue, we can bring back time averaging in the conventional fractional-N PLL. We use a DSM to produce a series of division ratios $\{\mathrm{div}[k]\}$, whose time average equals to $N + \alpha$, as indicated in (1). Even though the same time averaging concept is used, there is a key difference. In the conventional $\Delta\Sigma$ fractional-N PLL of Fig. 1, its DSM has a quantization step size of 1. The division ratio $\mathrm{div}[k]$, which is the DSM output, is an integer. $\mathrm{div}[k]$ has to switch between 3 and 4 to realize $N + \alpha = 3.375$ if the DSM is assumed to be the first order. In contrast, thanks to spatial averaging, the DSM of the proposed architecture of Fig. 4 has a finer quantization step size of $1/M$. Thus, its $\mathrm{div}[k]$ is a mixed fractional number that can be written in the form of $N + j/M$. It only needs to switch between 3.25 and 3.5 to realize $N + \alpha = 3.375$ with $M = 4$. As a result, the quantization error is reduced by M times.

In summary, by combining both spatial and time averaging, the proposed PLL architecture can realize any arbitrary fractional division ratio. Mathematically speaking, we have

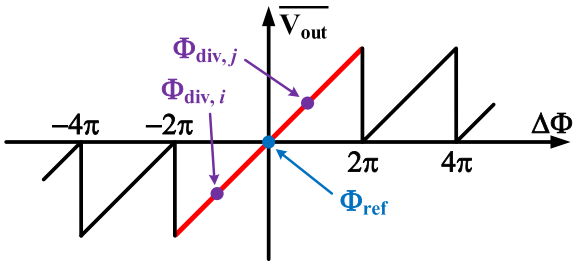

Fig. 6. Transfer characteristic of PFD.

$$N + \alpha = \underbrace{\lim_{K\to\infty}\frac{1}{K}\sum_{k=1}^{K}}_{\text{Time Averaging}}\underbrace{\frac{1}{M}\sum_{i=1}^{M}\mathrm{DivN}_i[k]}_{\text{Spatial Averaging}}. \tag{3}$$

This is also why we name it the STA PLL. Its quantization error is smaller than the conventional PLL with only time averaging.

D. Divider Selection

One key question that has not been answered is when the vector divider receives the division ratio $\mathrm{div}[k] = N + j/M$, how we select which j dividers to perform divide-by-$(N + 1)$ and which $(M - j)$ dividers to perform divide-by-N. This needs to be done carefully. We need to make sure that the rising edges of all divider outputs are close to the reference clock's rising edge, so that all PFDs work in the linear region from -2π to $+2\pi$, as shown in Fig. 6. If the phase difference between any divider output and the reference clock is beyond this range, its corresponding PFD would work in the nonlinear region, causing the spatial averaging to fail. This requirement implies that the phase difference between any two divider outputs must be within 4π, i.e., $|\Phi_{\mathrm{div},i} - \Phi_{\mathrm{div},j}| < 4\pi$. Since the divider output phase corresponds to the integration of the division ratio, this requirement can be translated to the following inequality:

$$\left|\sum_{k=1}^{K}(\mathrm{DivN}_i[k] - \mathrm{DivN}_j[k])\right| < 2N \tag{4}$$

which needs to be satisfied for any integer i, j, and K.

It is nontrivial to meet (4). There are two simple strategies to perform the divider selection. One is to perform a thermometer mapping. That is, given $\mathrm{div}[k] = N + j/M$, we set DivN_1 to DivN_j to be $N + 1$, and set DivN_{j+1} to DivN_M to be N. However, this means DivN_1 is always greater than DivN_M. As a result, the accumulated phase difference would go out of bound, which violates (4). The other simple strategy is to randomly select dividers with the division ratios of N or $N+1$. This strategy may seem to work, as it guarantees there is no systematic bias in the divider selection, and the averaged divider output frequencies are the same. However, this is still insufficient, as the accumulated phase difference can still go out of bound. To meet (4), we essentially need the spectrum of $\{\mathrm{DivN}_i[k]\}$ to be high-pass shaped with a zero at dc.

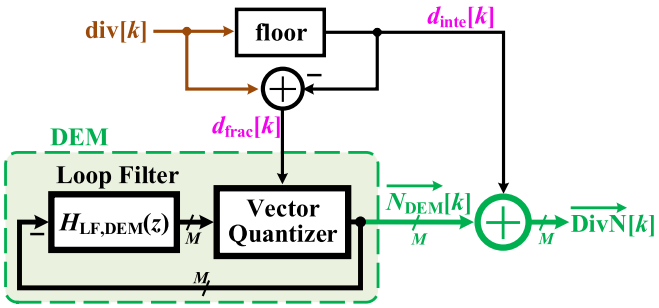

Fig. 7. Block diagram of the vector division ratio generator.

It may appear that we need to invent a new circuit to generate the right vector division ratio $\overrightarrow{\text{DivN}}[k]$, but it turns out that the requirements of (2) and (4) are exactly the same as the requirements for the DAC mismatch shaping in an analog multi-bit DSM [42]–[44]. Thus, we can directly borrow the dynamic element matching (DEM) technique and implement the vector division ratio generator of Fig. 4 by a DEM block. In the analog DSM, the DAC selection pattern is scrambled to ensure that each DAC element is turned on for the same number of times in order to shape the DAC mismatch error. Here, in the proposed STA PLL, we scramble the divider selection pattern to ensure that each divider has the same number of times with the division ratio of $N+1$, so that the divider output phases always stay close to one another.

Fig. 7 shows the block diagram of the vector division ratio generator in the proposed STA PLL, where the DEM block is, for instance, implemented using the vector-quantizer architecture [42]. The input div$[k]$ is first separated into the integer and the fractional parts, which are represented by $d_{\text{inte}}[k]$ and $d_{\text{frac}}[k]$, respectively. $d_{\text{frac}}[k]$ is processed by the DEM block and converted into an M-element integer-value vector, $\overrightarrow{N_{\text{DEM}}}[k]$. Finally, $\overrightarrow{N_{\text{DEM}}}[k]$ and $d_{\text{inte}}[k]$ are added together to obtain the vector division ratio $\overrightarrow{\text{DivN}}[k]$. Mathematically speaking, we have

$$\text{DivN}_i[k] = d_{\text{inte}}[k] + N_{\text{DEM},i}[k]. \tag{5}$$

If the DEM loop filter is a simple integrator, i.e., $H_{\text{LF,DEM}}(z) = z^{-1}/(1-z^{-1})$, it implements the data-weighted averaging (DWA) technique, which is the most widely used first-order DEM technique [43]. The barrel-shifting $\overrightarrow{\text{DivN}}[k]$ pattern shown in Table I is the result of the DWA technique. We can also realize higher order shaping by increasing the order of $H_{\text{LF,DEM}}(z)$ [42], [44]–[46]. Note that the DEM order needs to be at least one to cancel the first-order frequency-to-phase integration of the divider to satisfy (4).

E. Loop Response and Quantization Noise Analyses

Fig. 8 shows the phase-domain model of the proposed STA PLL. Its closed-loop transfer function can be derived as

$$G_{\text{closed}}(f) = \frac{\Phi_{\text{VCO}}(f)}{\Phi_{\text{ref}}(f)} = \frac{(N+\alpha)G_{\text{open}}(f)}{1+G_{\text{open}}(f)} \tag{6}$$

where the open-loop transfer function is

$$G_{\text{open}}(f) = K_{\text{PFD}} I_{\text{CP}} H_{\text{LF}}(f) \frac{K_{\text{VCO}}}{jf} \frac{1}{N+\alpha} \tag{7}$$

where K_{PFD} is PFD gain, I_{CP} is the total current of the vector CP, $H_{\text{LF}}(f)$ is the loop filter transfer function, and K_{VCO} is the VCO tuning gain. Note that (6) and (7) are exactly the same as the closed- and open-loop transfer functions of the conventional fractional-N PLL derived in [47], which proves that the proposed STA technique does not change the PLL loop dynamics.

Fig. 9 compares the simulated VCO control voltage of an 8-channel STA PLL with a conventional fractional-N PLL and an 8-tap FIR PLL under the same loop parameters. As expected, the proposed STA PLL and the conventional fractional-N PLL have the same settling time. Due to the delay of the register chain, the FIR PLL settles slower ($\sim 8T_{\text{ref}}$). The main differences among the three PLLs are the amplitudes of the ripples on the VCO control voltage. The ripple amplitude of the proposed STA PLL is eight times smaller than that of the conventional fractional-N PLL and is also smaller than that of the FIR PLL. The significant reduction on the ripple amplitude directly reflects the stronger quantization error suppression of our proposed STA technique, which matches the earlier analyses.

In Fig. 8, the DSM quantization error is modeled as e_q, which is high-pass shaped by its noise transfer function (NTF) $\text{NTF}_{\text{DSM}}(z)$. As the quantization step of the DSM in the proposed STA PLL is $1/M$, the magnitude of e_q is M times smaller than that of the conventional fractional-N PLL. Assuming e_q is uniformly distributed and $\text{NTF}_{\text{DSM}}(z) = (1-z^{-1})^L$, the quantization noise PSD at the output of the proposed STA PLL can be derived as

$$S_{\text{QN}}(f) = \frac{1}{M^2}\frac{\pi^2 T_{\text{ref}}}{3}\left|\frac{G_{\text{closed}}(f)}{N+\alpha}\right|^2 |1-z^{-1}|^{2L-2} \tag{8}$$

which indicates that the STA PLL has a $20\log_{10} M$ dB reduction to the quantization noise at all frequencies compared to the conventional fractional-N PLL. Note that the proposed STA PLL has no limit on the DSM structure and NTF, which means that both the single-loop and the multi-stage noise shaping (MASH) modulators are applicable to the proposed STA technique.

Fig. 10 compares the output quantization noise spectra of the conventional fractional-N PLL, the 8-tap FIR PLL presented in [35], and the proposed STA PLL with $M=8$ and 16, respectively, under the same loop parameters and $\text{NTF}_{\text{DSM}}(z) = (1-z^{-1})^3$. As shown, the proposed STA PLL reduces the quantization noise over the entire frequency range by 18 dB for $M=8$ and 24 dB for $M=16$. Although the FIR filtering technique proposed in [35] shows similar attenuation for high-frequency noise, it cannot reduce the low-frequency noise. In addition, its noise peak magnitude is 12-dB higher than that of the 8-channel STA PLL.

F. Mismatch Analyses

1) Gain Mismatch Analysis: Since the proposed STA PLL uses an array of dividers, PFDs, and CPs, a problem that

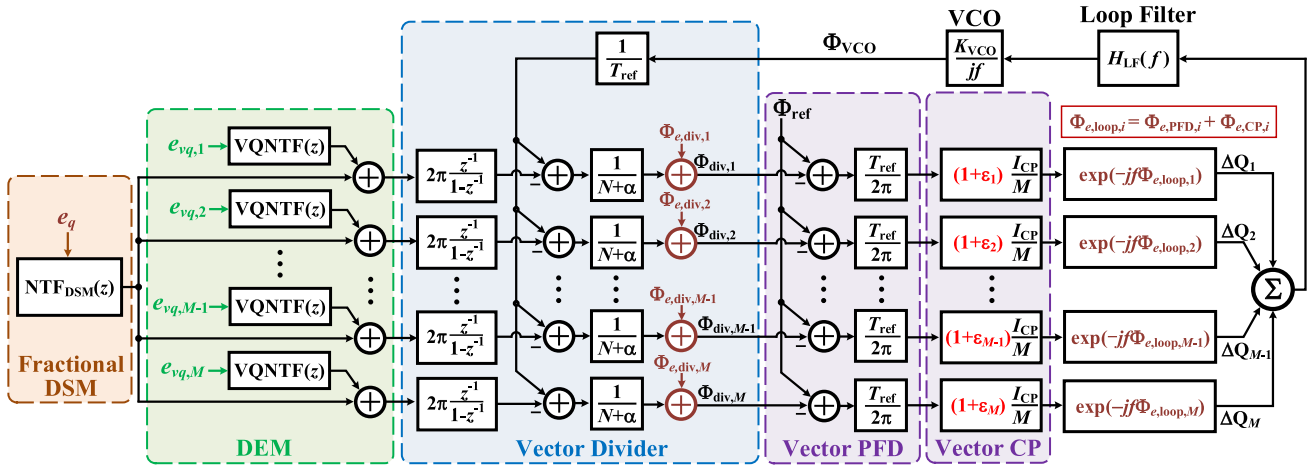

Fig. 8. Phase-domain model of the proposed STA PLL.

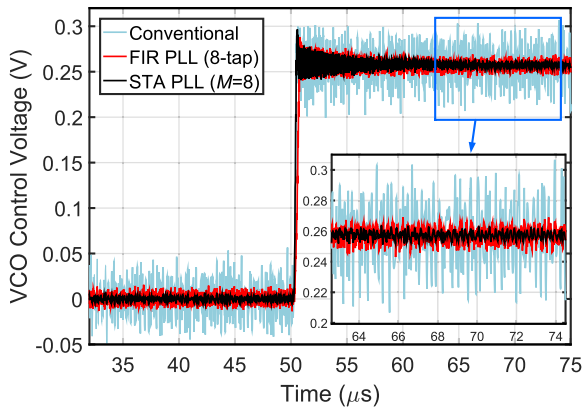

Fig. 9. VCO control voltage comparison.

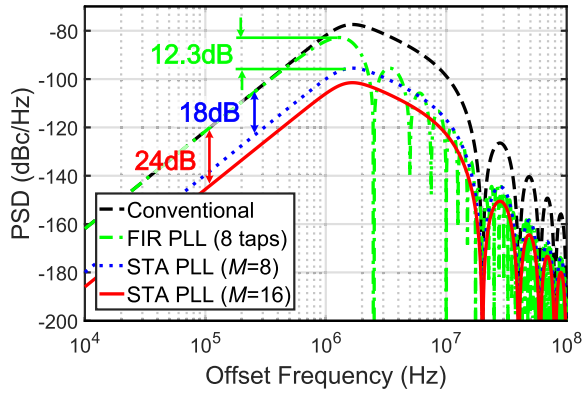

Fig. 10. Comparison of the output quantization noise.

naturally arises is the gain mismatch among different channels. Due to the digital nature of the PFD and the divider, their gains in the phase domain are fixed by their topology, and thus, do not have mismatch. The only gain mismatch is from the vector CP due to current source mismatch. In Fig. 8, the percentage mismatch of the ith CP slice is denoted as ε_i. For simplicity, we still define the total current of the vector CP with mismatch as $I_{\rm CP}$, and thus, we have $\sum_{i=1}^{M}\varepsilon_i = 0$. Therefore, the PLL closed-loop transfer function is unchanged and is still given by (6). Likewise, the transfer functions of the loop-filter noise, the VCO phase noise, and the DSM quantization noise remain the same. Nevertheless, the gain mismatch affects the vector quantization error of the DEM block. In Fig. 8, we use $\overrightarrow{e_{vq}}$ to represent the DEM vector quantization error. From the definition of the vector quantization error and (2), we have $\sum_{i=1}^{M} e_{vq,i}[k] = 0$. This means that, if there is no gain mismatch, $\overrightarrow{e_{vq}}$ would be canceled out naturally in the charge domain at the input of the loop filter. Thus, $\overrightarrow{e_{vq}}$ itself does not contribute phase noise at the PLL output. However, due to the presence of the CP current mismatch, the gain of the ith element of $\overrightarrow{e_{vq}}$ becomes $(1+\varepsilon_i)$ rather than unity. As a result, the summation $\sum_{i=1}^{M}(1+\varepsilon_i)e_{vq,i}$ $= \sum_{i=1}^{M}(\varepsilon_i \cdot e_{vq,i})$ is no longer zero and shows up as phase noise at the PLL output. Assuming the standard deviation of ε_i is σ and $e_{vq,i}$ is uniformly distributed, the phase noise due to the vector CP mismatch is given by

$$S_{\rm MN}(f) = \frac{1}{M}\frac{\pi^2\sigma^2 T_{\rm ref}}{3}\left|\frac{G_{\rm closed}(f)}{N+\alpha}\right|^2\left|\frac{\rm VQNTF(z)}{1-z^{-1}}\right|^2 \tag{9}$$

where VQNTF(z) is the vector quantization NTF of the DEM block. If DWA is used, VQNTF$(z) = (1-z^{-1})$. Thus, (9) can be derived as

$$S_{\rm MN}(f) = \frac{1}{M}\frac{\pi^2\sigma^2 T_{\rm ref}}{3}\left|\frac{G_{\rm closed}(f)}{N+\alpha}\right|^2. \tag{10}$$

It shows that the first-order shaped mismatch noise by DWA cancels out the frequency-to-phase integration of the divider, and thus, the vector CP current mismatch-induced phase noise shows up as white noise filtered by $G_{\rm closed}(f)$ at the PLL output.

Fig. 11 compares the simulated output frequency spectra of the proposed STA PLL, the conventional fractional-N PLL, and the FIR PLL with only the DSM quantization noise and the mismatch induced noise under different conditions. As expected, the vector CP mismatch shows up as white noise and flattens out the notch at the PLL output frequency. Nevertheless, the impact of vector CP mismatch is small. Comparing Fig. 11(a)–(c), the total rms jitter of the proposed STA PLL hardly changes with $\sigma = 1\%$ vector CP mismatch. It only mildly increases from 3.1 to 3.4 ps with a large $\sigma = 5\%$ vector

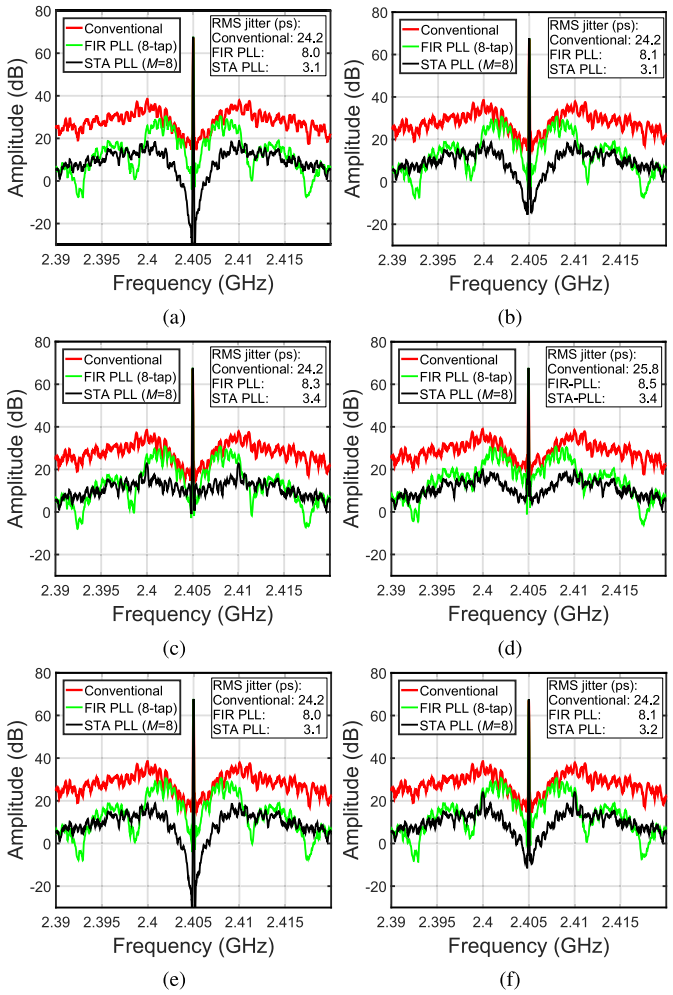

Fig. 11. Simulated output spectra with (a) no mismatch, (b) $\sigma = 1\%$ vector CP mismatch, (c) $\sigma = 5\%$ vector CP mismatch, (d) $\sigma = 5\%$ vector CP mismatch plus 5% up/down CP current mismatch, (e) $\sigma = 4.4$-ps divider delay mismatch, and (f) $\sigma = 2.3$-ps loop delay mismatch.

CP mismatch, but still much smaller than the conventional PLL and the FIR PLL, which are 24.2 and 8.3 ps, respectively, under the same simulation condition.

In addition to the vector CP mismatch, each CP slice may suffer from another mismatch due to the unequal charging and discharging currents. Fig. 11(d) shows the simulated output spectra with both $\sigma = 5\%$ vector CP current mismatch and 5% up/down CP current mismatch. As shown, the rms jitter is the same as that in Fig. 11(c), where only $\sigma = 5\%$ vector CP current mismatch is included. This indicates that the impact of this mismatch is insignificant to the proposed STA PLL. In fact, the up/down CP current mismatch is also a common issue in conventional fractional-N PLLs, and techniques to address this issue, such as [48]–[50], are applicable to the proposed STA technique.

2) Delay Mismatch Analysis: For any divider, PFD, and CP element in the array, there may be a propagation delay mismatch, which are represented as $\overrightarrow{\Phi_{e,\text{div}}}$, $\overrightarrow{\Phi_{e,\text{PFD}}}$, and $\overrightarrow{\Phi_{e,\text{CP}}}$ in Fig. 8, respectively. Based on the different impacts of the phase noise, these delay mismatches can be divided into two categories: the divider delay mismatch and the loop delay mismatch. The divider delay mismatch comes from the different clock-to-Q delays of the D flip-flops (DFFs) in the vector divider and the wire length difference among the M divider-to-PFD paths. As PFD detects the phase difference between the reference clock and the divider output, this mismatch generates a constant phase error $\Phi_{e,\text{div},i}$ at the input of the ith element of the vector PFD. After summed and averaged, the phase error is finally converted into a phase offset at the PLL output. However, this phase offset does not influence the loop response of the PLL. Fig. 11(e) plots the simulated output spectra with $\sigma = 4.4$-ps divider delay mismatch. As shown, the spectra and rms jitter are the same as that of the ideal case in Fig. 11(a), which matches the analysis. In the simulation, the standard deviation of 4.4 ps is obtained from Monte Carlo (MC) simulation.

The loop delay mismatch, including $\overrightarrow{\Phi_{e,\text{PFD}}}$ and $\overrightarrow{\Phi_{e,\text{CP}}}$, is caused by the propagation delay difference among the M channels in the vector PFD and the vector CP. This mismatch introduces a phase shift term $\exp(-jf\Phi_{e,\text{loop},i})$ to the gain of the ith channel, where $\Phi_{e,\text{loop},i} = \Phi_{e,\text{PFD},i} + \Phi_{e,\text{CP},i}$. As a result, the ith element of the DEM vector quantization error $\overrightarrow{e_{vq}}$ has to be multiplied by $\exp(-jf\Phi_{e,\text{loop},i})$, which causes the summation $\sum_{i=1}^{M} e_{vq,i} \cdot \exp(-jf\Phi_{e,\text{loop},i})$ to be nonzero, and shows up as additional phase noise at the PLL output. Fig. 11(f) shows the simulation results with a typical $\sigma = 2.3$ ps loop delay mismatch from MC simulation. As shown, the loop mismatch slightly increases the in-band phase noise, leading to the rms jitter rising from 3.1 to 3.2 ps. However, the proposed STA PLL still performs better quantization noise reduction than the conventional fractional-N PLL and the FIR PLL.

IV. Spatial Averaging With a Single Divider

The spatial averaging technique in Fig. 4 requires an array of M dividers. Since the divider operates at the VCO output frequency, the total divider power would increase by M times, which can be a significant power penalty, especially for a large M. To reduce power, this section presents a way to realize spatial averaging with only a single divider.

Let us again take a look at Fig. 5, in which the vector division ratio $\overrightarrow{\text{DivN}_i[k]}$ is generated by using DWA. Note that the phase difference between any two divider outputs is either 0 or T_{VCO}. This is due to the barrel-shifting nature of DWA, which ensures that the accumulated vector division ratios differ at most by 1 from one another. Mathematically speaking, it means

$$\left|\sum_{k=1}^{K}(\text{DivN}_i[k] - \text{DivN}_j[k])\right| \leq 1. \tag{11}$$

This formula means that the divider output phases are not independent. Fig. 12 replots the output phases. As shown, for every reference clock rising edge, there are only two possible choices of phases among all dividers: a leading phase Φ_{Lead} marked in pink and a lagging phase Φ_{Lag} marked in blue. Hence, as long as we can generate these two phases and perform correct selection between them, we can produce all required divider output phases. Since Φ_{Lag} always lags Φ_{Lead}

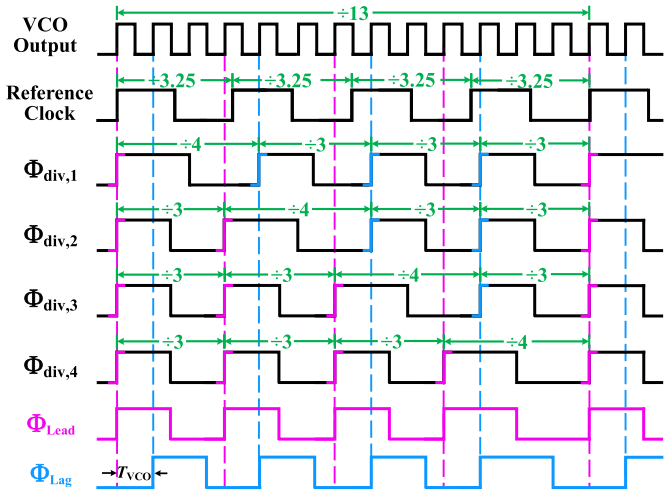

Fig. 12. Time-domain waveform of the spatial averaging with a single divider and phase selection.

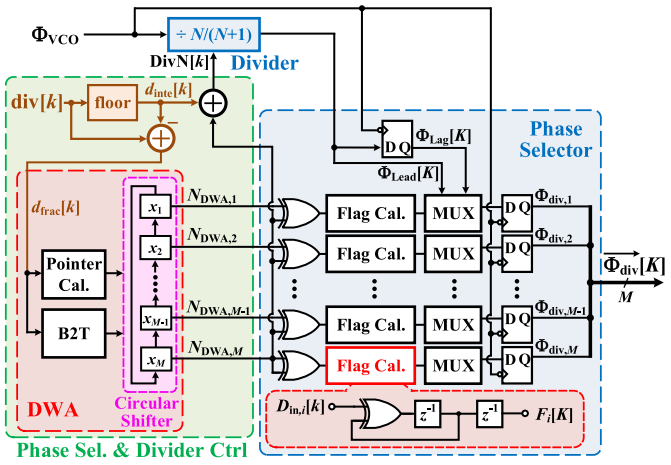

Fig. 13. Circuit implementation of spatial averaging with a single divider and phase selection.

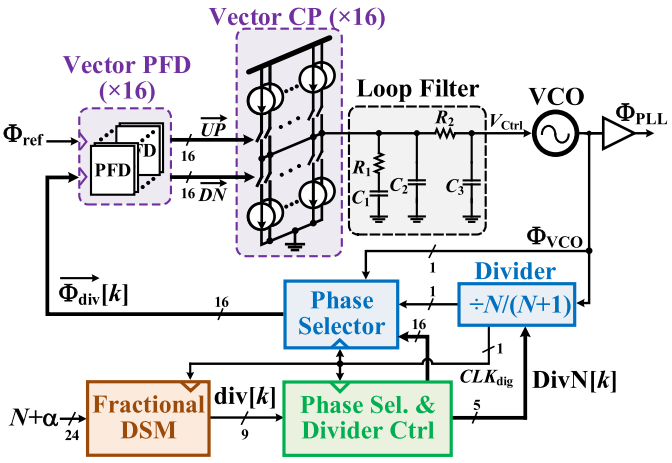

Fig. 14. Block diagram of the proposed fractional-*N* PLL.

by T_{VCO}, we can use *only one divider* to generate Φ_{Lead} and delay it by one T_{VCO} to obtain Φ_{Lag}. In addition, by carefully examining Fig. 12, we can see that the rising edge of the last divider #4 always leads that of the other three dividers, and thus, we can simply use divider #4 to produce Φ_{Lead} and delay it to get Φ_{Lag}. All other dividers can be removed. Note that even though Fig. 12 is a special example with $M = 4$ and $N + \alpha = 3.25$, the proposed one-divider scheme is valid for any M and $N+\alpha$, which is guaranteed by the nature of DWA.

To perform the correct phase selection, we need to know the relationship between any divider output phase $\Phi_{div,i}[K]$ and that of the last divider $\Phi_{div,M}[K] = \Phi_{Lead}[K]$. For simplicity, let us express $\Phi_{div,i}[K]$ as the accumulated number of VCO clock cycles

$$\Phi_{div,i}[K] = \sum_{k=1}^{K} \mathrm{DivN}_i[k] = \sum_{k=1}^{K} (d_{inte}[k] + N_{DWA,i}[k]). \quad (12)$$

Since $d_{inte}[k]$ is common to all dividers (see Fig. 7), it is easy to derive that

$$\Phi_{div,i}[K] = \Phi_{div,M}[K] + \sum_{k=1}^{K} (N_{DWA,i}[k] - N_{DWA,M}[k]). \quad (13)$$

As mentioned earlier, since DWA ensures that $F_i[K] \equiv \sum_{k=1}^{K} (N_{DWA,i}[k] - N_{DWA,M}[k])$ can only take the value of 0 or 1, we can rewrite (13) as

$$\Phi_{div,i}[K] = \begin{cases} \Phi_{Lead}[K], & \text{for } F_i[K] = 0 \\ \Phi_{Lag}[K], & \text{for } F_i[K] = 1 \end{cases} \quad (14)$$

which clearly shows that $\Phi_{div,i}[K]$ can be obtained via phase selection between $\Phi_{Lead}[K]$ and $\Phi_{Lag}[K]$ based on the value of the flag $F_i[K]$.

Fig. 13 shows the direct circuit implementation. A standard DWA block is used to produce $\overrightarrow{N_{DWA,i}}[k]$. The last DWA output $N_{DWA,M}[k]$ is sent to the single divider to produce $\Phi_{Lead}[K]$ and $\Phi_{Lag}[K]$. Since both $N_{DWA,i}[k]$ and $F_i[K]$ can only take the value of 0 or 1, $F_i[K]$ can be simply realized using XOR gates for subtraction and addition without the need for full-blown digital subtractors or adders. A multiplexer uses $F_i[K]$ to select either $\Phi_{Lead}[K]$ or $\Phi_{Lag}[K]$. Finally, a retiming DFF is used to reduce the phase mismatch among M channels. Note that the proposed single-divider spatial averaging technique looks like the PI technique, but they work differently. Instead of selecting among multiple phases generated by a sophisticated phase interpolator, the proposed technique realizes the instantaneous fractional frequency division with only two phases produced by a single DFF. This technique is highly digital and PVT robust. In addition, with the proposed technique, the resolution of the fractional frequency division can be adjusted simply by changing the number of channels.

V. Circuit Implementation

To verify the proposed STA technique, a prototype 2.4-GHz $\Delta\Sigma$ fractional-*N* PLL is implemented. Fig. 14 shows the top-level block diagram, which is based on a type-II PLL. 16 PFDs and CPs are used for spatial averaging.

Fig. 15 shows the block diagram of the fractional DSM, which is the third order and can provide a fine quantization step of 1/16. In this way, the quantization noise can be reduced by 24 dB over the entire frequency range. The DSM adopts the cascade-of-resonators-feedback (CRFB) structure with an

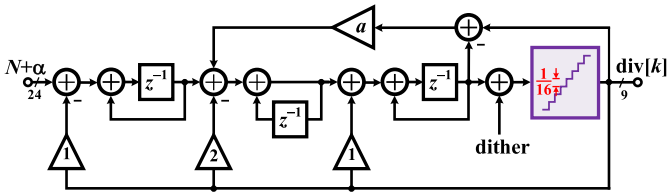

Fig. 15. Block diagram of the fractional DSM.

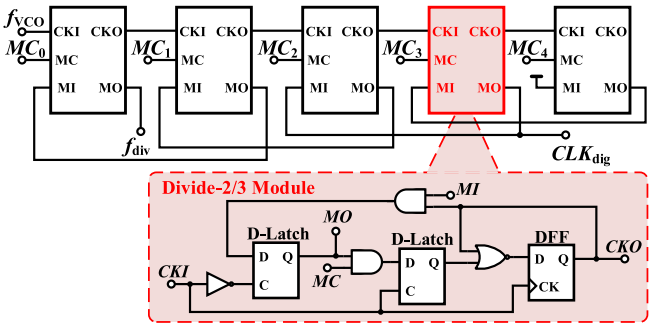

Fig. 16. Schematic of the only divider.

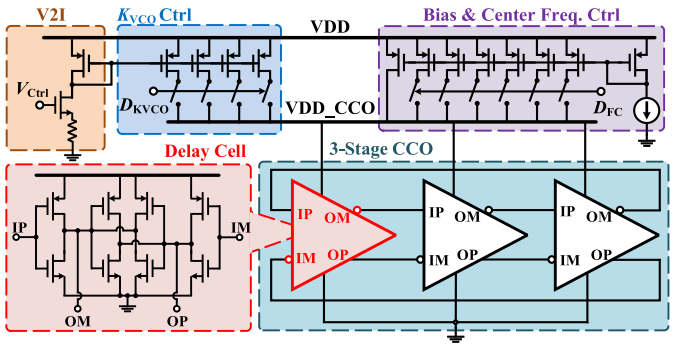

Fig. 17. Schematic of the VCO.

internal feedback factor of $a = 1/16$ to realize a pair of complex zeros at 2 MHz. Although this way changes the quantization error below 2 MHz to be the first-order shaped, the overall quantization noise of the PLL can be reduced due to a notch in NTF. In order to clearly demonstrate the benefits of the proposed STA technique, the DSM is designed to have a reconfigurable quantization step that can vary among $\{1, 1/2, 1/4, 1/8, 1/16\}$ simply by changing the number of fractional bits in div$[k]$.

Instead of using an array of 16 dividers as shown in Fig. 4, the prototype adopts the more power-efficient single-divider scheme of Fig. 13. Fig. 16 shows the schematic of the only divider, which is implemented by cascading five divide-2/3 modules, providing a frequency division range from 32 to 63.

The loop filter is a third-order passive filter, which supports a 2.76-MHz closed-loop bandwidth. Fig. 17 shows the VCO schematic. The VCO core is a three-stage current-controlled oscillator (CCO) made of cross-coupled inverters. The control voltage V_{Ctrl} from the loop filter is converted to current via a voltage-to-current (V2I) block. The typical VCO tuning gain is 300 MHz/V, which can be adjusted by D_{KVCO}. The center frequency of the VCO is controlled by D_{FC} to support a wide output frequency range.

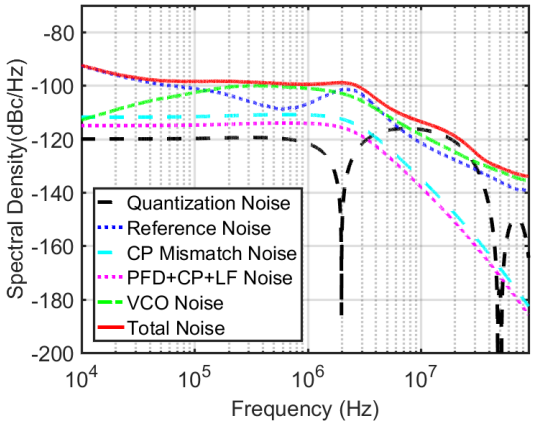

Fig. 18. Simulated phase noise of the proposed fractional-N PLL with main contributors.

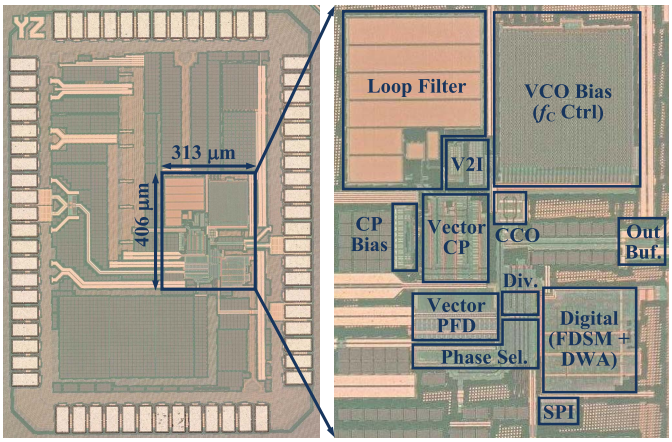

Fig. 19. Die photograph of the proposed STA PLL.

Fig. 18 plots the simulated phase noise of the proposed fractional-N PLL prototype, in which all noises are referred to the PLL output. Note that, the first-order shaped quantization noise at frequencies below 2 MHz cancels the frequency-to-phase integration of the divider and becomes flat at in-band frequencies. Thanks to the proposed STA technique, the quantization noise becomes the nondominant phase noise source at both the in-band and out-of-band frequencies, except in 10–30 MHz. Within this frequency range, the quantization noise peak raises the output phase noise by around 3 dB compared to the VCO phase noise. The phase noise induced by the vector CP current mismatch is also shown in Fig. 18. As shown, although the mismatch noise increases the in-band phase noise, it is much lower than the phase noise contributed by the VCO and the reference clock, which are the two main phase noise sources in the proposed PLL prototype and dominate at almost the entire frequency range.

VI. Measurement Results

The prototype PLL is fabricated in a 40-nm CMOS process. Fig. 19 shows the die photograph, whose core area is 0.086 mm^2. The output frequency ranges from 1.67 to 3.12 GHz with a reference clock frequency f_{ref} of 50 MHz.

Fig. 20 shows the measured output spectrum at the integer-N mode with $N = 48$. The PLL output frequency is 2.4 GHz.

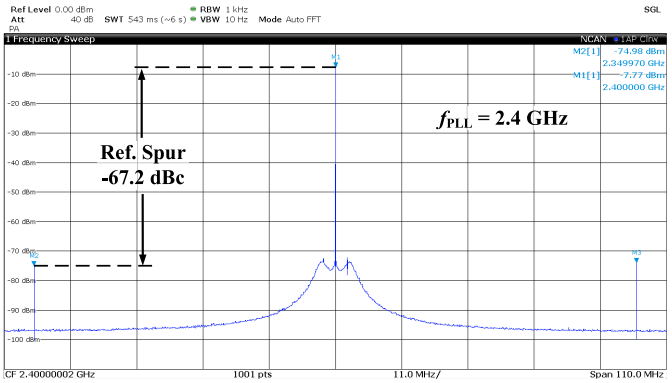

Fig. 20. Measured output spectrum at the integer-N mode with $N = 48$.

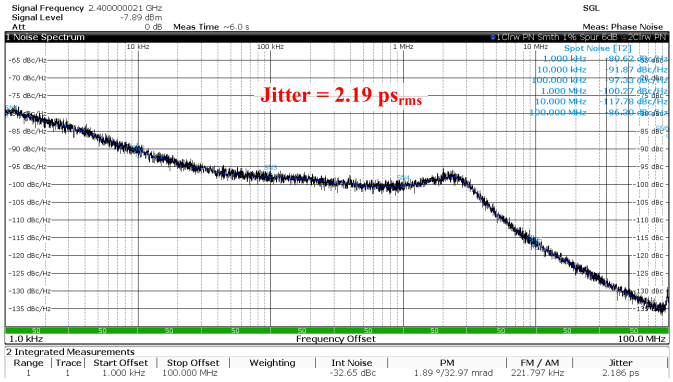

Fig. 21. Measured output phase noise at the integer-N mode with $N = 48$.

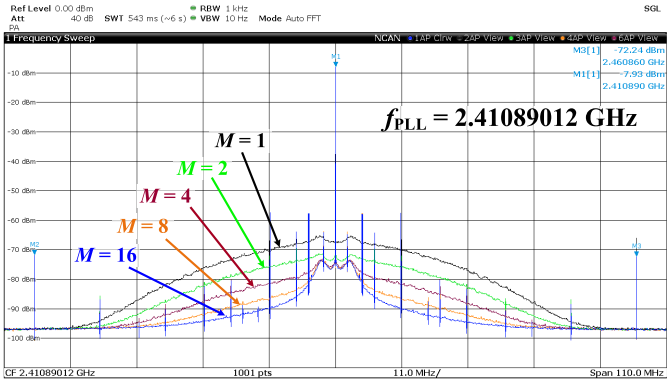

Fig. 22. Measured output spectra at the fractional-N modes with different M values.

The measured reference spur is −67.2 dBc. Fig. 21 plots the measured output phase noise at this mode. As shown, with a closed-loop bandwidth of 2.76 MHz, the in-band (at 1 MHz) and the output-of-band (at 10 MHz) phase noise are −100 and −118 dBc/Hz, respectively. By integrating the phase noise from 1-kHz to 100-MHz frequency offset, the rms jitter is 2.19 ps.

Fig. 22 compares the measured output frequency spectra with $M = 1, 2, 4, 8, 16$ and a general fractional frequency division ratio that cannot be written as $N + j/16$ (where N and j are integers). Specifically, when $M = 1$, the DSM quantization step is 1, and thus, the prototype PLL returns to the conventional fractional-N PLL. As shown, the proposed STA technique improves the output phase noise at all frequencies. When M is small, the improvement rate is 6 dB per every

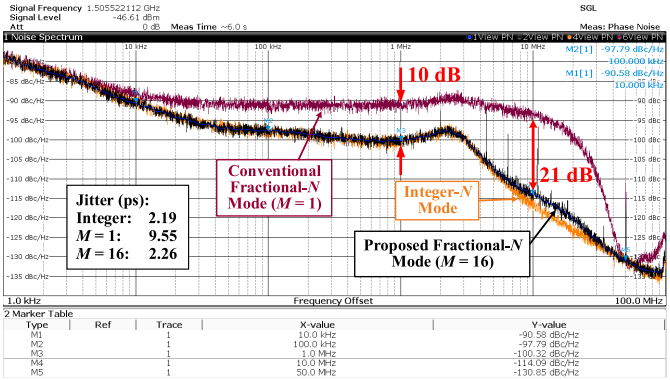

Fig. 23. Phase noise of the integer-N mode and the fractional-N modes with $M = 1$ and $M = 16$.

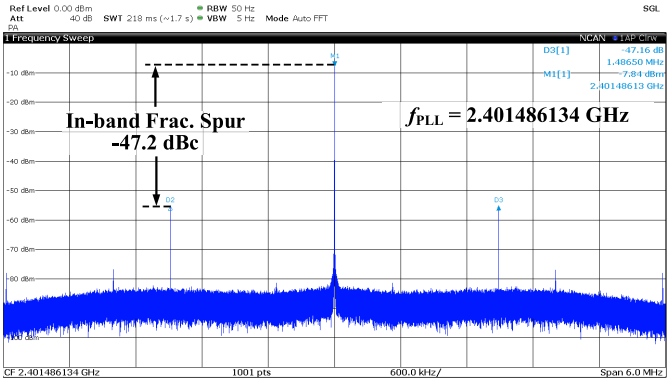

Fig. 24. Measured in-band fractional spur.

TABLE II
INTEGRATED RMS JITTER SUMMARY

Modes		Integrated rms Jitter (ps)
Integer-N		**2.19**
Fractional-N	$M = 1$	9.55
	$M = 2$	4.90
	$M = 4$	3.06
	$M = 8$	2.45
	$M = 16$	**2.26**

doubling of M, which matches the analyses in Section III. When M is above 4, the in-band noise improvement is less significant, as it starts to be dominated by other noise sources, such as the input reference noise and the VCO noise. The out-of-band noise improvement still follows the $20\log_{10} M$ (dB) trend, until $M = 16$ when the out-of-band noise starts to be dominated by the VCO noise.

Fig. 23 compares the measured output phase noise at $M = 1$ and $M = 16$ with that of the integer-N mode. Compared to the conventional architecture (i.e., $M = 1$), the proposed PLL with $M = 16$ reduces the in-band and out-of-band phase noise by 10 and 21 dB, respectively. The integrated rms jitter is reduced from 9.55 to 2.26 ps. Again, the measurement result in the fractional-N mode with $M = 16$ is almost the same as the integer-N mode. The only difference is the 3-dB higher noise in the range of 10–30 MHz, which comes from the peak of the quantization noise as Fig. 18 shows. Table II summarizes the integrated rms jitters at different modes. The rms jitter decreases with the increase of M due to the reduced

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	Yu [35] JSSC '09 Type-II	Jee [29] JSSC '13 Type-II	Kao [30] ISSCC '13 Type-II	Nandwana [31] JSSC '15 Type-II	Liang [51] ISSCC '15 Type-II	Elkholy [24] JSSC '16 Type-II	Kong [37] JSSC '18 Type-I	**This work Type-II**
Quan. Noise Reduction Tech.	8-tap FIR	PI & 8-tap FIR	Segmented PI	Hybrid-P/C PI	Switch Cap. LF	DTC cancel	35-tap FIR	**16-channel STA**
Technology (nm)	180	130	40	65	40	65	45	**40**
Reference Freq. (MHz)	27	32	26	50	26	50	22.6	**50**
Output Freq. (GHz)	0.17–1.25	0.86–1.26	1.87–1.98	4.25–4.75	2	2.0–5.5	2.31–3.05	**1.67–3.12**
Bandwidth (MHz)	1	3.2	2	12	1.51	5	5.65	**2.76**
In-band Phase Noise (dBc/Hz)	N/A	−106 (@ 100kHz)	−98 (@ 1MHz)	−104 (@ 400kHz)	−98 (@ 1MHz)	−97 (@ 1MHz)	−104 (@ 1MHz)	**−100 (@ 1MHz)**
Out-of-band Phase Noise (dBc/Hz)	N/A	−107.5 (@ 6MHz)	−115 (@ 10MHz)	N/A	−115 (@ 10MHz)	N/A	−121.4 (@ 10MHz)	**−114 (@ 10MHz)**
Ref. Spur (dBc)	N/A	−66	−67	−60	−87	−44	−60	**−67.2**
Power (mW)	6.1	16.8	10	11.6	9.1	4	10	**4.85**
Active Area (mm^2)	0.5	0.31	0.055	0.48	0.046	0.084	0.096	**0.086**
RMS Jitter (ps) Integ. Range (MHz)	17.3 (1–100)	N/A	3.4 (0.004–40)	1.46 (0.002–20)	2.4 (0.001–40)	1.86 (0.01–100)	1.5 (0.01–50)	**2.26 (0.001–100)**
FoM[1](dB)	−207.4	N/A	−219.4	−225.8	−222.8	−228.5	−226.5	**−226.1**

[1] $\text{FoM} = 10\log_{10}\left[\left(\frac{\text{Jitter}_{\text{rms}}}{1\text{ sec}}\right)^2\left(\frac{\text{Power}}{1\text{ mW}}\right)\right]$

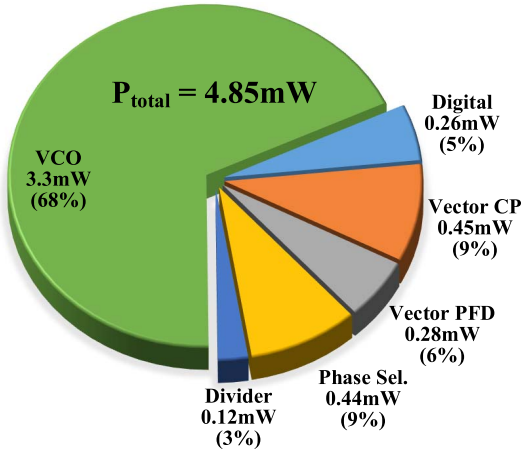

Fig. 25. Measured power breakdown.

DSM quantization error. These results clearly prove the benefit of the proposed STA PLL architecture in quantization noise reduction.

Fig. 24 shows the measured fractional spur performance with $N+\alpha = 48.0625-(2^{-10}+2^{-14}+2^{-19})$. With the PLL bandwidth of 2.76 MHz, the in-band fractional spur magnitude is measured to be −47.2 dBc.

The total power of the prototype PLL with 2.4-GHz output frequency is 4.85 mW from the 1.1-V power supply, where 3.3 mW is consumed by the VCO. Fig. 25 shows the measured power breakdown. The combined power of the divider and the phase selection block is 0.56 mW. It is much smaller than the total power consumed by an array of 16 dividers, which would be more than 2 mW. This shows the benefit of the one-divider scheme of Section IV in reducing the divider power.

Table III summaries and compares the performance of the proposed PLL with the state-of-the-art wide-bandwidth PLLs. The prototype PLL achieves a jitter figure of merit (FoM) of −226.1 dB, which is in line with the state-of-the-art works.

VII. CONCLUSION

This article presented a highly digital and calibration-free technique that can significantly reduce the quantization noise of fractional-N PLLs over the entire frequency range. In this technique, the instantaneous fractional frequency division is achieved through spatial averaging by using an array of dividers, PFDs, and CPs. To reduce the power of the divider array, a method is proposed to realize the spatial averaging with a single divider and phase selection. Based on the proposed STA technique, a 2.4-GHz $\Delta\Sigma$ fractional-N PLL is implemented. The measurement results show that the quantization noise has been significantly reduced. Hence, the fractional-N PLL can almost achieve the same phase noise and jitter as an integer-N PLL.

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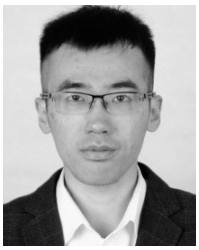

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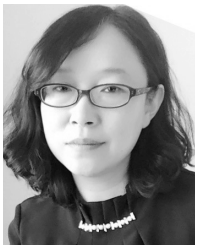

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