0.13pW/Hz Ring VCO-Based Continuous-Time Read-Out ADC for Bio-Impedance Measurement

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***Abstract*—This work presents a continuous-time ring voltage-controlled oscillator (VCO)-based second-order $\Delta\Sigma$ analog-to-digital converter (ADC) for bio-impedance measurement. The proposed ADC addresses several limitations of prior works which pre-dominantly use successive approximation register (SAR) ADC, such as kickback noise from sampling circuit and power hungry driver required to drive large sampling capacitance of SAR ADC. A current-reuse architecture is used to reduce power consumption and input-referred noise of the proposed ADC. The ADC is implemented in 65nm CMOS process and used for measuring amplitude and phase of a phantom which models skin impedance. A digital matched filter is used to extract amplitude and phase of the impedance of the phantom. The ADC measures amplitude with a maximum error of 2.8% and measures phase with a maximum error of 0.86° over a frequency range of 1-300kHz. The ADC has a mean SNR of 67dB with a power efficiency of 0.13pW/Hz which is 9x better than state-of-the-art.**

***Index Terms*—analog-to-digital converter, bio-impedance, continuous-time $\Delta\Sigma$, electrical impedance tomography, noise shaping, voltage controlled oscillator (VCO)**

I. Introduction

Bio-impedance measurement has a variety of medical applications, such as lung ventilation monitoring through electrical impedance tomography (EIT), cancerous tissue detection, spectroscopy for impedimetric immunosensors, etc. Out of the different applications, EIT is a promising and well studied technique for non-invasive imaging of the interior of a body based on impedance measurements on the skin. EIT measurement for human tissue is usually performed by injecting an ac current through two electrodes and measuring the boundary voltage induced at the other electrodes. A complete EIT systems comprises of i) a current source; ii) data acquisition block; and iii) reconstruction of conductivity map from acquired impedance data. The focus of this work is the data acquisition block.

Data acquisition of existing EIT systems is overwhelmingly performed using successive approximation register (SAR) analog-to-digital converter (ADC) [1]–[5]. This is understandable since SAR is a popular architecture for medium resolution ADCs (10-12 bits) due to simplicity of design and highly digital nature. However, SAR ADC comes with two limitations - a) the switched capacitor digital-to-analog converter (DAC) creates kickback noise during sampling; and b) power-hungry ADC driver is needed to drive the large sampling capacitor [1]. While [1] uses a pipelined sampling and conversion stage to reduce power, the ADC driver still consumes significant power.

In this work, we propose a continuous-time (CT) ring voltage-controlled oscillator (VCO)-based $\Delta\Sigma$ ADC for impedance measurement that can address the aforementioned limitations of SAR ADC. While research on VCO-ADC has gained a lot of traction in recent years, VCO-ADC has not been used so far as read-out for bio-impedance measurements. A ring VCO converts analog input voltage into time-domain (TD) and performs a TD-integration before the VCO output is sampled and quantized. By performing the integration over a long time, VCO-ADC can quantize small input signals with high SNR. The CT nature ensures there is no kickback to the input since sampling happens after quantization. The proposed ADC is the second iteration of our previous VCO-based $\Delta\Sigma$ ADC reported in [6]. The key difference of this work from our prior work is the use of a current-reuse DAC architecture which improves ADC energy efficiency by more than 2x. The current-reuse architecture is discussed in detail in Section II. The ADC is implemented in 65nm CMOS process, and the test chip improves power efficiency by almost 9x while maintaining similar SNR as state-of-the-art [1]. The rest of this paper is organized as follows: Section II presents the architecture of the ADC used for impedance measurement, Section III presents measurement results on the ADC test chip and impedance measurement performance on a phantom model of skin, and Section IV brings up the conclusion.

II. Proposed ADC Architecture

Fig. 1 shows circuit schematic of the proposed bio-impedance measurement ADC. A phantom is used to model skin impedance. The phantom comprises parallel combination of a resistor and capacitor, denoted by R and C in Fig. 1(a) [7]. The electrode impedance is modeled by R_E in Fig. 1(a). As part of impedance measurement, a sinusoidal input with known amplitude and frequency, is injected through R_E. The ADC quantizes the fraction of the input current that flows into it. The ADC digital output is passed through a low-pass filter to remove out-of-band quantization noise, followed by digital matched filter, and the amplitude and phase of the phantom are extracted as shown in Fig. 1(b). Details of impedance measurement technique as well as ADC circuit design are discussed in the following sub-sections.

A. Mathematical Model

Fig. 2 shows mathematical model of the proposed impedance measurement circuit. A half-circuit model is shown

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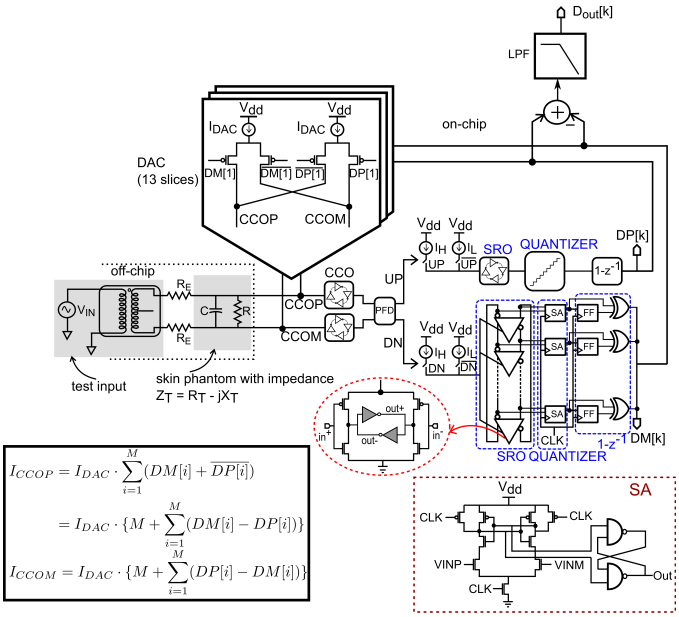
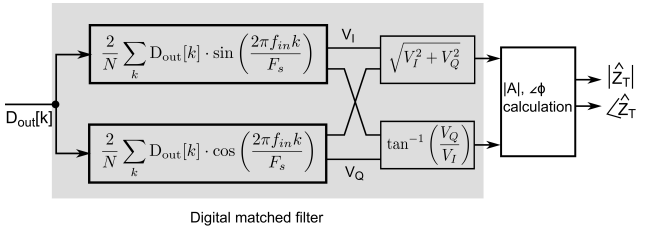


(a)



(b)

Fig. 1: (a) Proposed VCO-based read-out ADC schematic with an in-vitro phantom and (b) schematic for digital matched filter based amplitude and phase extraction

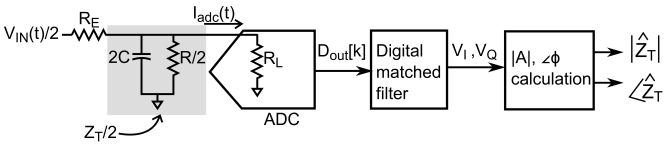


Fig. 2: Mathematical model for impedance measurement

in Fig. 2 for the sake of simplicity. The ADC single-ended input impedance is denoted by R_L. Assuming an input signal $V_{IN}(t) = 2A_m \cos(2\pi f_{in} t)$, the input current seen by the ADC is given by

$$I_{adc}(j\omega) = \frac{A_m \left(R_T - jX_T\right)}{R_T \left(R_L + R_E\right) + 2R_L R_E - jX_T \left(R_L + R_E\right)} \quad (1)$$

The ADC quantizes the analog input, and the low-pass filtered digital output is denoted by $D_{out}[k]$ in Fig. 2. The digital matched filter performs I/Q extraction [8]. The I and Q components of the matched filter output are given by

$$V_I = \frac{2}{N} \sum_{k=0}^{N-1} D_{out}[k] \cdot \sin\left(\frac{2\pi f_{in} k}{F_s}\right) \quad (2)$$

$$V_Q = \frac{2}{N} \sum_{k=0}^{N-1} D_{out}[k] \cdot \cos\left(\frac{2\pi f_{in} k}{F_s}\right) \quad (3)$$

where N is the number of taps in the digital matched filter, f_{in} is the frequency of the input sinusoid used for impedance measurement and F_s is the sampling frequency. The number of filter taps is selected such that $N = \lceil m \cdot (F_s/f_{in}) \rceil$ where $m \in \mathbb{Z}$. Assuming the ADC has a signal-transfer function of $STF(j\omega)$, the real ($\hat{R}_T$) and imaginary ($\hat{X}_T$) components of the impedance under measurement are extracted by solving the following equations:

$$\left|\frac{1}{STF(j\omega)}\right| \cdot \sqrt{V_I^2 + V_Q^2} = \sqrt{\frac{A_m^2 \cdot \left(\hat{R}_T^2 + \hat{X}_T^2\right)}{\{\hat{R}_T \left(R_L + R_E\right) + 2R_L R_E\}^2 + \{\hat{X}_T \left(R_L + R_E\right)\}^2}} \quad (4)$$

$$\tan^{-1}\left(\frac{V_Q}{V_I}\right) = \tan^{-1}\left(\frac{\hat{X}_T(R_L + R_E)}{\hat{R}_T R_L + \hat{R}_T R_E + 2R_L R_E}\right) + \angle STF(j\omega) - \tan^{-1}\left(\frac{\hat{X}_T}{\hat{R}_T}\right) \quad (5)$$

where $\hat{Z}_T = \hat{R}_T - j\hat{X}_T$ is the extracted impedance.

The phantom is a low-pass filter and attenuates input signals at high frequency. For this work, we have used a phantom with $R = 1k\Omega$ and $C = 10$nF [7] which corresponds to a 3-dB cut-off frequency of 16kHz. The simulated CCO input resistance R_L is 0.5kΩ. R_L can be reduced further by increasing CCO center frequency at the cost of power consumption. The proposed VCO-based ADC measures impedance over a frequency range of 1-300kHz. The phantom attenuates the input at 300kHz by 26dB. Hence, the matched filter has to be designed to recover the loss in SNR at the highest frequency of operation. As shown in [9], an N-tap matched filter improves SNR by $10\log_{10}(N/2)$dB if thermal noise is the dominant noise source, as is the case for our ADC. Fig. 3 shows variation in N and m versus input frequency. For 300kHz input and $F_s = 52$MHz, m is set to 12 corresponding to 2080-tap matched filter which improves SNR by approximately 30dB, while for 1kHz input, m is set to 1 corresponding to 52000-tap matched filter.

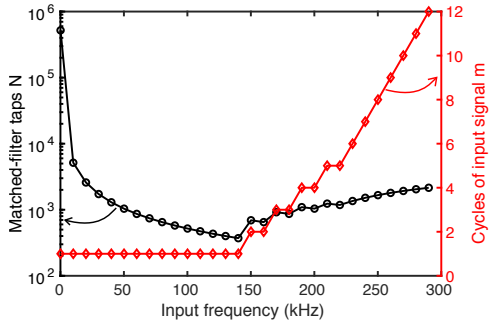


Fig. 3: Matched filter taps and number of input cycles vs frequency

B. ADC Circuit

The ADC circuit schematic is shown in Fig. 1(a). The ADC consists of two differential time-domain integrators in a

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single feedback loop. The first integrator is a current-controlled oscillator (CCO) which integrates the input current. Phase output of the differential CCOs are extracted using a tri-state phase/frequency detector (PFD) and fed to the second integrator through a 1-bit DAC. The 1-bit DAC produces a high current output, I_H, and a low current output, I_L, depending on whether the PFD outputs are '1' or '0'. The second integrator switches between two oscillation frequencies, f_H and f_L, corresponding to its input currents I_H and I_L respectively. Hence, the second integrator acts switched ring oscillator (SRO) and has very high linearity. At any given time instant, only one of the inverters in the SRO is undergoing transition. The change in SRO phase over a sampling period is obtained by finding how many inverters have undergone transition between two successive sampling instants. This is done by sampling outputs of all the inverters in the SRO with sense-amplifier (labeled as 'SA' Fig. 1(a)) and XOR-ing them with their sampled values from the previous cycle. A multi-element current steering non-return-to-zero (NRZ) DAC is used for creating negative feedback loop around the integrators. The CCOs and SROs are built from 13-stage pseudo-differential ring inverters. Fig. 1 shows a single inverter stage used in the CCOs and SROs. Weak cross-coupled inverters (shaded in gray) are used to ensure that phase difference between positive and negative outputs of each stage stays at $180°$.

In our earlier work [6], an NMOS current steering DAC is used which sinks current away from the front-end CCO and an additional PMOS current source is required to supply bias current to the CCO. By contrast, in this work, the combination of PMOS current source and NMOS DAC is replaced by a PMOS DAC as shown in Fig. 1. The current supplied by the PMOS DAC to the CCO, I_{CCOP} and I_{CCOM}, are shown in Fig. 1(a) which shows that the center frequency of the differential CCOs are set by $M \cdot I_{DAC}$. Since the DAC current is re-used to bias the CCO, power consumption of the ADC is reduced compared to our previous work [6]. The input referred noise is also reduced since there is no separate PMOS current source to bias the CCOs. As shown in [6], PMOS current source can be a significant contributor to ADC noise. Thus, the current-reuse DAC architecture reduces both ADC noise and power. Static element mismatch in the DAC is high-pass shaped by intrinsic data-weighted averaging due to the XOR gates which implement digital differentiation of SRO output as shown in Fig. 1(a) [6].

Since the proposed ADC is continuous-time with an NRZ DAC, it is susceptible to excess loop delay (ELD). While the effect of ELD on stability can be countered through proper selection of ADC parameters [6], ELD has a more significant effect on $\angle STF(j\omega)$. Based on SPICE simulations, the nominal ELD of our ADC is 400ps with worst case values ranging from 180ps to 800ps across process, voltage supply and temperature corners. The large variation in ELD around nominal value can increase the spread of $\angle STF(j\omega)$ at large sampling frequencies and degrade accuracy of impedance phase measurement. Thus, the ELD places a limit on the OSR. Fig. 4 shows simulation results for maximum spread in $\angle STF(j\omega)$ for different values of nominal normalized ELD, τ as a function of frequency, where τ is ELD normalized

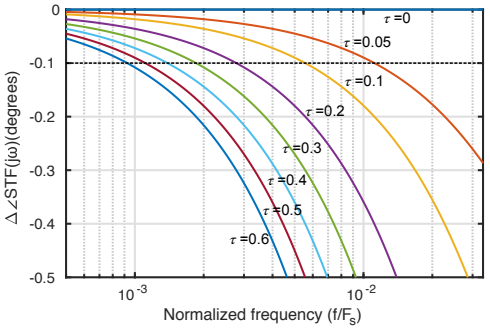

Fig. 4: Change in $\angle STF(j\omega)$ for different ELD

with respect to T_s. For each nominal τ, spread in $\angle STF(j\omega)$, denoted by $\Delta\angle STF(j\omega)$, is calculated by varying ELD from $\tau/2$ to 2τ. As expected, $\Delta\angle STF(j\omega)$ increases with both τ and frequency. For this design, $0.1°$ is set as the upper limit on $\Delta\angle STF(j\omega)$. From Fig. 4, it can be seen that if the nominal τ is 0.05, the maximum input frequency for impedance measurement is $F_s/90$, whereas if the nominal τ is 0.1, the maximum input frequency for impedance measurement is $F_s/180$. Hence, for an worst-case loop delay of 1ns and $\tau = 0.05$, the sampling frequency F_s is 50MHz and the maximum input frequency that can be used for impedance measurement is 550kHz, such that ELD does not affect calculation of impedance phase.

Fig. 5 shows the effect of variation in R_E on phantom impedance extraction. We introduce mismatch differentially in the two electrode impedances and sweep the standard deviation of mismatch, σ_{mis}, from 2% to 10%. For each σ_{mis} value, the simulation is repeated 100 times and effect of thermal noise is not considered for this simulation. Fig. 5 shows that error in phantom impedance extraction increases with σ_{mis}. In order to extract amplitude of phantom impedance with 98% accuracy, σ_{mis} should be $< 4\%$.

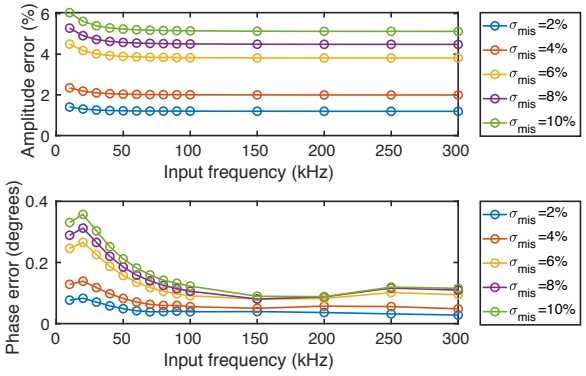

Fig. 5: Effect of mismatches in R_E on impedance extraction

C. ADC Design Optimization

In order to optimize ADC power and SNR, F_s is swept for signal bandwidth of 400kHz and Fig. 6(a) shows variation in ADC SNR and input referred noise versus F_s. M is set to 13 to ensure that the CCO and SRO have similar tuning gains as in [6] after supply voltage scaling. Since the ADC noise is dominated by thermal noise, reducing M reduces ADC power

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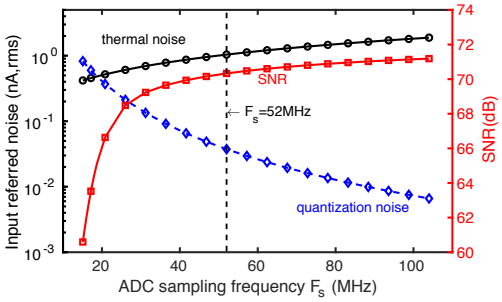
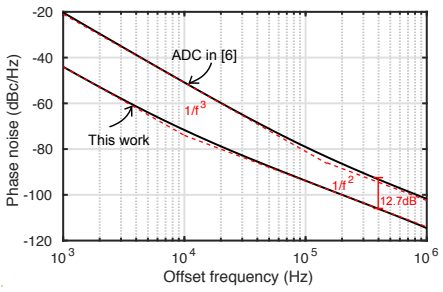
without degrading SNR. As shown in [6], the ADC open-loop gain is proportional to $k_{cco}k_{sro}I_{DAC}I_{sro}T_s^2$, where k_{cco} and k_{sro} are tuning gains of CCO and SRO respectively, and I_{sro} is given by $I_H - I_L$. If T_s is increased, I_{DAC} and I_{sro} have to be reduced proportionally, and vice-versa, to keep the ADC stable. Due to the current-reuse DAC architecture, change in I_{DAC} also changes CCO center frequency, and hence, its thermal noise. As shown in Fig. 6(a), as ADC sampling frequency F_s increases, both thermal noise and maximum input signal swing increases proportionally which results in relatively constant SNR. At very low F_s, ADC quantization noise is dominant which reduces SNR. For this design, F_s is set to 52MHz for which SNR is above 70dB and meets the lower limit set by ELD.



(a)



(b)

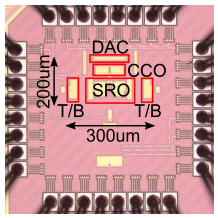
Fig. 6: (a) ADC SNR and noise vs F_s (b) Comparison of CCO+DAC noise with [6]

Fig. 6(b) compares the simulated phase noise from CCO+DAC combine with that of [6]. Removal of the PMOS current source lowered flicker noise significantly and the 1/f noise corner is reduced by $15\times$. Thermal noise PSD is reduced by $4.3\times$ or 12.7dB compared to [6] due to scaling of $M \cdot I_{DAC}$ and subsequent scaling of CCO center frequency, and removal of PMOS current source.

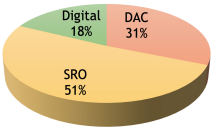
III. Measurement Results

A. ADC Measurement

A prototype ADC is implemented in 65nm CMOS process. Fig. 7 shows the die microphotograph of the test chip with key blocks highlighted, power breakdown as well ADC performance summary. The ADC has a core area of 0.06mm^2. The test chip runs at 52MHz and consumes 90μW power from 0.9V power supply. The ADC has a walden FoM of 43.3fJ/step which is 3.5x better than our previous work [6] and compares very favorably with state-of-the-art. The power reduction compared to [6] is due to supply scaling from 1.2V to 0.9V, use of current-reuse DAC and scaling of $M \cdot I_{DAC}$.



(a)



(b)

	This work	Prior work [6]
Process(nm)	65	65
Supply(V)	0.9	1.2
Power(mW)	0.09	1
F_s(MHz)	52	205
BW(MHz)	0.4	2.5
Noise (pA/$\sqrt{\text{Hz}}$)	1.7	7.5
SNDR(dB)	69.8[1]	64.2[1]
SNR(dB)	70.4[1]	65[1]
DR(dB)	71.7[1]	69[1]
FoM$_w$(fJ/step)	43.3	150.9

[1]measured with 50kHz input

Fig. 7: Die microphotograph and ADC performance summary

The test chip is measured in two phases - first the ADC is characterized by itself and then it is used to measure impedance of a phantom. Fig. 8 shows the measured SNR versus input frequency. The ADC has a mean SNR of 67dB with standard deviation of 1.94dB over the frequency range.

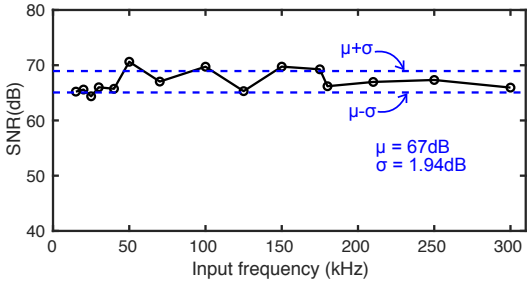


Fig. 8: Measured SNR of ADC versus frequency

B. Impedance Measurement

A phantom comprising a parallel combination of 1kΩ resistor and 10nF capacitor is used for impedance measurement. A 58mV (pk-pk) sinusoid input with frequency ranging from 1-300kHz is applied to the phantom. Fig. 9 shows the cole-cole plot showing the extracted values of real and imaginary parts of the impedance overlaid on top of ideal values. The measurement results show good agreement with ideal values. Fig. 10 shows the measured amplitude of the impedance versus frequency overlaid on top of ideal amplitude bode plot. The maximum error in extracted amplitude is 2.8%. Fig. 11 shows the measured phase of the impedance overlaid on top of ideal phase bode plot. The maximum error in extracted phase is 0.86°.

Table I compares this work with current state-of-the-art. The proposed ADC has 9x better power efficiency compared to state-of-the-art thanks to the highly digital, ring VCO-based $\Delta\Sigma$ architecture, lowest power, lowest input referred noise and the best accuracy for amplitude extraction. While bandwidth of the proposed ADC is lower than the ADCs in [1], [5], bandwidth can be increased by scaling up the sampling frequency while maintaining power efficiency.

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TABLE I: Comparison with state-of-the-art impedance measurement systems

	[1]	[10]	[4]	[3]	[2]	[5]	**This Work**
Process(nm)	180	180	180	65	180	350	**65**
Demodulation	digital	analog	analog	analog	digital	analog	**digital**
ADC type	SAR	SAR	SAR	SAR	SAR	–	**VCO**
Frequency ($f_2 - f_1$) (kHz)	0.1-10000	< 90	10-200	10-300	500-700	0.050-1000	**1-300**
Power (mW)	21.7	6.3	1.73	6.69	11.8	3.4	**0.09**
SNR (dB)	65	40	56.3	62	71	–	**67**[1]
Amplitude error(%)	7.5	–	8.5	10	1.8	5	**2.8**
Phase error (degrees)	0.15	–	–	–	2.8	–	**0.86**
FoM[2](pW/Hz)	1.22	4.44	13.97	18.32	4.09	–	**0.13**

[1]average SNR; [2]FoM = Power/$(10^{\text{SNR}/20} \times (f_2 - f_1))$

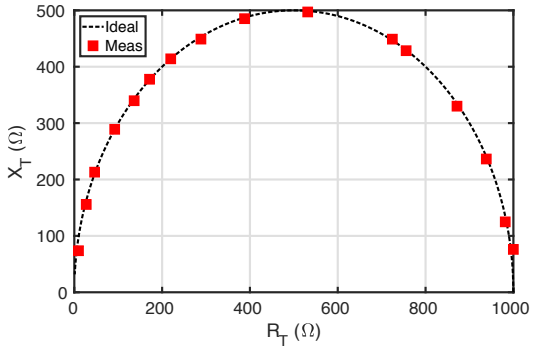

Fig. 9: Measured cole-cole plot over 1kHz-300kHz

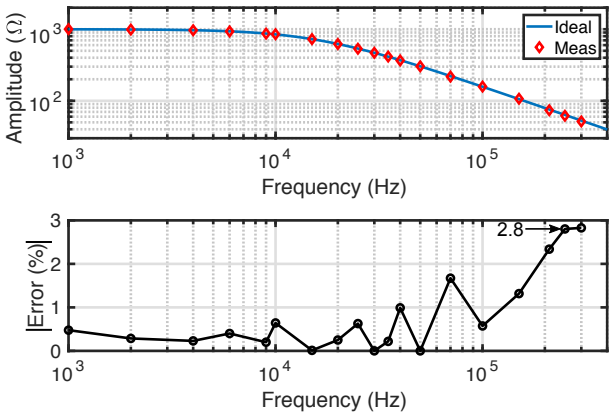

Fig. 10: Measured amplitude of impedance of the phantom

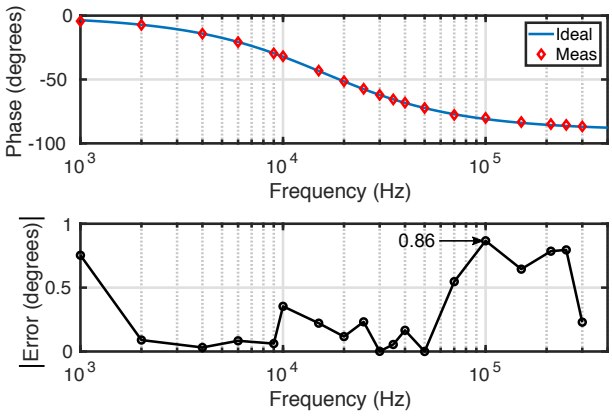

Fig. 11: Measured phase of impedance of the phantom

IV. Conclusion

A continuous-time, VCO-based $\Delta\Sigma$ ADC is presented in this work for impedance measurement. The proposed ADC addresses several limitations of existing SAR ADC based impedance measurement systems, such as kickback noise from sampling switch and power hungry ADC driver required to drive large sampling capacitor. While CT operation and highly digital nature of the proposed ADC results in state-of-the-art power efficiency along with high SNR, excess loop delay places a limit on the bandwidth of the ADC. To increase the frequency range of impedance measurement, ADC sampling frequency and, hence, power consumption has to be scaled up proportionally. The ADC power efficiency can be further improved by migrating to advanced CMOS nodes.

V. Acknowledgment

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