Fully Digital 1-1 MASH VCO-Based ADC Architecture

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***Abstract*—This paper proposes a novel architecture for purely voltage controlled oscillator (VCO) based 1-1 MASH second-order analog-to-digital converter (ADC). Each stage of the MASH uses an open loop inverter based ring VCO. The proposed ADC uses phase information from all inverters in the VCO in both the MASH stages to perform efficient multi-bit quantization. A novel VCO quantization error extraction circuit is proposed to easily extract quantization noise of the first VCO stage. A gain calibration for the second stage of the ADC has been analyzed. Behavioral simulations have been performed to validate the proposed architecture.**

I. Introduction

Ring voltage-controlled oscillator (VCO) based ADCs are a popular choice for recent analog-to-digital converters (ADCs) due to their highly digital nature. A ring VCO combines both integration and multi-bit quantization properties which makes it highly attractive for $\Delta\Sigma$ ADC design in advanced CMOS technologies. However, since quantization happens implicitly while reading out the phase of VCO, it is not trivial to design higher-order $\Delta\Sigma$ ADCs simply by cascading multiple ring VCOs. Early attempts to build high-order $\Delta\Sigma$ ADCs using VCOs embedded the ring VCO inside a loop with active integrators [1], [2]. More recent attempts have developed high-order $\Delta\Sigma$ VCO-ADCs by using passive integrators [3], modified DPLL based architecture [4]–[7] and multi-stage noise shaping (MASH) architectures [8], [9].

We present a MASH architecture in this work that implements second-order $\Delta\Sigma$ ADC by using two open-loop ring VCO stages. Existing MASH VCO ADCs use the phase information of all the inverter stages of ring VCO only in the last stage of the MASH and use phase information of only 1 inverter stage of ring VCO for all the preceding MASH stages. Using only phase information of 1 inverter stage of ring VCO allows extraction of VCO quantization error with digital logic similar to a phase detector, but is not an efficient way of designing a MASH since the phase information from all the inverter stages are not being used. As an example, for same SQNR, an N-stage ring VCO has to run N times faster if only 1 inverter phase is used for quantization than if phase information of all N inverter stages are used. Thus, using phase information of all inverter stages in ring VCO for quantization in both stages of 1-1 MASH, the proposed technique can achieve significant power savings and reduction in thermal noise since the VCO can run at a lower center frequency.

The rest of the paper is organized as follows: the proposed ADC design is presented in Section II, simulation results are presented in Section III and the conclusion is brought up in Section III.

II. Proposed Architecture

A. MASH VCO ADC architecture

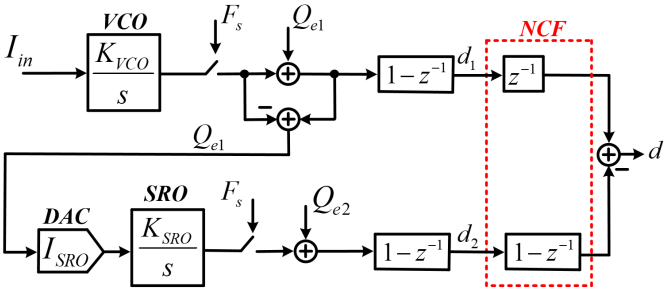

Fig. 1. Block diagram of 1-1 MASH ADC.

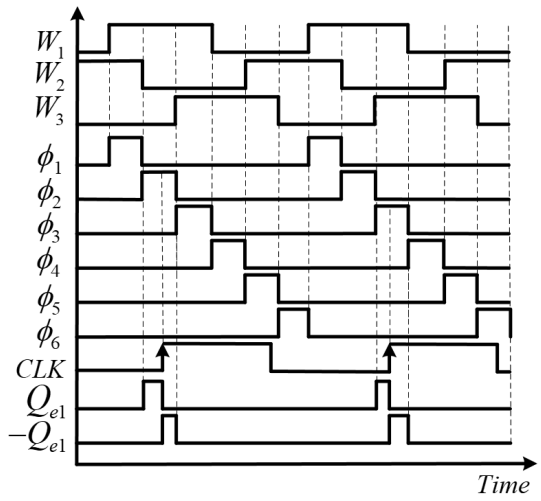

Fig. 2. Timing diagram for Q_{e1} extraction.

Fig. 1 shows the mathematical model of the proposed ADC. The analog input I_{in} is integrated by the first-stage VCO with a gain K_{VCO}. The quantization noise of the VCO, Q_{e1}, is extracted and fed to the second stage VCO, with gain K_{SRO}, in the form of timing pulses. Since, Q_{e1} is a pulse, the second

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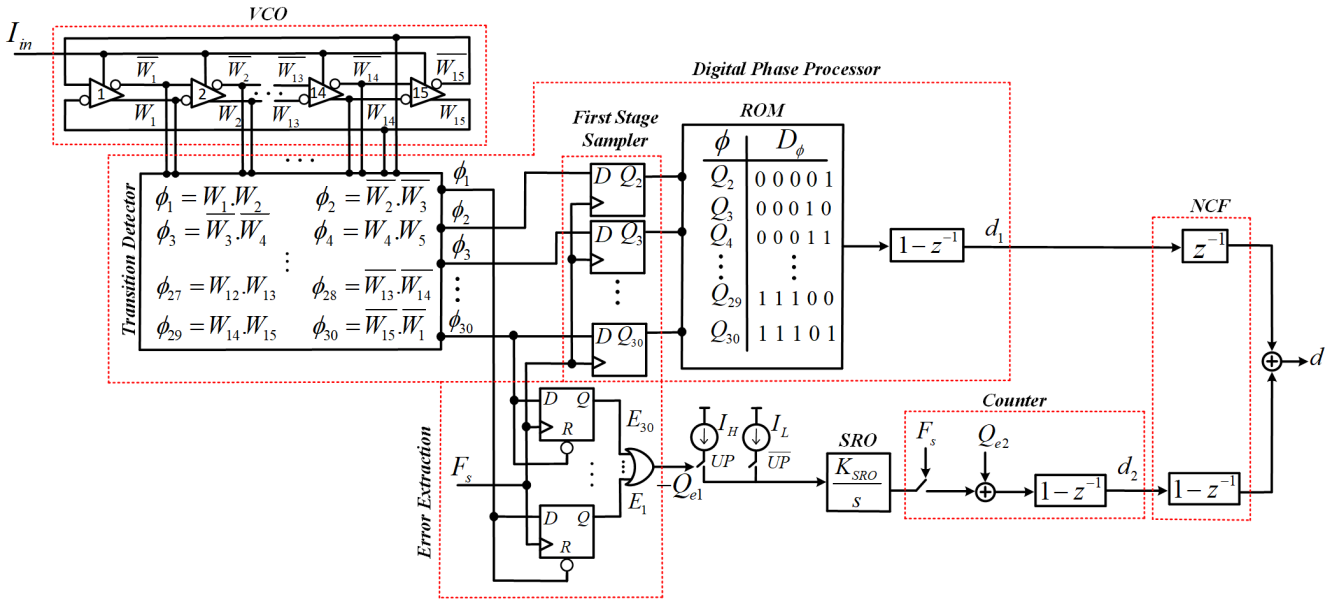


Fig. 3. Circuit schematic of the proposed ADC.

stage VCO oscillates at only two frequencies, depending on whether the instantaneous value of Q_{e1} is '0' or '1'. Hence, the stage VCO acts as a switched ring oscillator (SRO) and has very high linearity. The sampled outputs of the two VCOs are digitally differentiated and passed through a noise cancellation filter (NCF) for MASH as shown in Fig. 1. Mathematically, the ADC operation can be written as

$$\begin{aligned} d_1 &= G_1 z^{-1} I_{in} + (1 - z^{-1}) Q_{e1} \\ d_2 &= G_2 z^{-1} Q_{e1} + (1 - z^{-1}) Q_{e2} \\ d &= z^{-1} d_1 - (1 - z^{-1}) d_2 \\ &= z^{-2} G_1 I_{in} + z^{-1}(1 - z^{-1})(1 - G_2) Q_{e1} \\ &- (1 - z^{-1})^2 Q_{e2} \end{aligned} \quad (1)$$

where $G_1 = K_{VCO} T_s$, $G_2 = I_{SRO} K_{SRO} T_s$, I_{SRO} is the current gain of DAC at the input to second-stage SRO, Q_{e2} is quantization noise of SRO and T_s is the sampling period. It can be seen from (1) that $I_{SRO} K_{SRO} T_s$ has to be 1 to perfectly cancel out quantization noise of the first stage at the ADC output.

B. ADC Circuit

As mentioned before, we use phase information from all the inverter stages in the first-stage VCO. At any given time, only one of the inverters in the ring VCO is making a transition. By finding out which inverter is making a transition at the instant phase output of the VCO is sampled, we can quantize the VCO phase output. For an N stage ring VCO, there are $2N$ possible transitions, corresponding to rising and falling transitions of each of the N inverters. Thus, an N stage ring VCO acts as phase quantizer with $2N$ levels between 0 and 2π. The quantization error can be extracted by computing the difference in time from start of a transition to the sampling instant. We illustrate the quantization error extraction, we employ a 3-stage ring VCO as shown in Fig. 2. W_1, W_2, and W_3 are the outputs of the three inverters in the VCO and ϕ_1 to ϕ_6 are the 6 possible phase transition periods each with pulse widths of $\pi/3$. The first sampling edge (rising edge of CLK in Fig. 2), arrives somewhere during the second transition period or ϕ_2 and the quantized phase is $2\pi/3$. The phase difference between rising edges of ϕ_2 and CLK is the quantization error Q_{e1} as shown in Fig. 2. The second sampling edge arrives somewhere during ϕ_3 and Q_{e1} for the second sampling period can be extracted similarly by finding the difference between the rising edges. If instead of extracting the phase difference between the rising edges of transition period and sampling clock, we extract the phase difference between rising edge of sampling clock and falling edge of the transition period in which the clock arrives, we merely get $-Qe1$. For this work, we extract $-Q_{e1}$ as it is easier to do using simple digital logic as we will show next.

Fig. 3 shows the circuit schematic of the proposed MASH ADC. In order to find out which of the N inverters is making a transition during the sampling instant, we use a digital logic circuit labeled as 'Transition Detector' in Fig. 3. We define rising and falling transitions in the following way: a rising transition occurs when the positive input of an inverter cell is greater than switching threshold of the inverter and the positive output is less than switching threshold of the inverter. Similarly, a falling transition occurs when the positive input of an inverter cell is less than switching threshold of the inverter and the positive output is greater than switching threshold of the inverter. Since each transition state depends on both rising and falling edges of the inverters, non uniform quantization of phase is avoided which would otherwise lead to significant

distortion in the ADC output [10]. The $2N$ possible transitions can be detected by AND-ing the inputs and outputs of the inverters in the VCO stage as shown in Fig. 3. Output of the transition detector is sampled and processed to quantize the VCO phase output. The transition detector output is one-hot encoded and we use a digital logic, labeled as 'ROM' in Fig. 3 to convert the one-hot encoded values into binary number. The output of the ROM is quantized phase in binary format and is digitally differentiated to recover the signal input as digital word.

The digital logic for extracting quantization error of the first stage VCO is labeled as 'Error Extraction' in Fig. 3 and consists of only $2N$ D flip-flops (DFFs) corresponding to the $2N$ transition periods and an OR gate. During each sampling period, if the sampling clock edge arrives in the k-th transition period ($k \in [1, 2N]$), only the k-th DFF's output will go high from the time the sampling edge arrives to the end of the k-th transition period. All the other $2N-1$ DFFs will hold their outputs at '0' over the duration of the sampling period. Quantization error, $-Q_{e1}$, is encoded in the pulsewidth of the k-th DFF's output and is extracted by logical OR-ing of all DFF outputs. The timing pulse containing $-Q_{e1}$ is fed to the second-stage SRO through a DAC. The SRO input switches between two currents I_H and I_L depending on whether the instantaneous error pulse is at '1' or '0'. The sampled outputs of the SRO and first-stage VCO are combined through an NCF to obtain the overall ADC output as mentioned in Section II-A.

C. Interstage gain

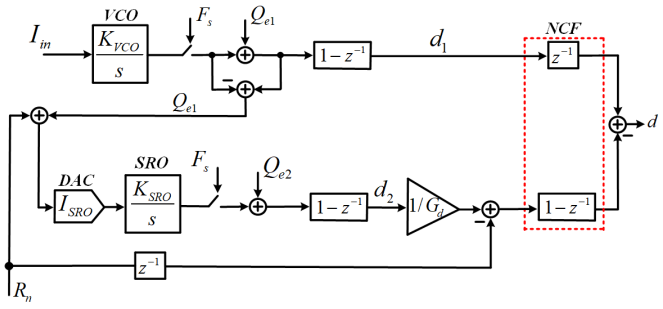


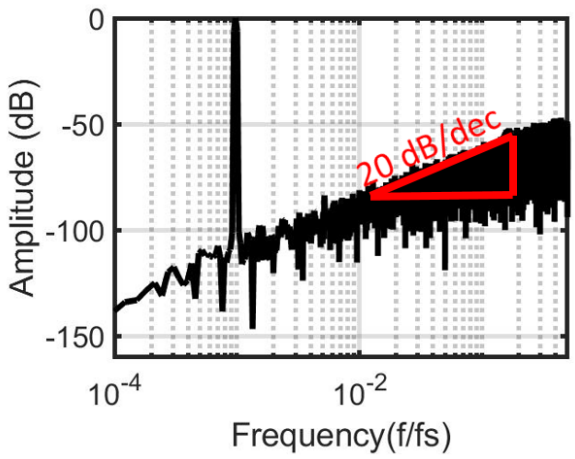
Fig. 4. Block diagram of the proposed MASH architecture for extracting the second stage gain.

As is well known, MASH ADCs suffer from sensitivity to interstage gain error. This can also be seen from (1) in which $I_{SRO}K_{SRO}T_s$ has to be set to '1' to ensure that Q_{e1} does not leak to the output. This is problematic since K_{SRO} varies with PVT. We propose a simple calibration technique similar to that in [11] to extract interstage gain. We inject a scaled 1-bit pseudo-random sequence, R_n, to the second-stage SRO through the DAC. The pseduo-random sequence can be generated using a linear feedback shift register (LFSR).

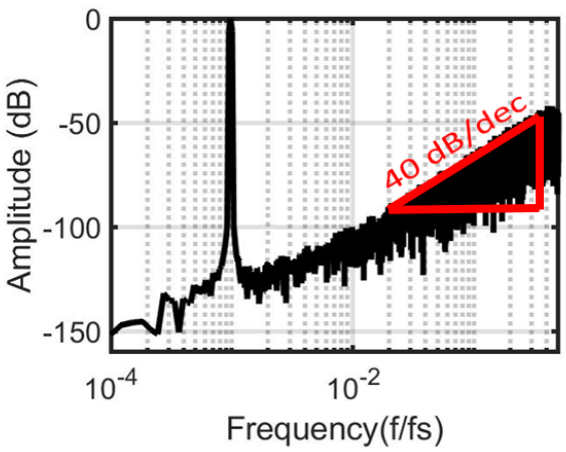
$$\begin{aligned} d_2 &= G_2 z^{-1}(Q_{e1} + R_n) + (1 - z^{-1})Q_{e2} \\ d &= z^{-2}G_1 I_{in} + z^{-1}(1 - z^{-1})(1 - G_2/G_d)Q_{e1} \\ &- (1 - z^{-1})^2 Q_{e2}/G_d \\ &+ R_n(1 - G_2/G_d)(z^{-1} - z^{-2}) \end{aligned} \quad (2)$$

From (2), we see that if we can set the digital gain G_d equal to analog interstage gain G_2, both Q_{e1} and R_n are canceled at the output. Since R_n is uncorrelated with the other terms in (2), correlating R_n with d_2 allows extraction of G_2. A simple way of injecting R_n into the second stage VCO is to dither one of the currents I_H and I_L depending on whether R_n is '0' or '1'. As an example, when R_n is '1', I_L can be replaced by a slightly different current source I_{L1}. Accurate current references are required to generate I_L and I_{L1} to ensure accuracy of the interstage gain calibration.

III. Simulation Results



(a)



(b)

Fig. 5. FFT of (a) first stage output (b) ADC output)

We performed behavioral level simulations to validate the proposed second-order ADC architecture. We used 15 inverter stages for both the first-stage VCO and second-stage SRO. Both the VCO and SRO gains are chosen to be $K_{VCO} = K_{SRO} = K_v = 5.7\mu$A/MHz. The VCO center frequency is set to 300MHz. A current input signal with amplitude of $10\mu A$ at a frequency of 4.5MHz is used. The ADC is sampled at 300MHz. It should be noted that there is no requirement for setting the VCO center frequencies same as ADC sampling frequency as long as the VCO and SRO gains are set to avoid overflow in both stages. Thermal noise has not been considered for this simulation. Fig. 5 shows the simulated spectrum of first-stage output and overall ADC. The FFT has been normalized with respect to input signal amplitude. At an OSR of 32, the first-stage VCO has an SQNR of 67dB and shows first-order noise shaping (see Fig. 5(a)). The overall ADC output shows second-order noise shaping (see Fig. 5(b)) and has an SQNR of 88.7dB for the same OSR. Fig. 6 shows the ADC SNDR versus input amplitude plot. The proposed MASH ADC has a high dynamic range of 92dB.

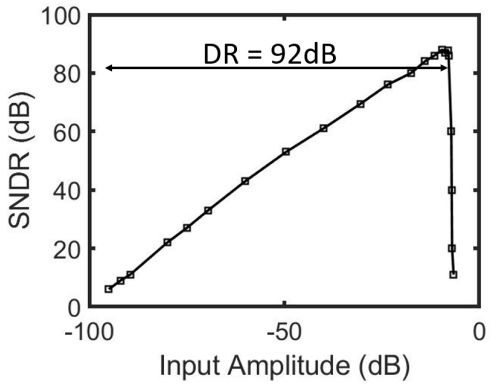


Fig. 6. ADC SNDR versus input amplitude.

Fig. 7 shows the ADC SNDR versus G_d/G_2. At $G_d/G_2 = 1$, quantization noise from first stage and R_n are perfectly canceled and the ADC has a high SNDR of 88.7dB. As G_d/G_2 ratio deviates from 1 on both sides, the ADC SNDR drops as expected.

IV. Conclusion

This paper has presented a novel, highly digital purely VCO-based second-order MASH ADC. The proposed architecture is based on 1-1 MASH architecture which uses phase information from all the inverter stages of ring VCOs in both stages of MASH. It is expected that the power consumption and the performance of the proposed ADC will improve with technology scaling due to its highly digital nature. The proposed architecture can also be extended to develop higher-order (> 2) VCO-based MASH ADC.

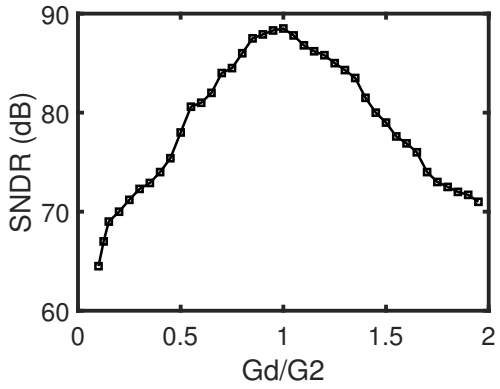


Fig. 7. SNDR changes versus DAC gain.

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