A Single Channel Bandpass SAR ADC with Digitally Assisted NTF Re-configuration

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***Abstract*—A single channel band-pass (BP) SAR ADC has been presented in this work. The proposed ADC uses a maximum likelihood estimator (MLE) to estimate the SAR residue similar to a two-stage architecture. The ADC output is obtained by subtracting a delayed version of the MLE estimate from the SAR output thus generating a noise transfer function (NTF) which can be re-configured by changing the delay. A 65nm BP ADC prototype achieves a 67.8dB SNDR when clocked at 2MS/s over a 79kHz bandwidth. The ADC consumes 13μW from a 1V supply leading to a 166dB schreier FoM.**

I. Introduction

Conventional band-pass (BP) analog-to-digital converters (ADCs) rely on high-gain amplifiers or LC resonators, that consume large area, [1]–[3] to implement complex noise transfer function (NTF). It is challenging to design high gain amplifiers with high energy efficiency at scaled CMOS technologies. An alternate method of implementing a BP ADC is to use a time-interleaved (TI) architecture [4] comprising multiple low-pass $\Delta\Sigma$ ADCs to implement a complex NTF. However, TI ADCs suffer from timing and gain mismatches and require power hungry clock buffers and/or calibration techniques to reduce mismatches [5]. Time-domain (TD) ADCs provide a viable alternative to conventional $\Delta\Sigma$ ADCs, by replacing high gain operational amplifier based integrator with a ring oscillator (RO) which performs both integration and quantization [6]. [4] presents a time-interleaved (TI) BP ADC that utilizes eight discrete-time (DT) RO based sub-ADC. However, despite the highly digital nature of RO, the benefits of using a RO based ADC are limited due to inherent RO non-linearity, and susceptibility to process, voltage, and temperature (PVT) variation. Moreover, the open loop RO used in [4] provides low dynamic range owing to RO non-linearity. In contrast to $\Delta\Sigma$ ADCs, successive approximation register (SAR) ADCs have scaled well into advanced CMOS nodes due to their highly digital nature. SAR ADCs have also been used to form highly digital low-pass $\Delta\Sigma$ ADCs by incorporating noise shaping (NS) [7], [8].

In this work, we use a fully digital technique to implement a BP ADC using a single SAR. After SAR finishes quantization, the comparator is fired multiple times prior to the next sampling phase and a maximum likelihood estimator (MLE) is used to estimate the SAR residue based on the comparator decisions. The estimated residue is delayed by N clock cycles and subtracted from SAR output to form the overall ADC output, thus converting nyquist SAR ADC into a BP ADC with N zeros in the NTF. The proposed ADC has a single channel thereby eliminating power hungry clock buffers, and timing mismatches. A prototype ADC is implemented in 65nm CMOS and achieves high energy efficiency thanks to the highly digital nature of SAR ADC. The rest of this paper is organized as follows: Section II presents the proposed architecture. Measurement results for the 65nm prototype and summary of performance are presented in Section III. Finally, the conclusion is brought up in Section IV.

II. Proposed Architecture

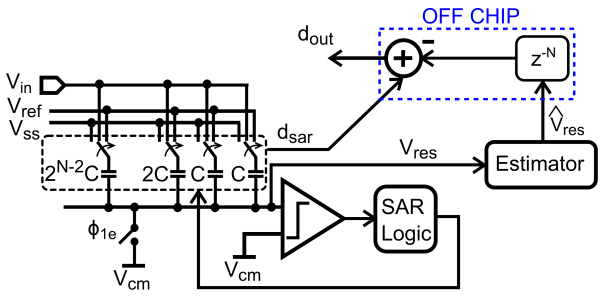


Fig. 1. Circuit diagram of proposed ADC

Fig. 1 illustrates the proposed SAR ADC architecture. For the sake of simplicity a single-ended model of the ADC is shown in Fig. 1 while the actual implementation of the ADC is fully differential. The analog input V_{in} is sampled onto bottom-plate of a 10-bit capacitive DAC array with 4.8fF unit capacitor.

Switching power of the proposed ADC is reduced by 86% in comparison to conventional switching techniques by employing the bi-directional switching (BDSS) technique of [9]. Fig. 2 shows the comparison of switching energy of our ADC with conventional SAR ADC and other well known SAR switching techniques, such as split capacitor technique [10] and monotonic switching [11]. From [12] the switching power of the 10-bit SAR is calculated to be 5.8μW.

Fig. 3 illustrates mathematical model of the proposed ADC architecture. The SAR output is given by

$$d_{sar} = V_{in} + n_{th} + q_1 \equiv V_{in} + V_{res} \quad (1)$$

where n_{th} is thermal noise of the comparator and DAC (assuming kT/C noise is much smaller than comparator noise),

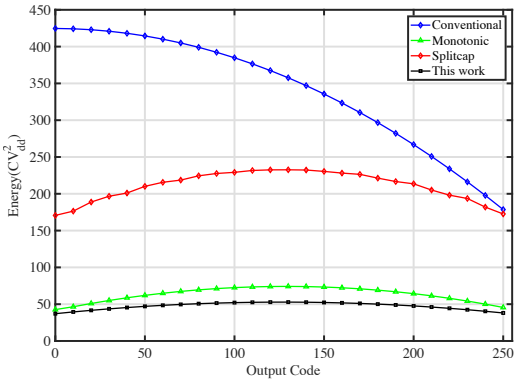
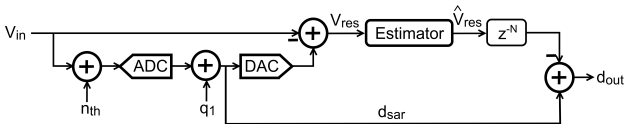


Fig. 2. Comparison of BDSS with other switching techniques



(a)

Fig. 3. Mathematical model of proposed ADC

q_1 is the SAR quantization noise, and V_{res} is residue after SAR quantization. The SAR residue voltage is available at the input nodes of the comparator after quantization. The comparator is fired M times after SAR quantization and the comparator outputs, $d[i]$, are used to derive an estimate of the residue $\hat{V}_{res}$. A maximum likelihood estimator [13] is employed in this work for estimation of SAR residue voltage. For MLE, the joint density of V_{res} and $d[i]$ is used as the likelihood function $L(\cdot)$ defined by

$$L(V_{res}|d[1],d[2],...,d[M]) = \frac{1}{\sqrt{(2\pi\sigma^2)^M}} \prod_{i=1}^{M} e^{-\frac{(d[i]-V_{res})^2}{2\sigma^2}} \quad (2)$$

where σ represents the standard deviation of V_{res}. The estimate of V_{res} is then obtained by setting derivative of the log-likelihood function to zero, and is mathematically expressed as

$$\hat{V}_{res} = -\frac{1}{2} + \sqrt{\frac{1}{M}\sum_{i=1}^{M} d[i]^2 + \frac{1}{4}} \quad (3)$$

An N-cycle delayed version of $\hat{V}_{res}$ is subtracted from the SAR output and the overall ADC output is given by

$$d_{out} = d_{sar} - z^{-N} \cdot \hat{V}_{res} \quad (4)$$

where z^{-N} refers to the N clock cycle delay of the quantized residue. From (3) and (4) it can be derived that

$$d_{out} = d_{sar} + \left(1 - z^{-N}\right) \cdot V_{res} + \epsilon \quad (5)$$

where ϵ is the estimation error of MLE. As long as ϵ is much smaller than V_{res}, i.e, the MLE estimator is highly accurate, the NTF of the ADC is determined by $\left(1 - z^{-N}\right)$ and has N zeros. Thus, the ADC becomes band-pass and has signal bands at $[0, f_{BW}]$, $[k \cdot f_s/N - f_{BW}/2, k \cdot f_s/N + f_{BW}/2]$ ($k \in [1, N/2-1]$) and $[f_s/2 - f_{BW}, f_s/2]$, where f_{BW} is the width of each signal band. As seen from (5), resolution of the proposed ADC is now purely limited by the estimation error ϵ arising from MLE, which can be reduced by increasing the number of times the comparator is fired (M) and is shown in Section III. Conventional NS SAR ADCs implement the NTF using active, and passive integrators [7], [8] in the analog domain. In contrast, the proposed ADC implements the NTF entirely in the digital domain and hence, the NTF can be re-configured easily by simply changing the number of delay taps, N, which is easy to do digitally. In (5), if $N = 1$, the proposed ADC has a low-pass NTF and if $N > 1$, the ADC transforms into a BP ADC. Currently, the subtraction of estimated residue from the SAR output is implemented off-chip to allow quick testing of different NTFs. Hence, one might argue that an on-chip implementation of the aforementioned digital processing would degrade ADC energy efficiency. From a hardware implementation perspective, the digital blocks required are a thermometer-to-binary converter (T/B) which sums the comparator outputs ($d[i]$), delay elements, and a subtractor to subtract the estimated residue from the SAR output. A T/B in 65nm consumes 0.2μW power, and a typical 12/13-bit carry select adder consumes less than 0.2μW power [14] when clocked at 2MS/s (f_s used in this work). Thus, the power consumed by the T/B, and subtractor would be 2% of the overall ADC power, and will not affect energy efficiency of the ADC if implemented on-chip.

A concern in two-stage architectures is inter-stage gain error. The MLE estimator effectively acts as second-stage in the proposed ADC. Parasitic capacitance, C_{par}, at the comparator input node scales the residue by a factor $\alpha = C_{DAC}/(C_{DAC} + C_{par})$, ($C_{DAC}$ is the DAC capacitance), which changes the inter-stage gain. Ideally, $\hat{V}_{res}$ should be scaled by $1/\alpha$ for perfect cancellation of inter-stage gain error. As the comparator is optimized for low-power consumption and has transistors with small aspect ratios, C_{par} is much smaller than C_{DAC} and does not significantly change the interstage gain, thus obviating the need for gain error calibration. While parasitic capacitance at the comparator input node can potentially introduce non-linearity, optimal sizing of the comparator in the proposed ADC results in a comparator input capacitance which is only 0.05% of C_{DAC}, and hence does not affect ADC linearity. Fig. 4 shows variation in SNR of the BP ADC ($N = 6$) as inter-stage gain error is varied from 0-10%. It can be seen from Fig. 4 that SNR changes by less than 0.5dB as inter-stage gain varies by 10%, indicating that interstage gain calibration is not required for this work.

III. Measurement Results

A 65nm prototype of the proposed ADC was fabricated in 65nm CMOS. Fig. 5 depicts the chip microphotograph, and ADC layout. The ADC occupies a core area of 350μm×350μm. The prototype consumes 13μW power from 1V supply when clocked at 2MHz, and the comparator is fired 18 additional times to estimate the residue after SAR

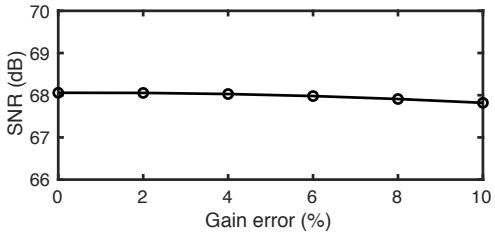


Fig. 4. Inter-stage gain error versus SNDR

quantization. A detailed power break down reveals that 7μW is consumed by the comparator and SAR logic while the DAC consume 6μW.

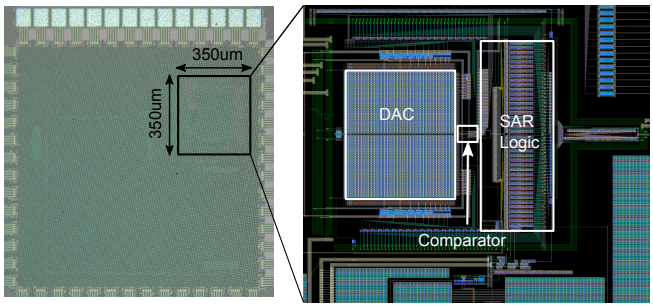
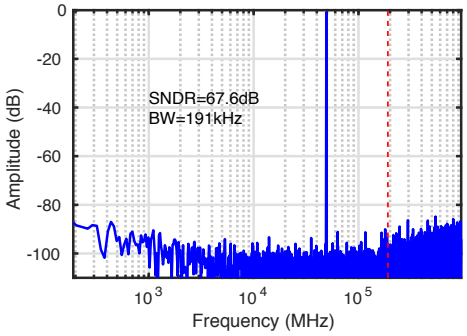


Fig. 5. Chip microphotograph and layout

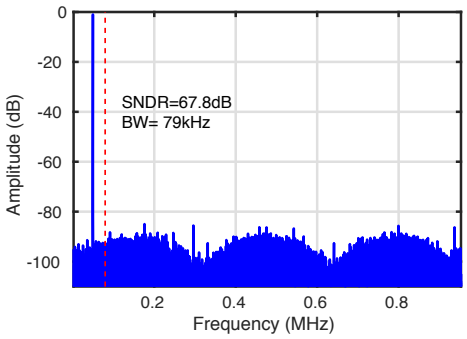
Fig. 6 shows the measured ADC spectrum. The ADC was tested with an input of 1.6V$_{pk-pk}$ amplitude and 50kHz frequency. Fig. 6(a) illustrates the ADC spectrum with N=1 for which the ADC exhibits a first-order low-pass NTF with an SNDR of 67.6dB at bandwidth of 191kHz. As shown in Fig. 6(b) the ADC exhibits a band-pass NTF when $N = 6$. SNDR of the BP ADC is 67.8dB at bandwidth of 79kHz. Thus, the prototype ADC achieves an effective number of bits (ENOB) of 11 with a 10-bit SAR. SFDR of the prototype ADC is $>$ 80dB for both low-pass and band-pass cases.

Fig. 7 illustrates the SNDR versus input amplitude for the proposed BP ADC with $N = 6$. For low signal amplitudes beyond the range of our signal generator, the SNDR plot has been extrapolated and shown with dotted line in the plot. The prototype BP ADC achieves a 71dB dynamic range.

A key design parameter that directly affects the energy efficiency of the prototype is number of times the comparator is fired to estimate the residue $\hat{V}_{res}$ after the SAR finishes quantization. Fig. 8 shows SNDR and energy efficiency (walden FoM) of the BP ADC as a function of M. As M increases, both SNDR and energy efficiency of the ADC improves for small values of M ($<$10). For values of $M > 10$, SNDR keeps improving gradually with increase in M but energy efficiency remains relatively constant. Eventually, if M becomes very large, exceeding the range shown in Fig. 8, SNDR will keep improving, but energy efficiency will start degrading. For this design, M is set to 18 corresponding to an SNDR of 67.8dB and walden FoM of 40fJ/step.



(a)



(b)

Fig. 6. Measured ADC spectrum with (a) N=1 and (b) N=6

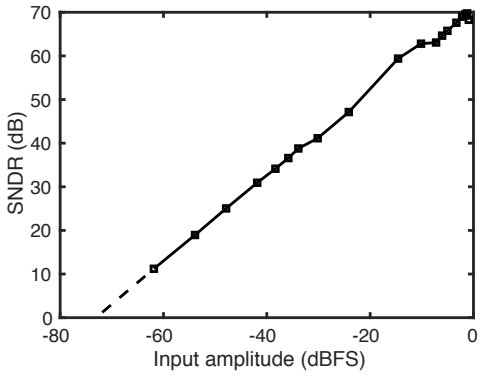


Fig. 7. SNR/SNDR versus input amplitude sweep

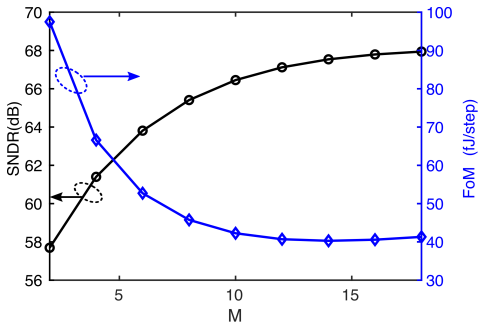


Fig. 8. M versus Energy efficiency/SNR

In order to validate robustness of the proposed ADC against PVT variations, the BP ADC measurements were taken at various power supply voltages, and temperatures. All the measurement results are for a $1.6V_{pk-pk}$ input signal at 50kHz frequency. Fig.9(a) depicts the variation of SNR/SNDR with variation in the supply voltage in the range of 0.9V - 1.05V. Fig.9(b) depicts the variation in SNR/SNDR of the BP ADC

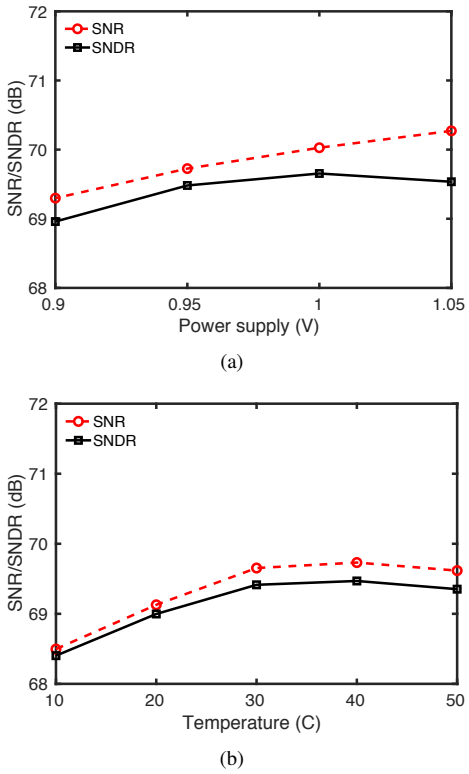


Fig. 9. ADC SNR and SNDR versus (a) supply voltage (b) temperature

with respect to change in temperature. For these measurements, the prototype along with the test-board was placed inside a thermally controlled chamber, and the temperature was varied from $10°$C to $50°$C. The temperature had to be limited to $60°$C to avoid damaging plastic components on the test-board. Measurement results from Fig. 9(a), and (b) demonstrate that PVT variations do not have significant effect on the performance of the ADC.

Table I summarizes the ADC performance. The prototype ADC achieves a walden FoM of 40fJ/step, and schreier FoM of 166dB, with M=18.

IV. Conclusion

This paper presents a novel single channel BP SAR architecture with re-configurable NTF that employs a low-power two-stage architecture, and shows promise by alleviating challenges plaguing conventional opamp and TI based BP ADC architectures, such as timing mismatches, poor energy efficiency, and lack of NTF re-configurability. The proposed architecture can be scaled easily, and optimized for high-speed, and high-resolution applications, giving rise to a new class of single channel BP ADC architectures.

TABLE I
Prototype BP ADC performance summary

Process	65 nm
Supply	1 V
Resolution	10 bits
Area	0.12 mm^2
Sampling Rate	2 MS/s
Bandwidth	79 kHz
Power	13 μW
SFDR	$>$ 80 dB
SNDR	67.8 dB
ENOB	11
walden FoM	40 fJ/c-step
schreier FoM	166 dB

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