A Highly Digital CCO-Based Asynchronous Analog-to-Time Converter

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***Abstract*—This paper presents an asynchronous current controlled oscillator (CCO) based analog-to-time converter (ATC). The proposed ATC uses a ring oscillator as phase-domain integrator and quantizer. A negative feedback loop using current steering digital-to-analog converter (DAC) relaxes linearity requirement of the CCO. The ATC output is a multi-phase pulse-width modulated (PWM) signal which can be used with continuous-time digital signal processing systems. The proposed ATC is simulated in 65nm CMOS process and has a 59.2dB SNDR with an input-referred noise of 42.6nV/$\sqrt{\text{Hz}}$ over 500kHz bandwidth while consuming 11μW from 0.5V power supply.**

I. Introduction

Time assisted data conversion techniques have garnered a lot of attention over the last decade [1]–[4]. CMOS technology scaling have resulted in lower voltage headrooms and reduced intrinsic transistor gain which has made conventional voltage based signal processing less energy efficient. In contrast, processing signals in time-domain (TD) has gained more traction since CMOS scaling has reduced transistor delay thus reducing quantization error in TD data converters. In addition, most recent TD data converters can achieve very high dynamic range at low supply voltages. The first step in TD data conversion involves transforming excursions of analog input from voltage to time. This is usually done by encoding the analog voltage input into a pulse-width modulated (PWM) output. Conventional $\Delta\Sigma$ modulators can generate PWM bitstream from analog voltage input but is not energy efficient [5]. Instead, an analog-to-time converter (ATC) [6] which uses mostly TD circuits can perform PWM encoding at much higher energy efficiencies. A multi-channel $\Delta\Sigma$ is presented in [7]. However, both [6], [7] uses op-amps as integrators which are challenging to design in scaled CMOS technologies. A recent work [5] uses a ring voltage-controlled oscillator (VCO) with capacitive digital-to-analog converter (DAC) that performs asynchronous analog-to-time conversion. Ring VCOs are highly digital and use of asynchronous ATC reduces aliasing of quantization tones into signal-band thus improving the overall SNDR. Recent advances in continuous-time (CT) digital signal processing [8] has also been an enabling factor for asynchronous ATC.

In this work, we propose an asynchronous ATC with a CCO based phase-domain integrator and a negative feedback loop comprising of a current steering digital-to-analog converter (DAC). The CT CCO phase output acts a multi-phase PWM signal which encodes the information of analog input in the pulsewidths of the output. The CCO is used as an integrator and hence, it has a large gain. The negative feedback loop relaxes the linearity requirement of the CCO. The proposed ATC is inherently robust against DAC unit element mismatch as the PWM encoding moves the mismatch error to even multiples of CCO center frequency. Simulated in 65nm CMOS process, the proposed ATC can handle input swing of 124mV$_{pk-pk}$ while having a low noise floor of 42.6nV/$\sqrt{\text{Hz}}$ over 500kHz bandwidth. The rest of this paper is organized as follows: the proposed ATC architecture is discussed in Section II. Simulation results on the proposed ATC architecture are presented in Section III, and the conclusion is brought up in Section IV.

II. Proposed Architecture

A. Circuit Design

The proposed asynchronous $\Delta\Sigma$ ATC architecture is shown in Fig. 1. The ATC employs a fully differential architecture. The analog voltage input is converted into current through two resistors each with resistance R. The analog current is fed differentially to two current controlled oscillators (CCOs). As shown in Fig. 1, each CCO has a pseudo-differential architecture and consists of 17 current-starved inverters. The CCOs act as inherent phase-domain integrator and quantizer. The phase difference between the two CCOs are extracted using XOR gates which act as linear subtractors in the phase domain. Since the CCOs have inherent quantization, their quantization noise appears at the output of the XOR gates. It should be pointed out here that since the XOR gates are continuous-time, the CCO quantization noise is not sampled. Rather, the CCO quantization noise consists of discrete tones at the XOR output. Since the output of XOR gates is a PWM signal [9], the output of 1 XOR gate can be written as $\{\frac{M}{2}\cos(\omega_{in}t) + \sum_{m=1}^{\infty} J_0\left(\frac{m\pi M}{2}\right)\sin\frac{m\pi}{2} \cdot \frac{2\cos(2m\omega_c t)}{m\pi} + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} J_n\left(\frac{m\pi M}{2}\right)\sin\frac{(m+n)\pi}{2} \cdot \frac{2\cos(2m\omega_c t + n\omega_{in}t)}{m\pi}\}$ where $M = k_{cco}I_{in}$, I_{in} being the current input to the CCO and k_{cco} is the tuning gain of the CCO, ω_{in} is the input frequency, ω_c is the CCO center frequency and $J_n(\cdot)$ denotes a Bessel function. Thus, the XOR gate output shows discrete tones centered around even multiples of CCO center frequency and spaced by the analog

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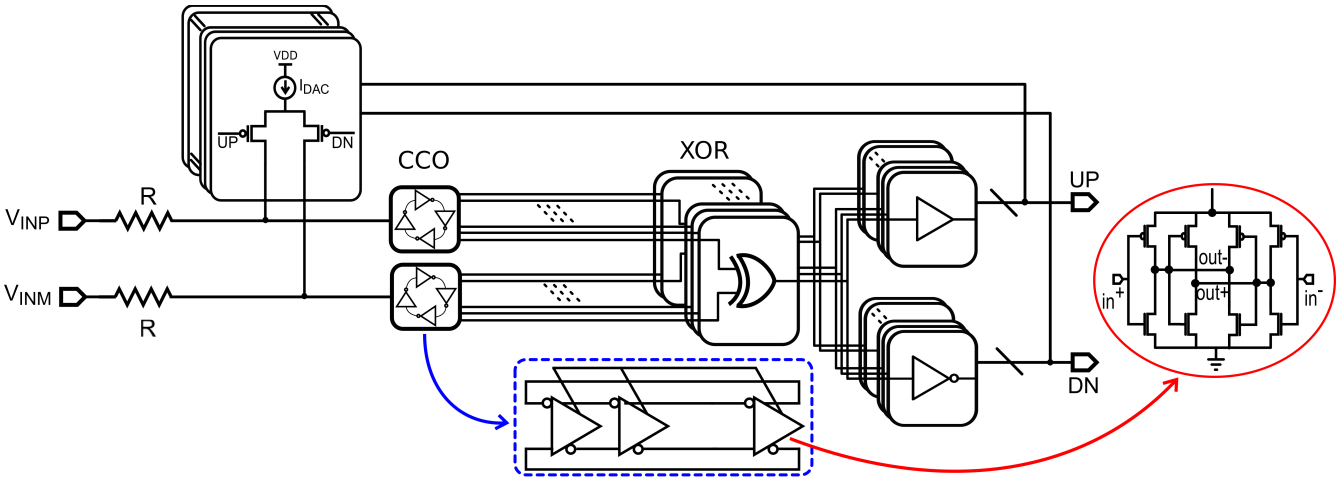

Fig. 1. Architecture of proposed asynchronous ATC

input frequency. These discrete tones represent quantization noise of the CCO. The feedback loop performs high-pass filtering on the CCO quantization tones before they are fedback using current steering DAC. The DAC combines 1-bit pulses from each XOR gate to form a multi-phase PWM signal.

The CCO is biased using common-mode current of the analog input and PMOS DAC and does not use a separate transconductor for biasing. This helps in reducing $1/f$ noise of the ATC and no chopping is performed for the proposed ATC. There is a trade-off between CCO center frequency, CCO noise and linearity and DAC errors. Static element mismatches in the multi-element DAC are upconverted to frequencies around even multiples of the CCO center frequency. Thus, setting the CCO center frequency high will result in better SNDR. In addition, setting CCO frequency high also reduces aliasing of CCO quantization noise to signal band and improves CCO linearity. However, the PWM input to the DAC also performs intrinsic clock-level averaging (CLA) [9]. Thus, the DAC elements transition at a rate proportional to CCO center frequency. A high CCO center frequency increases the number of DAC transitions which increases intersymbol interference error. In addition, a higher CCO center frequency also increases CCO thermal noise. We have set the CCO center frequency to 30MHz in this design to satisfy the competing requirements of noise, linearity and DAC errors. The ATC does not uses clocks to sample the CCO outputs which reduces power consumption. Low v_{th} transistors are used to allow the ATC to operate from a low supply voltage of 500mV.

B. CCO Behavioral Model

Fig. 2 shows behavioral model of the proposed ATC. $I_{in}(t)$ denotes the analog current input. PWM action of the CCO is modeled by comparing the integrated input with a triangular wave (PWM carrier) which represents the rate at which the differential CCO phase changes in the absence of an input. The triangular waves have different initial phase to account for the phase shift in the different inverter stages in the CCO. The PWM carrier tones do not produce any in-band distortions, rather, the distortion tones are placed at multiples of the CCO center frequency ($2\times f_c$, $4\times f_c$, ...) where $f_c = \omega_c/(2\pi)$. Fig. 3 compares the spectral response of the behavioral model

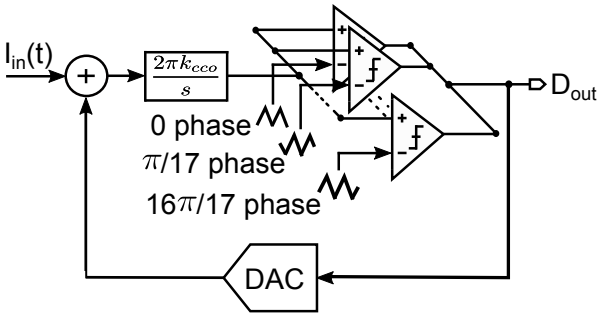

Fig. 2. ATC behavioral model

with Spectre simulation. An analog input at 140kHz frequency and with amplitude of $30\mu A_{pk-pk}$ is used for the simulation. The asynchronous ATC outputs are captured and interpolated to form the spectra. The simulation FFT response from the behavioral model matches closely with the Spectre simulation, thus validating the behavioral model of Fig. 2.

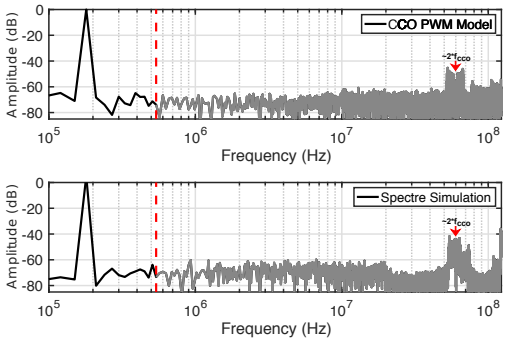

Fig. 3. Comparison of ATC behavioral model and Spectre simulation

III. Simulation Results

The proposed ATC is designed in 65nm CMOS process. A 17-stage pseudo-differential CCO, with k_{cco}=1.4MHz/μA is employed in the circuit. Spectre simulations were performed to validate the performance of the ATC. An input sinusoidal signal with amplitude of 124mV_{pk-pk} and frequency of 142.5kHz was used for the simulations. The ATC output is asynchronously sampled and interpolated at 500MHz sampling rate and the 2^{16} point FFT response is shown in Fig. 4. The ATC has a simulated SNDR of 59.2dB over a bandwidth of 500kHz and a power consumption of 11μW which results in a schreier FoM of 165.7dB and in-band noise floor of 42.6nV/$\sqrt{\text{Hz}}$.

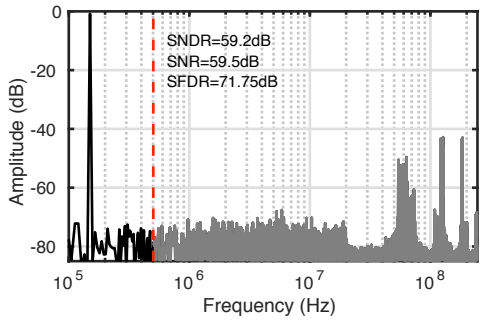

Fig. 4. 2^{16} point ATC spectrum with 124mVp-p input

Fig. 5 shows SNDR versus input amplitude for the proposed ATC. The ATC has a dynamic range of 66.3dB. A two tone test was performed on the ATC to analyze the effect of out-of-band interferers on the performance of the ATC. The input signals used for the test are f_1=142.5kHz, the fundamental tone, and f_2=532.5kHz. Fig. 6 depicts the ATC spectrum with a two tone input. The IM2 tone appears at $f_2 - f_1$=390kHz and is 68.4dB below the input signals, thus, indicating good linearity of the ATC.

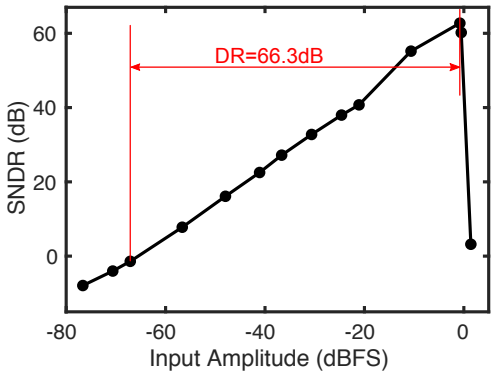

Fig. 5. ATC Dynamic Range

Transistor level simulations were performed to analyze the robustness of the ATC to device mismatches. Two major sources of mismatch that can affect performance of the ATC are (i) mismatch in CCO center frequencies (f_c), and (ii) static mismatch in DAC elements.

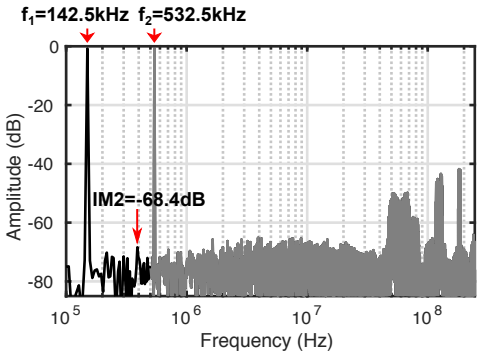

Fig. 6. ATC two tone test

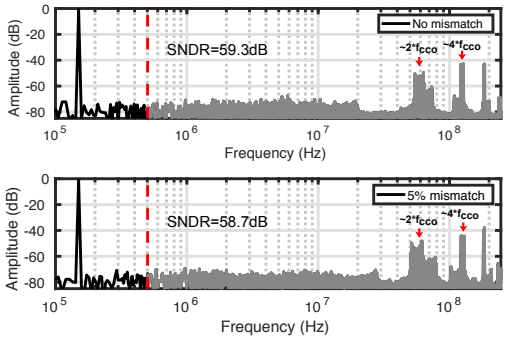

Fig. 7. ATC FFT with f_c mismatch

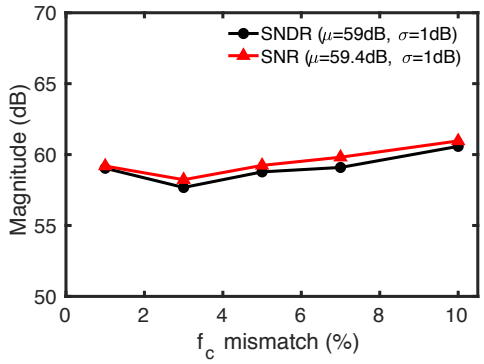

Fig. 8. SNDR/SNR versus f_c mismatch

Fig. 7 shows the FFT of the ATC for perfectly matched CCO center frequencies and effect of 5% mismatch. The simulation conditions are same as for that of Fig. 4 except for introduction of mismatch in CCO center frequencies. It can be seen that mismatch in CCO center frequencies does not affect the ATC SNDR and only increases distortion tones around even multiples of CCO center frequency. Fig. 8 shows the ATC SNR and SNDR as mismatch in CCO center frequencies is varied from 1-10%. ATC SNR/SNDR changes by less than 3dB as CCO center frequency mismatch is varied, indicating robustness to f_c mismatch. The ATC achieves a mean SNR of 59.4dB, and mean SNDR of 59dB over $1-10\%$ f_c mismatch.

Fig. 9 shows the FFT of the ATC with 5% mismatch in DAC unit elements compared to the case with no DAC mismatch. The simulation conditions are same as for that of Fig. 4 except for introduction of mismatch in DAC unit elements. Mismatch

errors in DAC are upconverted to frequencies around even multiples of CCO center frequency and does not affect ATC SNDR. Fig. 10 shows effect of DAC mismatch on ATC SNR/SNDR. ATC SNR/SNDR changes by less than 2dB as DAC mismatch is varied, thus indicating robustness against DAC mismatch. The ATC achieves a mean SNR of 60dB, and mean SNDR of 59.6dB over $1-10\%$ DAC static mismatch.

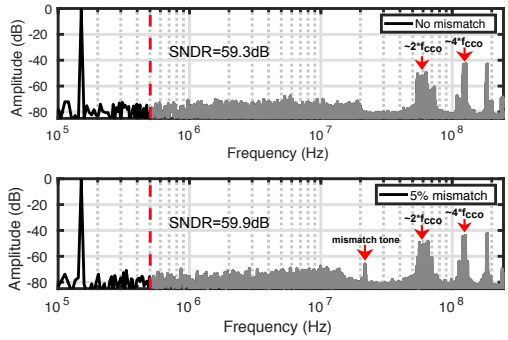

Fig. 9. ATC spectrum with DAC mismatch

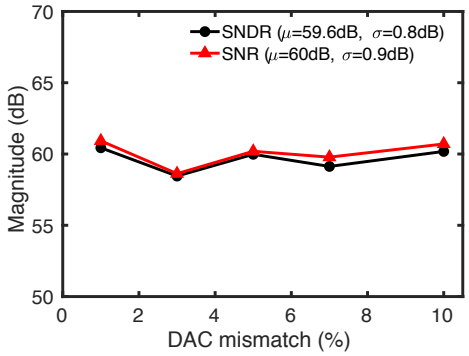

Fig. 10. SNDR/SNR versus DAC mismatch

Fig. 11 illustrates the variation of the ATC SNR/SNDR with respect to supply voltage. The ATC achieves a mean SNR of 59dB, and mean SNDR of 58.7dB with a standard deviation of 4dB with 10% mismatch in the supply voltage.

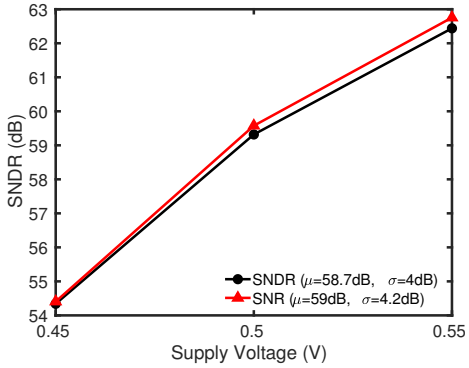

Fig. 11. SNDR/SNR versus supply voltage

Table I compares the proposed ATC with state-of-the-art ATCs of comparable bandwidths. The proposed ATC can handle the largest input swing and achieve very low noise floor of 42.6nV/$\sqrt{\text{Hz}}$ and schreier FoM of 165.7dB over a bandwidth of 500kHz. In contrast to existing ATCs which have either low noise floor or good energy efficiency, the proposed ATC achieves both low noise floor and high energy efficiency.

TABLE I
COMPARISON WITH STATE-OF-THE-ART ATCS

	[5]	[7]	[10]	**This work**
Process (nm)	65	180	40	**65**
Supply (V)	0.5	-	1.2	**0.5**
Power (μW)	1.2	11.5	17	**11**
BW (kHz)	11	10	5	**500**
SNR (dB)	51*	-	70*	**59.5**
SNDR (dB)	52*	49	61.8*	**59.2**
Input Range (mVpp)	4*	-	8*	**124**
Noise Floor (nV/$\sqrt{Hz}$)	36*	-	32*	**42.6**
FoM_S[1](dB)	151.6*	138	146.5*	**165.7**
FoM_W[2](fJ/c-step)	175*	2600	1643*	**14.43**

[1] $\text{FoM}_\text{S} = \text{SNDR} + 10\log_{10}(\text{BW}/\text{Power})$
[2] $\text{FoM}_\text{W} = \dfrac{\text{Power}}{2^{\text{ENOB}} \times 2 \times \text{BW}}$; *measurement results

IV. CONCLUSION

This paper presents a highly digital CCO-based asynchronous ATC which can operate from a very low supply voltage of 0.5V. The proposed ATC has a very low noise floor and high energy efficiency. The highly digital nature of the ATC implies that its performance will naturally improve with technology scaling.

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