A 2.4-GHz $\Delta\Sigma$ Fractional-N Synthesizer with Space-Time Averaging for Noise Reduction

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***Abstract*—This paper presents a highly digital technique that can significantly reduce the quantization noise of fractional-N phase-locked loops (PLLs) at all frequencies. This is achieved by using an array of dividers to realize *spatial averaging*. A fractional $\Delta\Sigma$ modulator (DSM) and a data-weighted averaging (DWA) module are used to generate the vector division ratio for the divider array. Based on this technique, a 2.4-GHz fractional-N frequency synthesizer is implemented in 40 nm CMOS process, in which *spatial averaging* is achieved with *only one divider* and *phase selection* to lower the power. Measurement results show that the phase noise at 1 MHz and 10 MHz frequency offsets are improved by 8 dB and 20 dB, respectively, compared to the conventional architecture. The output root-mean-square (rms) jitter is reduced from 10.4 ps to 3.1 ps, same as that at integer mode. The proposed synthesizer consumes only 4.9 mW in total, leading to a FoM of −223.3 dB.**

I. Introduction

Fractional-N phase-locked loops (PLLs) act as an essential role in modern communication systems, due to the merits such as finer frequency resolution, wider loop bandwidth, faster settling, etc. Fig. 1(a) shows the block diagram of a conventional fractional-N PLL. As the divider typically works with integer division ratios, an integer $\Delta\Sigma$ modulator (DSM) is used to realize the fractional frequency division by *time averaging*. The error between the integer instantaneous division ratio (DSM output) and the expected fractional division ratio (DSM input) results in ripples on the control voltage of the voltage-controlled oscillator (VCO) (see Fig. 1(b)), which introduces large quantization noise at the PLL output.

In recent two decades, there have been many works on quantization noise reduction without affecting the loop bandwidth. Among them, current digital-to-analog converters (DACs) and digital-to-time converters (DTCs) can be used to cancel quantization error [1]–[3]. However, they suffer from process, voltage and temperature (PVT) variations, and increase power and design complexity when calibration is applied. Phase interpolation (PI) techniques operate directly on quantization error without adding additional loops [4], [5], but they suffer from phase mismatch and cannot be directly applied to LC-VCOs. Although the finite-impulse-response (FIR) filtering technique is highly digital and immune to PVT variation [6], [7], it is only effective at high frequencies and does little help to low-frequency noise. Additionally, large number of taps are required for sufficient quantization noise suppression, which increases power, hardware cost and design complexity [7].

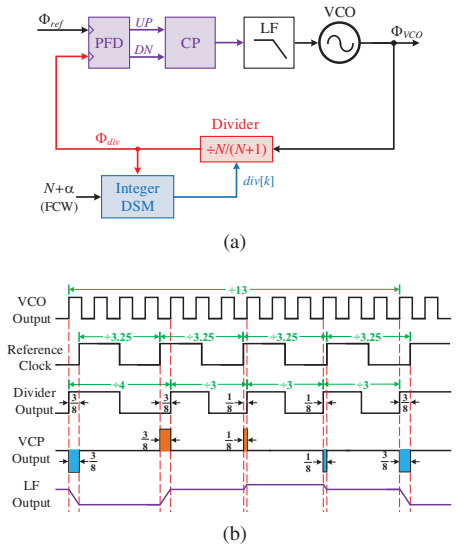

Fig. 1. (a) Block diagram and (b) time-domain waveform of a conventional fractional-N PLL.

To overcome these drawbacks, this paper presents a highly-digital, PVT-robust, calibration-free technique that can significantly reduce the quantization error over the entire frequency range. It is based on the new concept of *spatial averaging*, which is realized by using an array of dividers, phase/frequency detectors (PFDs), and charge pumps (CPs) [9]. If the divider array is considered as a whole, an instantaneous fractional division ratio is realized. In this way, the quantization step of the DSM can be a truly fractional number, rather than an integer in a conventional fractional-N PLL. While the original spatial averaging technique requires a large number of dividers, this paper proposes a method that requires only a single frequency divider, leading to substantially reduced power and hardware cost comparing to [9]. A prototype 2.4-GHz fractional-N frequency synthesizer is implemented in 40 nm CMOS process. Measurement results show that the in-band and out-of-band noise are reduce by 8 dB and 20 dB, respectively. The integrated jitter is reduced from 10.4 ps to 3.1 ps, which is the same as the case when the PLL runs in the integer-N mode. These results clearly prove the effectiveness of the proposed technique.

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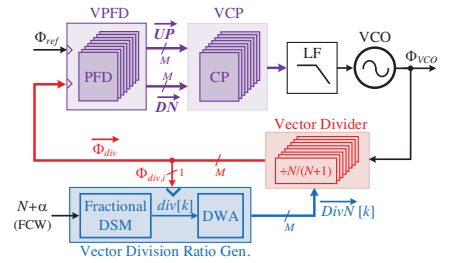
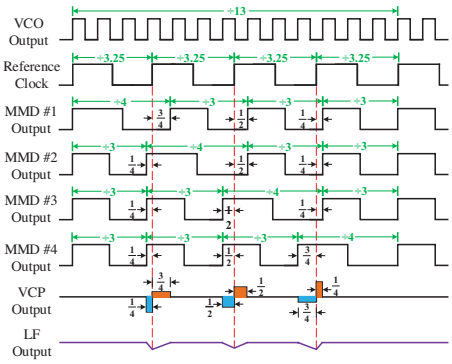


(a)



(b)

Fig. 2. (a) Block diagram and (b) time-domain waveform of the proposed fractional-N PLL with *space-time averaging*.

The rest of this paper is organized as follows. Section II introduces the basic principles of the *space-time averaging* technique. Section III presents the architecture of the proposed fractional-N frequency synthesizer. Section IV shows the measurement results, and Section V draws the conclusion.

II. Basic Principles of Space-Time Averaging

Fig. 2(a) displays the block diagram of the PLL with *space-time averaging* (STA) technique. Compared to the conventional architecture shown in Fig. 1(a), an obvious difference is that the new architecture employs an array-like vector divider, vector phase/frequency detector (VPFD) and vector charge pump (VCP), composed of M identical copies of corresponding elements, to achieve *spacial averaging*.

To better demonstrate the proposed STA technique, let us take an example shown in Fig. 2(b), where the frequency control word (FCW) is still $N + \alpha = 3.25$, same as that in Fig. 1(a). Unlike the conventional PLLs that has only one MMD dividing the VCO output by 4 or 3 for 25% and 75% of time, respectively, the STA technique has four MMDs working simultaneously, one of which divides the VCO output by 4 and the other three by 3 in every reference clock cycle. As a result, the *spatial averaging* of the division ratios of the four MMDs is 3.25, which does not change with time. In other words, the vector divider has an equivalent instantaneous fractional division ratio of 3.25, making its algebraic rising edge align to that of reference clock. As a result, the net charge injected to or removed by VCP is zero, greatly attenuating the ripples on the VCO control voltage when compared to that in Fig. 1(b). This reduces the quantization noise substantially and relaxes the linearity requirement of VCP, loop filter and VCO. In this way, it is possible to accurately generate any fractional division ratio in the form of $N + j/M$, where j is an integer and $j \in [0, M-1]$.

For an arbitrary division ratio $N+\alpha$ that cannot be written in the form of $N + j/M$, the *time averaging* of conventional fractional-N PLLs is brought back to generate a mixed fraction $div[k] = N + j/M$, whose long-time average equals to the FCW:

$$\lim_{K\to\infty} \frac{1}{K} \sum_{k=1}^{K} div[k] = N + \alpha \tag{1}$$

where $d_{inte}[k] = N$ and $d_{frac}[k] = j/M$ are the integer and fractional parts of $div[k]$, respectively. By selecting j MMDs to work with the division ratio of $(N+1)$ and $(M-j)$ MMDs to work with the division ratio of N, *space-time averaging* is achieved. In this way, the quantization noise is reduced by $20\log_{10} M$ (dB) over entire frequency range, *without* additional phase shifter or interpolater.

However, the key point is how to choose which j MMDs divide the VCO output by $(N+1)$ and which $(M-j)$ MMDs divide by N. To make the *spacial averaging* valid, each element of VPFD needs to work in the linear region with the difference of its two inputs within $[-2\pi, +2\pi]$, which means that the rising edges of all divider outputs must be closed to that of the reference clock. Mathematically speaking, we need to ensure:

$$\left| \sum_{k=1}^{K} (DivN_i[k] - DivN_j[k]) \right| \leq 2N \tag{2}$$

where K is a positive integer. To meet this requirement, every output of the vector divider needs to have same frequency as the reference clock. This is because phase is the integration of frequency, and thus, frequency difference must be zero when phase difference is bounded. It is nontrivial to satisfy (2). For example, we cannot choose some MMDs to always divide by $N+1$ while others always divide by N. Also, we cannot randomly select which MMD divides by $N+1$ or N, as this would also cause the phase difference to be unbounded. Besides, to ensure that the *spacial averaging* works, the other requirement to satisfy is:

$$\frac{1}{M} \sum_{i=1}^{M} DivN_i[k] = div[k] \tag{3}$$

where $DivN_i[k]$ is the division ratio of the i-th MMD.

Out of serendipity, (2) and (3) are same as the requirements for mismatch error shaping in multi-bit $\Delta\Sigma$ DACs. Thus, we can make use of the technique of data-weighted averaging (DWA), and place it between the fraction DSM and the vector divider to generate the vector division ratio $\overrightarrow{DivN[k]}$. The division ratio of the i-th MMD in the vector divider is:

$$DivN_i[k] = d_{inte}[k] + N_{DWA,i}[k] \tag{4}$$

In $\Delta\Sigma$ DACs, the barrel-shifted element selection pattern ensures each DAC element is turned on for the same time,

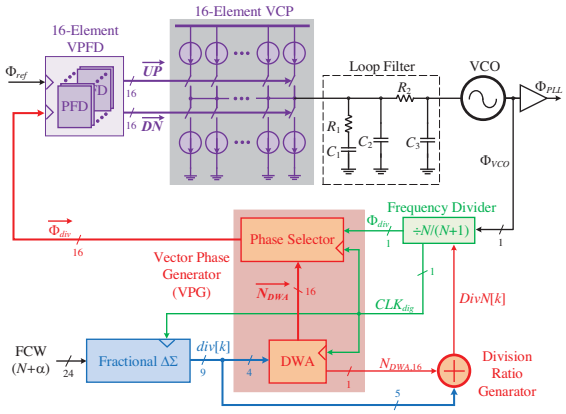


Fig. 3. Block diagram of the proposed fractional-N synthesizer.

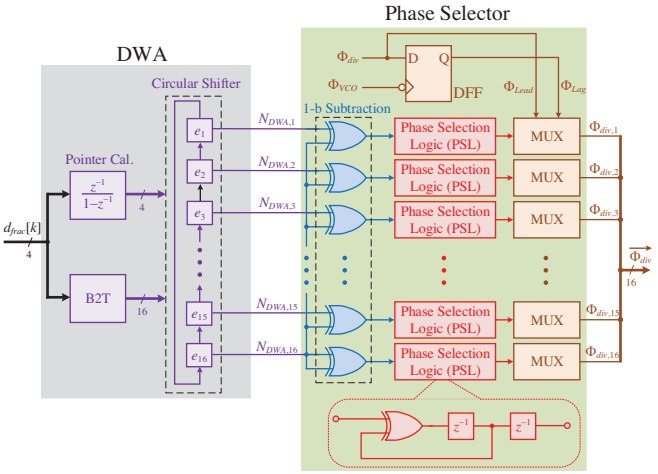


Fig. 4. Block diagram of the proposed vector phase generator (VPG).

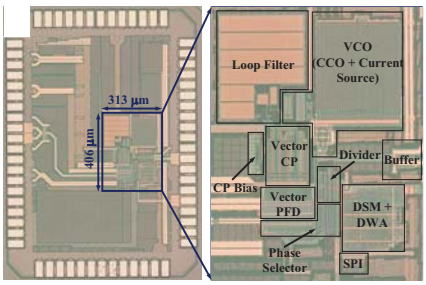


Fig. 5. Die photograph of the proposed synthesizer.

performing 1st-order shaping to the mismatch among DAC elements. Likewise, in the STA technique, the division ratio pattern is barrel-shifted to ensure each MMD has the same averaged division ratio. This makes the phase of one MMD always stay close to one another. Moreover, DWA here performs 1st-order mismatch shaping to the current mismatch in VCP.

III. Circuit Implementation

Fig. 3 depicts the block diagram of the proposed $\Delta\Sigma$ fractional-N frequency synthesizer, in which the STA technique is utilized. In the synthesizer, *time averaging* is achieved by a 3rd-order single-loop DSM with a quantization step of 1/16, which is implemented with four fractional bits in $div[k]$. Thus, both VPFD and VCP has 16 elements to realize the *spacial averaging*. By this means, the quantization noise can be theoretically reduced by 24 dB at all frequencies. The loop filter is a 3rd-order passive filter to support a 2.7-MHz closed-loop bandwidth.

As Fig. 2(a) shows, all MMDs in the vector divider divide the VCO output, consuming huge power when M is large. To reduce the total power of the proposed synthesizer, we use *only one frequency divider* together with *phase selection* to perform the function of the vector divider, generating the 16-element feedback signal $\overrightarrow{\Phi_{div}}$. As shown in Fig. 3, in the proposed synthesizer, the division ratio of the only divider is obtained by adding the 16th element of the DWA output, $N_{DWA,16}$, to the integer part of $div[k]$. The output of this divider is then processed by the phase selector, in which the selection pattern is generated from the DWA output vector $\overrightarrow{N_{DWA}}$. Fig. 4 displays the detail architecture of the vector phase generator (VPG) in Fig. 3. In this module, DWA employs the typical architecture and converts the 4-bit binary d_{frac} into a 16-element vector $\overrightarrow{N_{DWA}}$.

In PLLs, the frequency divider acts as a phase accumulator. Therefore, according to (4), the output phase of the i-th MMD in the vector divider is:

$$\Phi_{div,i}[K] = 2\pi \sum_{k=1}^{K-1} d_{inte}[k] + 2\pi \sum_{k=1}^{K-1} N_{DWA,i}[k] \qquad (5)$$

Based on the concept of DWA, the 16th element of its output is the last one to output 1, which means $N_{DWA,i} \geq N_{DWA,16}$ always holds. Hence, we choose the output phase of the 16th MMD as the reference for phase selection to match the initial condition of the vector divider, and (5) can be written as:

$$\Phi_{div,i}[K] = \Phi_{div,16}[K] + 2\pi \sum_{k=1}^{K-1} (N_{DWA,i}[k] - N_{DWA,16}[k]) \qquad (6)$$

As the 1st-order shaped mismatch noise is finally converted into white noise at the synthesizer output, the second part of (6) is either 0 or 2π. As a result, the output phase of the i-th MMD in the vector divider can be obtained by selecting between the output phase of the 16th MMD (Φ_{Lead}) and one VCO cycle delay of that (Φ_{Lag}). As shown in Fig. 4, these two phases is generated via a D-type flip-flop (DFF) sampled by the VCO output, the 1-bit subtraction in the brackets is achieved by an XOR gate, and the accumulation is realized by the phase selection logic (PSL) that generates the phase selection pattern. If the PSL output is 0, $\Phi_{div,i} = \Phi_{Lead}$; otherwise, $\Phi_{div,i} = \Phi_{Lag}$. In this way, the vector feedback signal $\overrightarrow{\Phi_{div}}$ is obtained.

IV. Measurement Results

The prototype frequency synthesizer is fabricated in 40 nm CMOS process. It occupies an active area of 0.1 mm^2 as Fig.

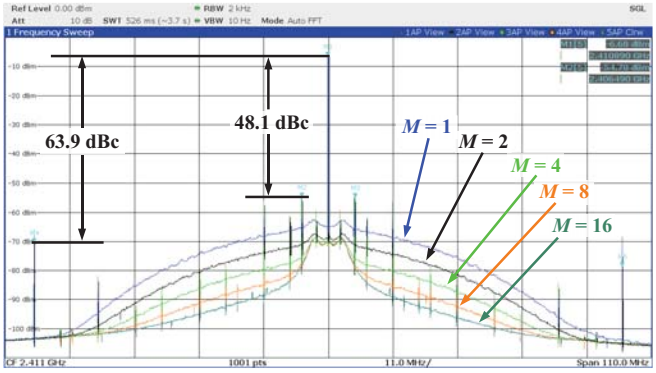


Fig. 6. Measured output spectra in the fractional-N mode with different M.

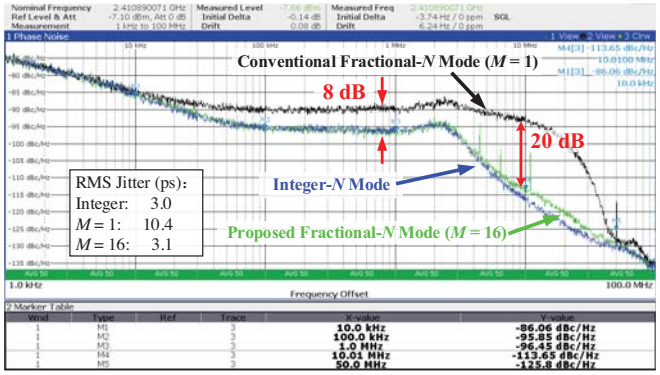


Fig. 7. Measured phase noise in different modes.

5 shows. The operation frequency range covers from 1.67 to 3.12 GHz with a 50-MHz reference clock. The synthesizer consumes 4.9 mW from 1.1-V power supply in total (VCO: 3.3 mW, VCP: 0.5 mW, phase selector: 0.4 mW, VPFD: 0.3 mW, digital: 0.3 mW, divider: 0.1 mW).

Fig. 6 shows the measured output frequency spectra in the fractional-N mode with $M = 1, 2, 4, 8, 16$, respectively, where $M = 1$ represents the conventional fractional-N architecture. As shown, the proposed synthesizer improves the output phase noise at all frequencies with the increase of M. As $M > 4$, the in-band noise improvement becomes less significant due to the dominance of other noise sources. The out-of-band noise is reduced gradually with the increase of M. As shown in Fig. 6, the out-of-band noise is reduced by around 6 dB when M doubles. When $M > 8$, this improvement is less than 6 dB due to the quantization noise is no longer the dominant source of the total output phase noise. Fig. 6 also shows the measured reference and fractional spurs of the proposed synthesizer, which are 63.9 dBc and 48.1 dBc, respectively.

Fig. 7 compares the output phase noise of the proposed synthesizer with the conventional architecture. As shown, the proposed synthesizer has 8-dB and 20-dB improvements at 1 MHz and 10 MHz frequency offsets, respectively. Fig. 7 also shows that the proposed synthesizer reduces the integrated root mean square (rms) jitter from 10.4 ps to 3.1 ps at $M = 16$, same as noise level of the integer mode (3.0 ps). This means

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Specifications	[6] ISSCC '08	[5] ISSCC '11	[8] ISSCC '13	[2] ISSCC '15	[7] ISSCC '17	**This work**
Quan. Noise Reduction Tech.	8-tap FIR	PI with 8-tap FIR	Segmented PI	Switched Cap. LF	35-tap FIR	**16-channel SPA**
Architecture	Type-II	Type-II	Type-II	Type-II	Type-I	**Type-II**
Technique (nm)	180	130	40	40	45	**40**
Ref. Freq. (MHz)	27	32	26	26	22.6	**50**
Output Freq. (GHz)	1	1	1.87	2	2.42	**2.41**
Bandwidth (MHz)	1	3.2	2	1.51	5.5	**2.7**
PN @ 1MHz (dBc/Hz)	N/A	−103	−98	−98	−104	**−96**
PN @ 10MHz (dBc/Hz)	N/A	−114	−115	−115	−121.4	**−114**
Ref. Spur (dBc)	N/A	−66	−67	−87	−60	**−63.9**
Frac. Spur (dBc)	< −40	N/A	−50	−70	−41	**−48.1**
Freq. Resolution (Hz)	26	N/A	N/A	100	340	**3**
Power (mW)	6.1	16.8	10	9.1	10	**4.9**
Active Area (mm^2)	0.5	0.31	0.055	0.046	0.096	**0.1**
RMS Jitter (ps) Integ. Range (MHz)	17.2 (1–100)	N/A	3.4 (0.004–40)	2.4 (0.001–40)	1.5 (0.01–50)	**3.1 (0.01–50)**
FoM[1](dB)	−207.4	N/A	−219.4	−222.8	−226.5	**−223.3**

[1] $\text{FoM} = 10\log_{10}\left[\left(\frac{\text{Jitter}_{\text{rms}}}{1\text{ sec}}\right)^2\left(\frac{\text{Power}}{1\text{ mW}}\right)\right]$

that the quantization noise is no longer dominant in the overall output noise under this circumstance. Table I summaries the performance and compares with other works with quantization noise reduction techniques.

V. CONCLUSION

A highly digital technique for fractional-N PLLs to reduce quantization reduction over entire frequency range is proposed in this paper. Based on this technique, a 2.4-GHz $\Delta\Sigma$ fractional-N frequency synthesizer is implemented with a single divider. The measurement results shows the proposed fractional-N synthesizer realizes same noise level as the integer mode, but consumes very low power.

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