

# Ultra-Low Power Analog Multiplier Based on Translinear Principle

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**Abstract**—In this paper, a wide dynamic range, current-mode four-quadrant analog multiplier circuit is proposed that utilizes MOS translinear principle. The proposed multiplier is designed in 65nm technology using CMOS transistors operating in weak inversion. A thorough analysis of the proposed design is performed using Spectre and monte-carlo simulations. The multiplier consumes a low power of  $0.48\mu\text{W}$  and supports an input range of  $\pm 200\text{nA}$  while operating from  $0.8\text{V}$  supply and exhibits an average total harmonic distortion (THD)  $1.12\%$ . Post layout simulation results show a high figure-of-merit (FoM) of 1302 verifying superiority of our design against other state-of-the-art multiplier circuits.

## I. INTRODUCTION

While analog multipliers have been around for a long time, there is a recent increase in research attention on low-power, low-voltage analog current-mode circuits. This research attention has been primarily driven by the need to have low power and small area analog computing systems that can be used for machine learning or hardware security applications. Four-quadrant multiplication is a core operation that is widely used in analog signal processing applications. Four quadrant multipliers are used as modulators, frequency doublers, adaptive filters [1], phase detection [2], mixers [3], neural networks [4], sensor applications [5], gain controlling [6], and fuzzy systems [7], to name a few.

The first four-quadrant analog multiplier is the widely used Gilbert cell [8] which was implemented using bipolar transistors. Since then, a noticeable number of works have been reported in CMOS technology. The increasing demand for low voltage/low-power integrated circuits has encouraged the development of CMOS current-mode architectures. As in their voltage-mode counterparts, the operating principle of most current-mode structures uses MOS drain current either in strong inversion [9] or in weak inversion region [10], [11]. Current-mode four-quadrant analog multiplier circuits have been designed from different principles such as stacked [12] and folded MOS translinear loops (MTL) [11]. However, these techniques require either additional supply voltages, which increase power, or are sensitive to body effect.

This work presents a current-mode four-quadrant multiplier using MOS transistors operating in weak inversion. The proposed multiplier is built by using 3 squarer cells utilizing translinear loops in a cascode up-down structure which, as will be shown later, improves linearity compared to the folded translinear loop architecture of [11]. The squarer cell is basically inspired by the one which was designed in 180nm CMOS

technology process by this author for RMS-to-DC conversion application [13], and it has been developed and modified to be used as the main part of the multiplier circuit designed in 65nm technology process. The proposed multiplier provides a wide dynamic range and consumes less power than state-of-the-art designs. The loop architecture reduces the effect of mismatch leading to reduced errors in the output. The hierarchical design methodology, based on squarer circuit design, can be easily extended to circuits for other mathematical operations, such as square-root, division, geometric mean and absolute value.

The rest of this work is organized as follows: Section II presents the architecture of the proposed multiplier and provides analysis of the squarer and multiplier circuits, simulation results are presented in Section III. The conclusion is brought up in Section IV.

## II. PROPOSED ARCHITECTURE

### A. Multiplier Architecture

The proposed multiplier block diagram is shown in Fig. 1. As can be seen from Fig. 1, multiplication operation is done by three squarer blocks.  $I_{out}$  is the output current of multiplier.  $I_B$  is DC bias current.  $I_{in1}$ ,  $I_{in2}$ , and  $I_{in1} + I_{in2}$  are the input currents of squarer1, squarer2 and squarer3 respectively. Basically, the first two squarer cells have two outputs that  $I_{out1_1} = I_{in1}$  and  $I_{out2_1} = \frac{I_{in1}^2}{4I_B}$  are the outputs of squarer cell 1 and  $I_{out1_2} = I_{in2}$  and  $I_{out2_2} = \frac{I_{in2}^2}{4I_B}$  are the outputs of the second squarer cell.  $I_{out1_1}$  and  $I_{out1_2}$  are added to form the input current of the third squarer cell. Output current of the multiplier can be shown to be

$$\frac{I_{in1}^2}{4I_B} + \frac{I_{in2}^2}{4I_B} + I_{out} = \frac{(I_{in1} + I_{in2})^2}{4I_B} \implies I_{out} = \frac{I_{in1}I_{in2}}{2I_B} \quad (1)$$

### B. Squarer Circuit

In weak inversion region, MOS current can be written as follows [14]:

$$I_D = \frac{W}{L} I_{D0} \exp^{\frac{V_{GS}}{\eta V_T}} \quad (2)$$

where  $I_{D0} = I_s \exp^{\frac{V_{th}}{V_{GS}}}$ ,  $I_s = 2\eta\mu C_{ox} V_T^2$  which is a characteristic current that defines the current that leaks through the transistor,  $V_T = \frac{kT}{q}$  and  $\eta > 1$  (around  $1 \sim 1.5$ ) and defines the effect that the gate voltage has on the drain current. Except for  $\eta$ , (2) is similar to the exponential  $I_C/V_{BE}$  relationship in a bipolar transistor. With typical values of  $\eta$  and

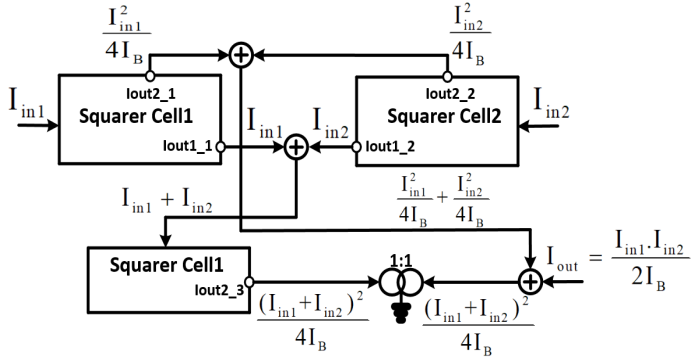


Fig. 1. Complete circuit of the multiplier.

at room temperature,  $I_D$  reduces by approximately a factor of 10 for every 80mV drop in  $V_{GS}$ . Fig. 2 shows the squarer cell used in the proposed multiplier. In this section, for better

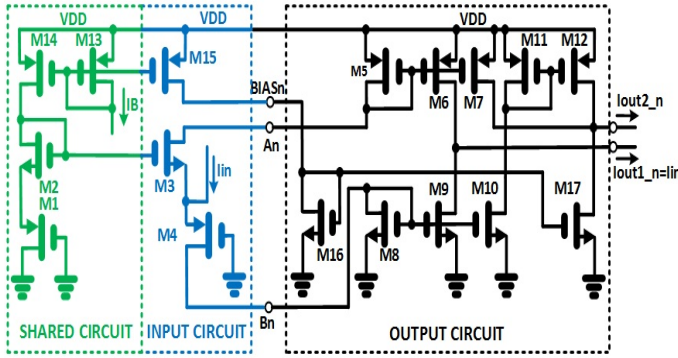


Fig. 2. The squarer cell made by the translinear loop including M1-M4

understanding, the drain current of transistor  $M_m$  is defined as  $I_m$ . Since M1–M4 form a translinear loop, we can write the following equations for such a loop:

$$\sum_{i=1}^2 V_{GSi} = \sum_{i=3}^4 V_{GSi}$$

$$\eta V_T \text{Ln} \left( \frac{I_1}{\left(\frac{W}{L}\right)_1 I_{D0}} \right) + \eta V_T \text{Ln} \left( \frac{I_2}{\left(\frac{W}{L}\right)_2 I_{D0}} \right) =$$

$$\eta V_T \text{Ln} \left( \frac{I_3}{\left(\frac{W}{L}\right)_3 I_{D0}} \right) + \eta V_T \text{Ln} \left( \frac{I_4}{\left(\frac{W}{L}\right)_4 I_{D0}} \right) \quad (3)$$

Assuming that  $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_4$  and  $\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3$ ,  $I_1 \cdot I_2 = I_3 \cdot I_4$ . From Fig. 2,  $I_1 = I_2 = I_B$  and  $I_4 = I_{in} + I_3$ . Thus,

$$I_3^2 + I_{in} I_3 - I_B^2 = 0 \quad (4)$$

$$\Rightarrow I_3 = -\frac{1}{2} I_{in} + I_B \left( 1 + \frac{I_{in}^2}{4I_B^2} \right)^{\frac{1}{2}} \quad (5)$$

Equation (5) can get linearized by Applying power series approximation  $\left( (1+x)^{\frac{1}{2}} \approx 1 + \frac{1}{2}x, -1 \leq x \leq 1 \right)$  results in

$$I_3 = I_6 = I_7 = -\frac{1}{2} I_{in} + I_B + \frac{I_{in}^2}{8I_B}, \quad (6)$$

Accordingly, output currents will be  $I_{out2} = I_7 + I_{12} - I_{17}$ ,  $I_{out1} = I_6 - I_9$ . Based on power series approximation and (5),  $x = I_{in}^2/4I_B^2$ . Therefore, the above results hold for  $-2I_B \leq I_{in} \leq 2I_B$ . For better approximation, x limit could be chosen by  $-0.5 \leq x \leq 0.5$ . Using (6) and  $I_{17} = 2I_B$ , it can be shown that  $I_{out2} = I_{in}^2/4I_B$  and  $I_{out1} = I_{in}$ . It should be noted that n has been applied in naming the nodes in Fig. 2 due to the fact that three squarer cells are used to build the multiplier circuit. Therefore, we use 1,2, and 3 instead of n in the figure showing the full circuit diagram of the multiplier (see Fig. 3).

### C. Multiplier Circuit

Fig. 3 shows the multiplier which is made by combining three squarer cells (see Fig. 1). As mentioned in the previous sections, the multiplier consists of 3 squarer cells and is based on Fig. 1. Thus, there will be 3 translinear loops consisting of M1-M2 and M3-M4 for the first loop, M1-M2 and M5-M6 for the second loop, and finally M1-M2 and M7-M8 for the third loop. According to Fig. 3, M3, M4, M11, output circuit1 block, and shared circuit in green make the first squarer. Also, M5, M6, M12, output circuit2 block, and shared circuit in green make the second squarer. Similarly, M7, M8, M13, output circuit3 block, and shared circuit in green make the third squarer. The currents of M11, M12, and M13 are equal to  $I_B$  which is the bias current.  $I_{out2_1}$  and  $I_{out2_2}$  are equal to  $I_{in1}^2/4I_B$  and  $I_{in2}^2/4I_B$ , respectively. As the input current of the third squarer cell is  $I_{out1_1} + I_{out1_2} = I_{in1} + I_{in2}$ , then the output current of this cell will be equal to  $(I_{in1} + I_{in2})^2/4I_B$ . Also,  $I_{out2_1}$  and  $I_{out2_2}$  are added to form  $(I_{in1}^2 + I_{in2}^2)/4I_B$ . Therefore, the output of the multiplier can be written as  $I_{out} = I_{out2_3} - I_{out2_1} - I_{out2_2} = I_{in1} I_{in2} / 2I_B$  (see Fig. 1 and Fig. 3). From Fig. 1 and Fig. 3, currents  $I_{in1}$ ,  $I_{in2}$ , and  $I_{in1} + I_{in2}$  are the inputs of squarer cell1, squarer cell2, and squarer cell3, respectively.

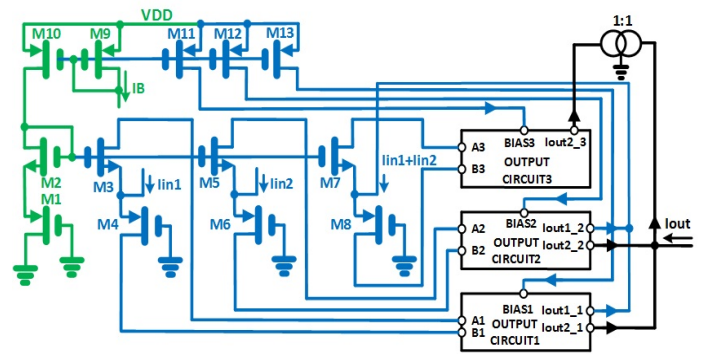


Fig. 3. Complete circuit of the multiplier.

As  $I_{in1} + I_{in2}$  goes to the third squarer cell,  $I_{in1}$  and  $I_{in2}$  should be chosen such that they meet the following criteria

$$|I_{in1} + I_{in2}| \leq 2I_B \quad (7)$$

If x limit of  $-0.5 \leq x \leq 0.5$  were applied, then the criteria would follow  $|I_{in1} + I_{in2}| \leq 2\sqrt{0.5}I_B$ .

#### D. Transconductance mismatch analysis

The effect of transconductance mismatch between NMOS and PMOS transistors in the design can be modeled by considering (2) and re-writing (3) as shown below

$$\begin{aligned} \eta_p V_T L n \left( \frac{I_1}{\left(\frac{W}{L}\right)_1 I_{D01}} \right) - \eta_p V_T L n \left( \frac{I_4}{\left(\frac{W}{L}\right)_4 I_{D04}} \right) &= \\ \eta_n V_T L n \left( \frac{I_2}{\left(\frac{W}{L}\right)_2 I_{D02}} \right) - \eta_n V_T L n \left( \frac{I_3}{\left(\frac{W}{L}\right)_3 I_{D03}} \right) &= \\ (\eta + \delta) V_T L n \left( \frac{I_1}{I_4} \frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_1} \frac{\left(2\eta_p \mu_p C_{ox} V_T^2 \exp^{-\frac{V_{thp}}{V_{GS4}}}\right)}{\left(2\eta_p \mu_p C_{ox} V_T^2 \exp^{-\frac{V_{thp}}{V_{GS1}}}\right)} \right) &= \\ (\eta - \delta) V_T L n \left( \frac{I_2}{I_3} \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_2} \frac{\left(2\eta_n \mu_n C_{ox} V_T^2 \exp^{-\frac{V_{thn}}{V_{GS3}}}\right)}{\left(2\eta_n \mu_n C_{ox} V_T^2 \exp^{-\frac{V_{thn}}{V_{GS2}}}\right)} \right) &= \\ \rightarrow (\eta + \delta) L n \left( \frac{I_1}{I_4} \right) = (\eta - \delta) L n \left( \frac{I_2}{I_3} \right) & \\ \rightarrow I_1^{\eta+\delta} I_3^{\eta-\delta} = I_4^{\eta+\delta} I_2^{\eta-\delta} & \end{aligned} \quad (9)$$

where  $\eta_p = \eta + \delta$  and  $\eta_n = \eta - \delta$ , and  $\delta$  is the slope factor mismatch between NMOS and PMOS transistors.  $V_{GS2} = V_{GS3}$  and  $V_{GS1} = V_{GS4}$  since these transistors have the same bias current  $I_B$ .

### III. SIMULATION RESULTS

The multiplier circuit has been designed in 65nm CMOS technology. The supply voltage and power dissipation are 0.8V and  $0.48\mu\text{W}$ , respectively. Transistor aspect ratios of the squarer cell in Fig. 2 are shown in Table I (squarer cells have the same transistors in aspect ratio), W/L unit of transistors in nm/nm. To bias the devices in weak inversion region, the bias current is set to 200nA. This current is implemented by a simple two-transistor current mirror with a resistor. Post layout simulations have been done on the layout shown in Fig. 4. Both  $I_{in1}$  and  $I_{in2}$  are between  $\pm 200\text{nA}$ . Fig. 5 shows the transient output current for inputs of  $I_1 = 100 \sin(2\pi \times 100\text{kHz} \cdot t)\text{nA}$  and  $I_2 = 100 \sin(2\pi \times 10\text{kHz} \cdot t)\text{nA}$ . The dotted curve shows the transient error of the multiplier which is  $I_{out}$  minus the ideal output. This simulation has been done in SS corner, temperature of  $85^\circ\text{C}$ , and supply voltage of 0.75V.

TABLE I  
TRANSISTOR ASPECT RATIOS

Transistor Name	(W/L)
M1, M4, M17	300/60
M2, M3	180/60
M5-M7, M11-M15	250/60
M8-M10, M16	150/60

Fig. 6 shows dc analysis of the proposed multiplier circuit for different inputs in the range of  $-200\text{nA} \leq I_{in} \leq 200\text{nA}$ .

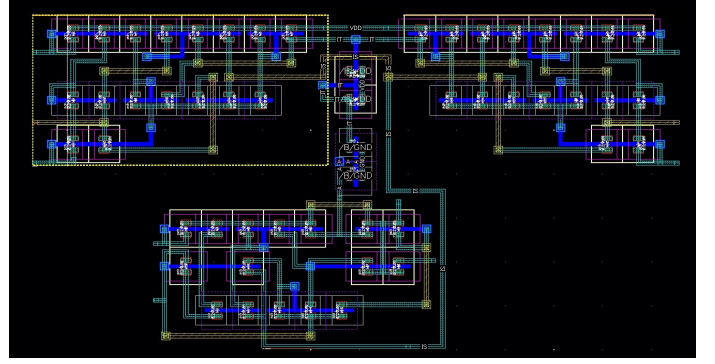


Fig. 4. Layout of the multiplier circuit

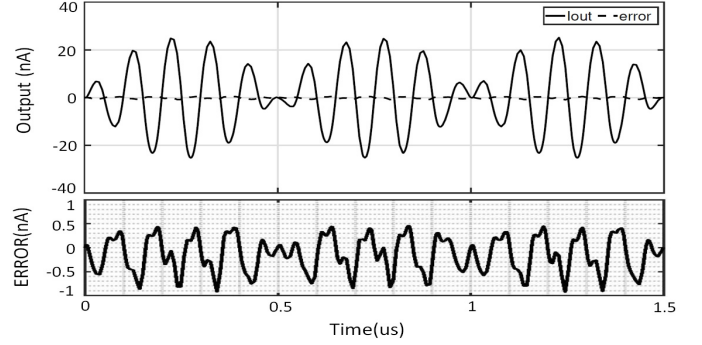


Fig. 5. Multiplication performance of the multiplier with the error.

Table II shows variations of THD, bandwidth, and output

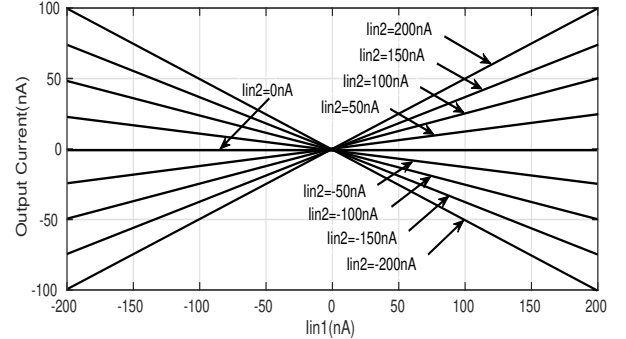


Fig. 6. DC response of the multiplier for both inputs changes.

current error across the different process corners, voltages, and temperature (PVT variations).  $V_{high}$  and  $V_{low}$  are the supply voltages with variations which are equal to  $V_{supply} \times (1+0.05)$  and  $V_{supply} \times (1-0.05)$ , respectively, and error = maximum{(simulated output - ideal output)/(ideal output)}  $\times 100$ . To evaluate the robustness of the multiplier against fabrication process uncertainties, monte carlo analysis with 50 iterations is carried. In addition, monte carlo simulations are done for THD and bandwidth to evaluate the robustness of the multiplier circuit against random mismatches and process corners. Fig. 7 shows the histogram of THD across different process and

TABLE II  
POST LAYOUT PVT VARIATION ANALYSIS

Temp (°C)	THD(%) @100KHz			BW(MHz)			Error(%)		
	-20	20	85	-20	20	85	-20	20	85
$V_{high}$ // SS	1.3	1.25	1.51	2.9	3.8	2.7	2.4	2.1	2.5
$V_{high}$ // FF	1.9	1.35	1.6	3.3	3.5	3.8	2.2	2	2.4
$V_{low}$ // SS	1.83	1.55	1.76	2.5	2.9	3.1	2.6	2.2	2.7
$V_{low}$ // FF	1.59	1.41	1.5	2.9	3.2	3.4	2.8	2.3	2.9

TABLE III  
COMPARISON WITH OTHER MULTIPLIER RESULTS

Parameters	[10]	[11]	This work
Process( $\mu\text{m}$ )	0.18	0.18	0.065
Supply(V)	0.5	1.8	0.8
Input range(nA)	$\pm 0.2$	$\pm 100$	$\pm 200$
Power ( $\mu\text{W}$ )	$0.85 \times 10^{-3}$	1.2	0.48
THD(%)	1.28@1KHz	1.37@100KHz	1.12@100KHz
BW(MHz)	$1.57 \times 10^{-3}$	8.2	3.5
FoM	0.2	500	1302

mismatch corners. The mean value and standard deviation of THD are 1.42% and 0.33% respectively. Fig. 8 shows the histogram of bandwidth across different process and mismatch corners. Fig. 8 indicates the mean value and standard deviation of the bandwidth are 3.4MHz and 0.24MHz respectively.

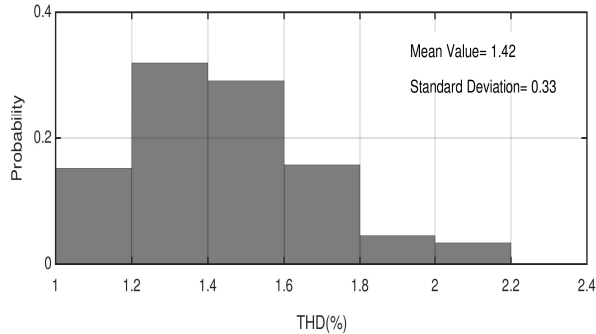


Fig. 7. Monte Carlo analysis result for THD

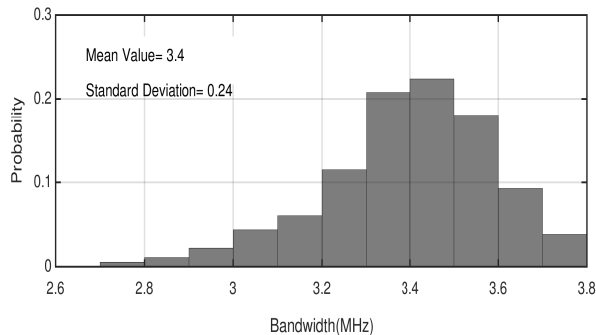


Fig. 8. Monte Carlo analysis result for bandwidth

Table III shows a comparison between this work and the other reported current mode multipliers including transistors working in weak inversion. For performance comparison of multiplier circuits, FOM is defined as

$$\text{FoM} = \frac{\text{BW(MHz)} \cdot \text{Input range(nA)}}{\text{THD(}\% \text{)} \cdot \text{Power}(\mu\text{W})} \quad (10)$$

The multiplier circuit shows better FoM than existing multipliers due to its higher dynamic range and better THD. Another advantage of this circuit is that it can work in scaled CMOS technologies, unlike [11] which requires a high voltage headroom for good dynamic range. Fig. 9 shows THD comparison between this work and [11], THD of which is not depicted for input currents more than 100nA because its input range is  $\pm 100\text{nA}$ . Based on this figure, it can be concluded that up-down structure can improve THD when the transistors work in weak inversion region.

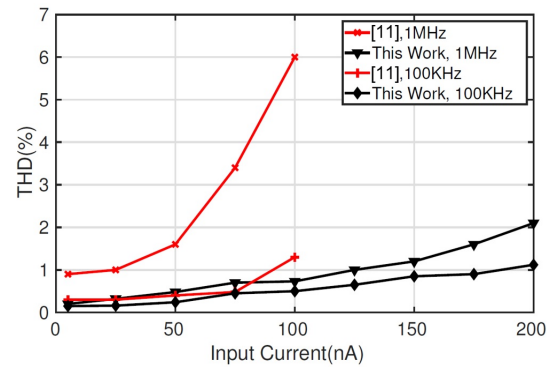


Fig. 9. THD (without applying PVT variations) difference between cascode up-down multiplier (This work) and the folded one [11]

#### IV. CONCLUSION

In this paper, a very low-power current mode multiplier based on MOS translinear loops operating with the devices in weak inversion region is presented. The proposed multiplier has many applications for a wide range of analog signal processing. The results obtained in Sec. III are based on post-layout simulations. Multiplication performance of the circuit at corner cases and Monte Carlo analysis has been investigated for THD, bandwidth, and output current error to verify the circuit performance. Additionally, post layout Monte Carlo for THD as well as bandwidth and PVT variations analysis indicate that the proposed circuit is less dependent on fabrication mismatches.

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