0.43nJ, 0.48pJ/step Second-Order $\Delta\Sigma$ Current-to-Digital Converter for IoT Applications

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***Abstract*—A second-order $\Delta\Sigma$ current-to-digital converter (CDC) for IoT sensing applications is presented in this paper. The proposed CDC uses pseudo-differential current-starved ring oscillators as phase domain integrators. A negative feedback loop relaxes input ring oscillator nonlinearity. The proposed architecture does not require excess loop delay compensation or nonlinearity calibration. Digital differentiation using XOR implements an intrinsic first-order high-pass shaping of static element mismatch in the current steering digital-to-analog converter. A prototype CDC in 65nm CMOS process achieves 62dB dynamic range at 0.48pJ/conversion-step and has 20X better energy-efficiency than state-of-the-art.**

I. Introduction

Current-to-digital converters (CDCs) are used in many applications, including imaging, biosensors [1] and automotives. With emerging internet-of-thing (IoT) applications, very low energy and high speed current sensors are required for a multitude of applications from smart home to automotives. A conventional CDC uses a transimpedance amplifier (TIA) to convert current to voltage followed by an analog-to-digital converter (ADC) to quantize the voltage [2]. While TIA offers a simple solution, it is not very energy-efficient due to the low noise OTA which consumes large power. Another technique is to convert the input current to frequency [3] and using a time quantizer to give a digital output proportional to the input current. While this technique does not use an OTA, input-dependent delay of comparator and switches introduces significant nonlinearity. A recent technique [4] uses a voltage-controlled oscillator (VCO) with a digital infinite-impulse response (IIR) loop filter to realize a highly digital, second order noise shaping CDC. The high gain IIR loop filter suppresses VCO nonlinearity. A digital $\Delta\Sigma$ modulator and explicit dynamic element matching (DEM) is used to suppress static element mismatch in current steering digital-to-analog converter (DAC). The technique in [5] uses an on-chip capacitor to implement a passive integrator and a clocked comparator as quantizer. An explicit DEM is used to suppress DAC mismatch [6].

We propose a simple and highly digital architecture for a $\Delta\Sigma$ CDC that builds upon the second-order modulator presented in [7]. The highly digital nature allows the proposed CDC to operate from low supply voltages and consume low energy which makes it suitable for IoT applications. A negative feedback loop reduces VCO nonlinearity. The proposed architecture does not require excess loop delay (ELD) compensation. A prototype CDC has been fabricated in 65nm process and achieves 62dB dynamic range at 0.43nJ energy. The rest of this paper is organized as follows: Section II presents the proposed architecture and design insights, Section III presents measurement results on the test chip and the conclusion is brought up in Section IV.

II. Proposed CDC

Fig. 1(a) shows the proposed current controlled oscillator (CCO) based CDC architecture. Input current, I_{IN}, is injected into one of the differential CCOs. CCO integrates I_{IN} in phase domain and a phase/frequency detector (PFD) is used to extract the phase difference between the differential CCOs. The PFD extracts the time instants when outputs of the two CCOs cross 2π and encodes this information in the form of UP and DN pulses. This operation is equivalent to having an edge detector after the CCO which outputs dirac delta impulses co-incident with rising edges of CCO output. The impulses are then converted into pulses by the PFD. As shown in [8], a CCO with an edge detector represents a pulse-frequency modulator. The CCO quantization tones pass through the SRO and XOR gates, which act as a sinc filter with nulls at multiples of sampling frequency, f_s, before getting sampled. If the CCO center frequency, f_{cco}, is chosen properly, CCO quantization noise can be adequately suppressed before aliasing into signal band. An optimal choice is selecting f_{cco} such that the quantization aliases remain out-of-band even if f_{cco} varies due to PVT changes. Based on behavioral simulations, setting $f_{cco} = 1.3f_s$ adequately suppresses in-band CCO quantization noise while providing robustness against variations.

The PFD phase output is integrated by a differential switched ring oscillator (SRO). The SRO switches between 2 currents, I_H and I_L, depending on the polarity of the PFD output. Thus, the SRO has very high linearity. The SRO performs another phase-domain integration on the PFD output. SRO phase is multi-bit quantized, digitally differentiated using XOR gates and fed back to the input using a multi-bit digital-to-analog converter (DAC). Similar to the CCO, the SRO can also be modeled by a PFM with the digital differentiation acting as a sinc filter [8]. The SRO sees unfiltered CCO quantization tones at its input and as such its spectral response contains contributions from a large number of inter-modulation products which when sampled form the SRO quantization noise. Since the SRO acts as a modulo integrator and XOR acts as modulo differentiator, the SRO center frequency should be set close to multiples of f_s to avoid phase overflow [9].

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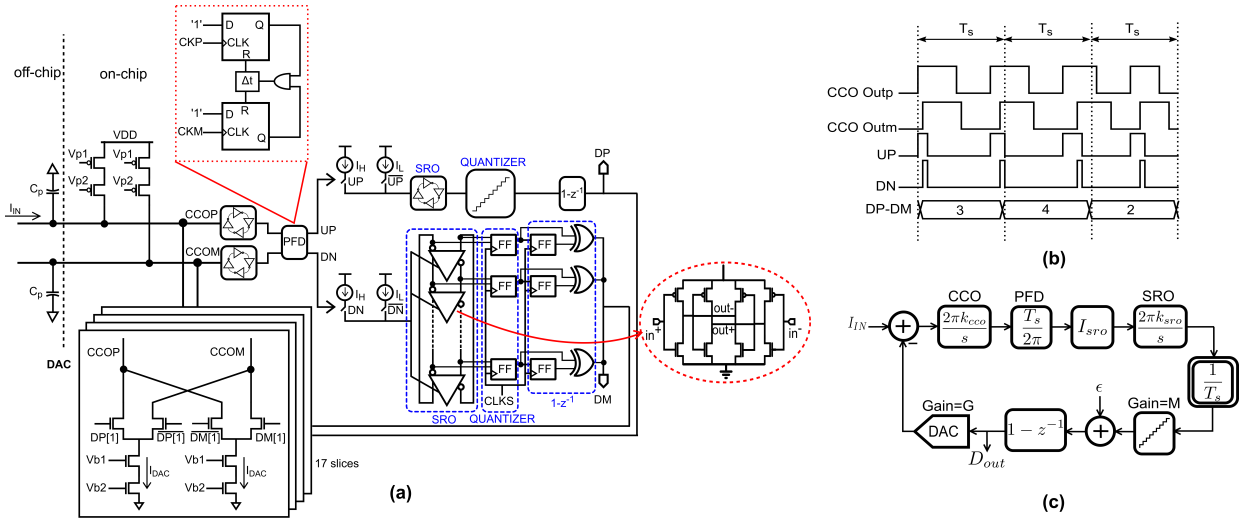

Fig. 1. (a) Proposed CDC architecture (b) timing diagram (c) simplified linear model

As shown in Fig. 1(a), the DAC consists of 17 NMOS cascode current sources with PMOS cascode current load. The cascode PMOS current loads are sized up to reduce random mismatch and flicker noise. Static mismatch in the NMOS current sources are first-order high-pass shaped by intrinsic data weighted averaging (DWA) pattern in SRO output [10], [11]. The two SROs quantize alternate half-cycles of the input current, i.e, DP is the quantized version of I_{IN} when $I_{IN} > 0$ and DM is the quantized version of I_{IN} when $I_{IN} < 0$. The DAC combines DP and DM such that the feedback current tracks I_{IN} and the CCOs sees small input current swing. The improved CCO linearity comes at the cost of static current consumption of $2N \cdot I_{DAC}$ in the DAC. Fig. 1(b) shows the timing diagram for the proposed CDC and Fig. 1(c) shows simplified linear model of the CDC. Using impulse-invariance transform, the CDC digital output, D_{out} can be written as

$$D_{out} = \frac{H\left(z^{-1}+z^{-2}\right)I_{IN} + 2\epsilon\left(1-z^{-1}\right)^2}{2+\left(HG-2\right)z^{-1}+\left(HG\right)z^{-2}} \quad (1)$$

where $H = 2\pi I_{sro} k_{cco} k_{sro} N T_s^2$, $I_{sro} = (I_H - I_L)$, N is the number of DAC elements, k_{cco} is the input CCO gain, k_{sro} is the SRO gain, T_s is the sampling period, ϵ is the SRO quantization noise and G is the gain of the N-element DAC. It can be seen from (1) that the proposed CDC high-pass shapes quantization noise to the second-order. Quantization noise from only SRO is considered because the CCO quantization noise is adequately suppressed at the output by sinc filter as mentioned earlier. It should be noted here that parasitic capacitances at the CCO input, denoted by C_p in Fig. 1(a) add a third pole to the NTF but that pole is far away from the signal band to significantly affect the CDC transfer function.

The proposed CDC has two integrators in a loop and has to be designed carefully to ensure stability. For the system to be stable, the integrators should not saturate, i.e, the PFD and SRO should not overflow. In addition, excess loop delay (ELD) can introduce additional pole in the system and degrade stability [12], more so, since a non-return-to-zero (NRZ) DAC

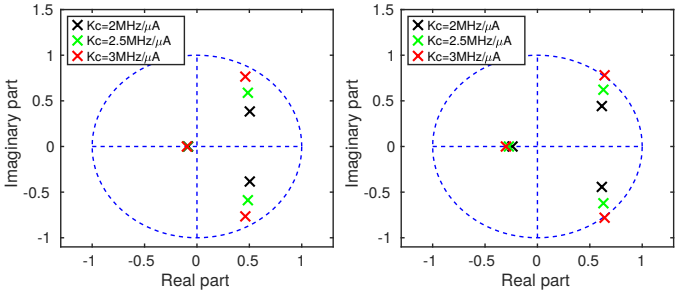

Fig. 2. z-domain poles of NTF for (a)$\tau = 0.4T_s$; and (b)$\tau = 0.8T_s$

is used to suppress clock jitter. Loop stability can be analyzed by looking at the poles of the noise transfer function (NTF) as a function of τ. Fig. 2 shows z-domain poles of the NTF versus ELD for different values of k_c=k_{cco}=k_{sro}. As can be seen from Fig. 2, as long as CCO and SRO gains remain below 2.5MHz/μA, the NTF poles remain inside unit circle and the loop can absorb an ELD of $0.8T_s$. The upper bound on the SRO gain, k_{sro}, for no phase overflow is given by $I_{sro} \cdot k_{sro} \cdot T_s \leq 0.5$. Setting $k_{sro} = 2.5$MHz/μA and $T_s = 5$ns, $I_{sro} \leq 40\mu$A. For the PFD to not overflow, the input current swing seen by the CCOs cannot exceed a certain limit. Input swing of the CCO is given by $(G \cdot D_{out} - I_{IN})$ and from (1), it can be seen that the input swing of the CCOs is set primarily by the out-of-band quantization noise. In order to find the maximum input handling capability of the CCOs, a simulation is performed by sweeping LSB step size (I_{DAC}) and recording SNR and CCO input swing. The CCO gain is kept at 2.5MHz/μA. The results are shown in Fig. 3. It can be seen that as I_{DAC} exceeds 5μA, the CCO input swing rises sharply which causes PFD overflow and the SNR to drop. From Fig. 3 it can be seen that higher I_{DAC} improves SNR as the CDC can support larger I_{IN} but setting I_{DAC} too high makes the loop unstable. In order to not exercise the nonlinear

region of the CCO, I_{DAC} is set to 4.5μA for this design. Monte-carlo simulations are performed across mismatch and PVT corners to check the variation of I_{DAC}. Fig. 4 shows the result of monte-carlo simulations. It can be seen that the standard deviation of I_{DAC} is 0.03μA and I_{DAC} does not exceed 4.8μA, thus, guaranteeing stability of the CDC.

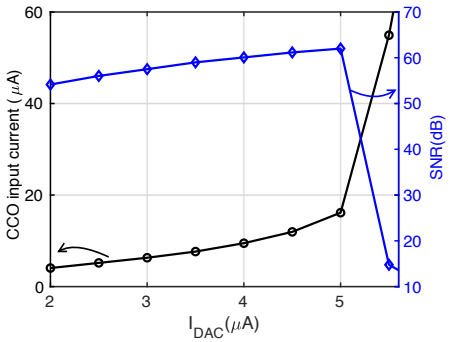

Fig. 3. CCO input swing and SNR versus I_{DAC}

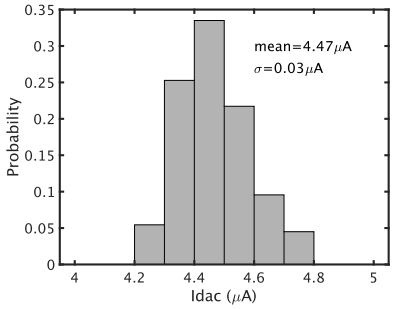

Fig. 4. Monte-carlo simulation results for I_{DAC}

To investigate the effect of variations in loop parameters on CDC stability, we varied the loop parameters, $k_{cco}, k_{sro}, I_{DAC}$ and I_{sro}. For this simulation, we assumed the four parameters vary independently with a standard deviation, σ_m, which is varied from 0 to 20%. The CDC is simulated 50 times for each perturbation. The SNDR is plotted versus σ_m in Fig. 5. It can be seen that increase in σ_m does not significantly change the SNDR upto $\sigma_m = 20\%$ but the standard deviation of SNDR increases. The dotted lines indicate the upper and lower bounds of SNDR and even with 20% variation in the loop parameters, the minimum SNDR is 59dB.

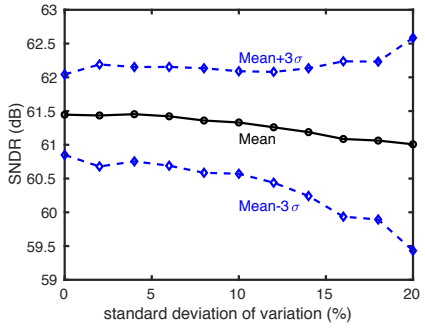

Fig. 5. SNDR vs perturbations in loop parameters

CDC noise is dominated by thermal and flicker noise from the input CCOs, thermal noise from the DAC, and quantization noise. Noise from the SRO is high-pass shaped and does not dominate the CDC noise. PMOS tail current source is used to reduce flicker noise from the CCO. Noise from CCO and DAC is calculated by referring the phase noise at the CCO output back to the CDC input. The simulated phase noise plot for CCO+single-ended DAC is shown in Fig. 6. Simulated flicker noise corner of the CCO+DAC combination is close to 100KHz. The input referred noise due to CCO+DAC is given by

$$\sqrt{\overline{i_{th,n}^2}} = \sqrt{2} \cdot \frac{\sqrt{2DT_s}}{2\pi k_{cco} T_s} \cdot \frac{1}{\sqrt{OSR}} \tag{2}$$

where the factor $\sqrt{2}$ takes into account the noise from different CCO and DAC. The phase diffusion constant D is given by $D = \phi(\Delta\omega).(\Delta\omega)^2/2$ where $\phi(\Delta\omega)$ is the phase noise at an offset frequency of $\Delta\omega$. At an offset frequency of 0.16MHz, the phase noise is -81.5dBc/Hz. For k_{cco} of 2.2MHz/μA, sampling frequency of 200MHz and OSR of 100, the input referred CCO+DAC noise is given by 12.7nA,rms.

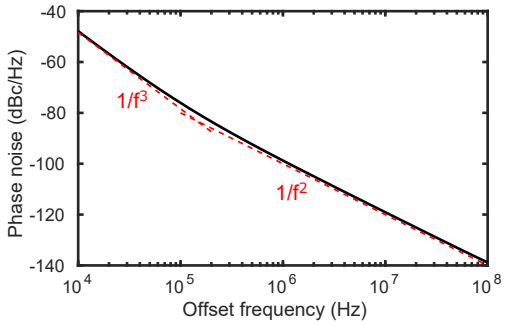

Fig. 6. Simulated CCO+DAC phase noise

Input referred quantization noise is given by

$$\sqrt{\overline{i_{q,n}^2}} = \frac{2I_{DAC}/N}{\sqrt{12}} \cdot \frac{\pi}{\sqrt{5}} \cdot (OSR)^{-5/2} \tag{3}$$

For an OSR of 100, the input referred quantization noise is given by 0.04nA,rms. While the in-band quantization noise is much lower than in-band thermal noise, the in-band quantization noise will increase to 4.7nA,rms if it is only first-order shaped. The quantization noise calculation does not take into account folding of quantization noise into signal band due to CCO nonlinearity. To evaluate the effect of quantization noise folding, behavioral simulation is performed with a 6-bit linear CCO. Fig. 7 shows the CDC spectra for a sinusoidal current input of $48\mu A_{pk-pk}$ and frequency of $f_s/2110$. For an ideal CCO, the SQNR is given by 96.7dB. With a 6-bit linear CCO, quantization noise folds back into the signal band and raises the noise floor. The SQNR is reduced to 73.2dB with 6-bit CCO. With addition of thermal noise, the SNR becomes 61.6dB.

III. Measurement Results

Fig. 8 shows die photograph and layout of a prototype CDC fabricated in 65nm process. The active core occupies an area

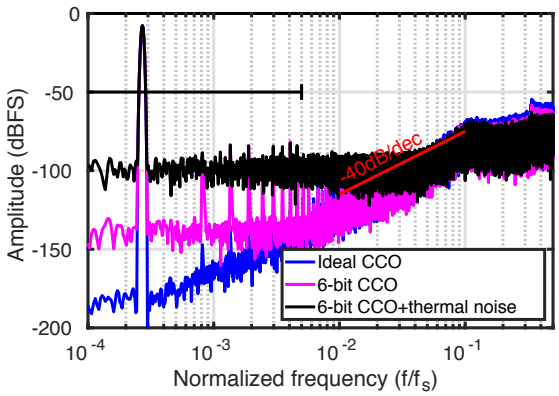

Fig. 7. CDC spectra for sinusoidal input with 16X averaging

of 0.06mm^2. The test chip consumes 0.87mW power operating from 1.2V supply at a sampling frequency of 205MHz.

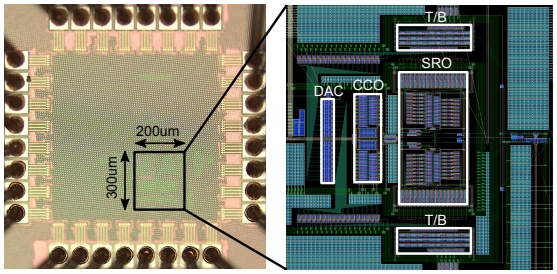

Fig. 8. Chip microphotograph and layout

TABLE I
COMPARISON WITH STATE-OF-THE-ART CDCS.

	[5]	[2]	[1]	**This work**
Process(nm)	350	180	180	**65**
Supply(V)	1.5	1.8	1.8	**1.2**
Energy	67nJ	1.48μJ	–	**0.43nJ**
Conv. time	4ms	0.62ms	–	**0.5μs**
Max. input(A)	3μ	21n	1μ	**48μ**
DR(dB)	77.4	77	60	**62**
ENOB	12.5	12	9.9	**9.8**
FoM$_w$[1](pJ/step)	11.3	259	–	**0.48**

[1]FoM$_w$ = Energy/2^{ENOB}

Fig. 9 shows the differential non-linearity (DNL) and integral non-linearity (INL) plots of the CDC output after decimation. The CDC has a DNL of $0.32/-0.24$ LSB and an INL of $0.38/-0.37$ LSB. The CDC performance is also tested by applying a sine wave input of 48μA peak-peak at a frequency of 100KHz and the spectrum is shown in Fig. 10. The CDC has an SNDR of 60.6dB and SNR of 60.9dB over a bandwidth of 1MHz. Second-order quantization noise shaping can be clearly seen in Fig. 10. Fig. 11 shows the SNDR variation as the ac input current amplitude is swept. The proposed CDC has a 62dB dynamic range for bandwidth of 1MHz.

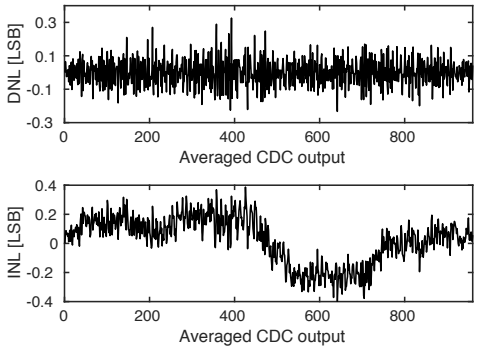

Fig. 9. CDC DNL and INL plot

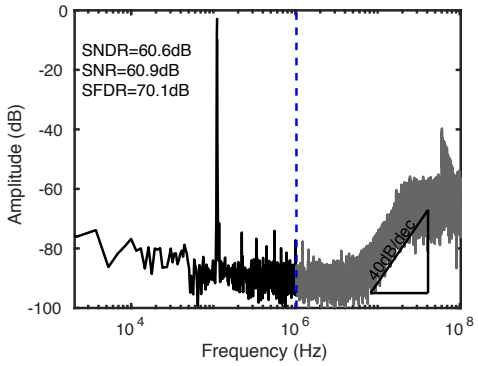

Fig. 10. CDC spectrum for $48\mu\text{A}_{pk-pk}$ input

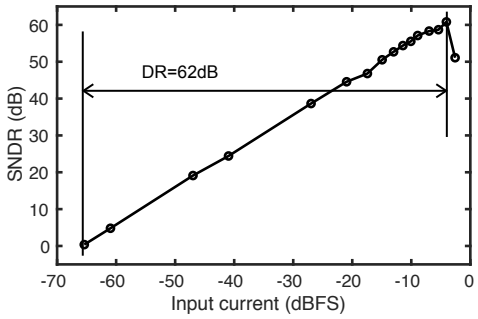

Fig. 11. SNDR versus input amplitude sweep

The prototype CDC is compared with state-of-the-art CDCs in Table I. Thanks to its highly digital nature, the proposed CDC has much lower energy consumption than state-of-the-art. The prototype requires only 0.5μs conversion time and has a very low energy consumption of 0.43nJ which makes it useful for real-time IoT sensing applications. The CDC dynamic range and ENOB can be further improved by using chopping to reduce flicker noise. As can be seen from Table I, the proposed CDC has 20X better energy efficiency than state-of-the-art CDC.

IV. CONCLUSION

This paper presented a highly digital, ring oscillator based second-order $\Delta\Sigma$ CDC. The proposed architecture does not require any nonlinearity calibration or excess loop delay compensation. A prototype CDC fabricated in 65nm CMOS process achieves close to 20X better energy efficiency than state-of-the-art.

V. Acknowledgment

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References

[1] M. M. Ahmadi and G. A. Jullien, "A wireless-implantable microsystem for continuous blood glucose monitoring," *IEEE Trans. Biomedical Circuits and Systems*, vol. 3, no. 3, pp. 169–180, 2009.

[2] R. T. Heitz, D. B. Barkin, T. D. O'Sullivan, N. Parashurama, S. S. Gambhir, and B. A. Wooley, "A low noise current readout architecture for fluorescence detection in living subjects," in *IEEE ISSCC*, 2011, pp. 308–310.

[3] X. Wang, W. Wong, and R. Hornsey, "A high dynamic range CMOS image sensor with inpixel light-to-frequency conversion," *IEEE Trans. electron devices*, vol. 53, no. 12, pp. 2988–2992, 2006.

[4] P. Prabha, S. J. Kim, K. Reddy, S. Rao, N. Griesert, A. Rao, G. Winter, and P. K. Hanumolu, "A highly digital VCO-based ADC architecture for current sensing applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1785–1795, 2015.

[5] H. Son, H. Cho, J. Koo, Y. Ji, B. Kim, H.-J. Park, and J.-Y. Sim, "A Low-Power Wide Dynamic-Range Current Readout Circuit for Ion-Sensitive FET Sensors," *IEEE transactions on biomedical circuits and systems*, vol. 11, no. 3, pp. 523–533, 2017.

[6] W. Mao, Y. Li, H. Chun-Huat, and Y. Lian, "High Dynamic Performance Current-Steering DAC Design With Nested-Segment Structure," *IEEE TVLSI systems*, vol. 26, no. 5, pp. 995–999, 2018.

[7] V. Prathap, S. T. Chandrasekaran, and A. Sanyal, "2nd-Order VCO-based CT $\Delta\Sigma$ ADC architecture," in *IEEE MWSCAS*, 2017, pp. 687–690.

[8] E. Gutierrez, L. Hernandez, F. Cardes, and P. Rombouts, "A pulse frequency modulation interpretation of VCOs enabling VCO-ADC architectures with extended noise shaping," *IEEE TCAS–I*, vol. 65, no. 2, pp. 444–457, 2018.

[9] G. Taylor and I. Galton, "A mostly-digital variable-rate continuous-time delta-sigma modulator ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, 2010.

[10] T.-K. Jang, J. Kim, Y.-G. Yoon, and S. Cho, "A Highly-Digital VCO-Based Analog-to-Digital Converter Using Phase Interpolator and Digital Calibration," *IEEE TVLSI system*, vol. 20, no. 8, pp. 1368–1372, 2011.

[11] K. M. AL-Tamimi and K. El-Sankari, "Preweighted Linearized VCO Analog-to-Digital Converter," *IEEE TVLSI systems*, vol. 25, no. 6, pp. 1983–1987, 2017.

[12] J. A. Cherry and W. M. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 4, pp. 376–389, 1999.