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Advances in Voltage-Controlled-Oscillator-Based ΔΣ ADCs

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SUMMARY Ring voltage-controlled-oscillators (VCOs) are increasingly being used to design ΔΣ ADCs. They have the merits of simple, highly digital and low-voltage tolerant, making them attractive alternatives for the classic scaling-unfriendly operational-amplifier-based methodology. This paper aims to provide a summary on the advancement of VCO-based ΔΣ ADCs. The scope of this paper includes the basics and motivations behind the VCO-based ADCs, followed by a survey covering a wide range of architectures and circuit techniques in both continuous-time (CT) and discrete-time (DT) implementation, and will discuss the key insights behind the contributions and drawbacks of these architectures.

key words: *voltage-controlled-oscillator, ring oscillator, analog-to-digital converter, time-domain signal processing, VCO-based ADC, ΔΣ ADC*

1. Introduction

Oversampling analog-to-digital converters (ADCs), or more generally known as ΔΣ ADCs, possess the merits of realizing high accuracy conversion with coarse quantizer as well as a relaxed analog anti-aliasing filter requirement, making them crucial building blocks in many systems, such as mobile, radar, and instrumentations. In the era of Internet of things (IoT) where a larger scale of sensing and communication is foreseen, ΔΣ ADCs are expected to show a growing significance. On the other hand, the voltage-domain, analog-intensive nature of many classic ΔΣ ADC architectures makes them increasingly challenging to design under the trend of process scaling. Their key building blocks: the high-gain operational transconductance amplifiers (OTAs) and precision comparators, suffer from performance degradation as a result of voltage supply and transistor intrinsic gain reduction in advance processes, leading to power and area penalty. It therefore presents a strong need for new design frameworks for ΔΣ ADCs that can leverage the properties of CMOS scaling instead of limited by it, as to cater for the stringent power efficiency requirements of emerging applications. In recent years, a lot of research efforts have been devoted to designing ΔΣ ADCs in a "more-digital, less-analog" mindset [1].

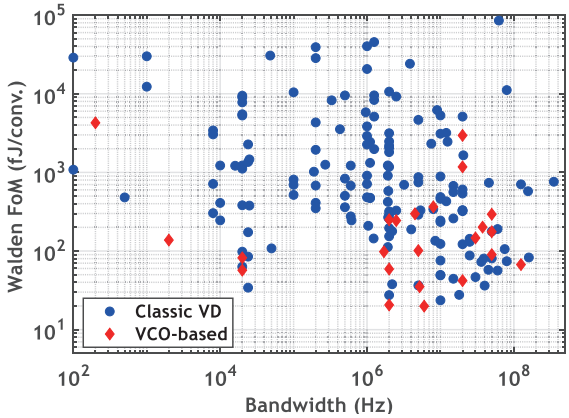

Fig. 1 Power efficiency comparison between VCO-based and classic VD ΔΣ ADCs.

Among these efforts comes a promising direction of time-domain (TD) analog signal processing. It exploits TD variables such as frequency, phase and delay in lieu of voltage to process analog signal in simple digital-like circuits (e.g., flip-flops and inverters), thus allowing analog circuits to harness process scaling for better performance. One notable representation of this framework is the use of ring voltage-controlled-oscillators (VCOs) as the integrator and quantizer of a ΔΣ ADC. The ring-VCO-based integrator and quantizer exhibits several key merits: 1) It utilizes the inherent integration from frequency to phase, thus providing infinite DC gain with little voltage headroom and intrinsic gain limitation. 2) Multilevel quantization can be obtained simply by either using an edge-triggered counter or decoding the bit pattern of the ring VCO nodes, hence obviating the need for precise reference level generation and relaxing the comparator design. 3) It is built with inverters, thus is easy to design. 4) Its operation is mostly dynamic and characterized by VCO gain, delay and/or timing-resolution, thus harnessing better performance naturally from process scaling. These advantages make the VCO-based implementation an attractive replacement candidate for the OTA-and-flash based counterpart and have motivated many silicon prototyping. Figure 1 compares state-of-the-art VCO-based

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ADCs with classic VD designs using data from [2] and ADCs reported in recent JSSC, CICC, ASSCC and ESSCIRC. The energy efficiency of different ADCs is compared using the well-known Walden figure-of-merit (FoM) given by FoMw = Power/($2^{ENOB}\times 2\times$BW), where ENOB and BW are the effective number of bits and the Nyquist bandwidth of the ADC, respectively. It can be clearly seen from Fig. 1 that state-of-the-art VCO-ADCs can achieve better energy efficiency than classic ΔΣ ADCs.

Despite the many advantages described above, in practice the performance of a VCO-based ADC yet depends on how efficient it can address the two key concerns of the ring VCO's non-ideal effects: the voltage-frequency conversion non-linearity and the sensitivity to process-voltage-temperature (PVT) variation. This has thus fostered a vigorous research prospect and led to a rich set of architectures and circuit techniques being proposed in recent years. Some have demonstrated open-loop VCO-based ADCs with calibration that attained a highly digital nature. Some advocated using closed-loop structure for a more robust nonideality mitigation. Apart from these two popular trends, subranging or hybrid structures have also been demonstrated as an efficient way by unifying the VCO with the merits of other ADCs. These diverse approaches have provided different perspectives about VCO-based ADCs. The aim of this paper is to provide a comprehensive survey on state-of-the-art VCO-based ΔΣ ADCs. This survey will cover a wide range of architectures and circuit techniques as possible in both continuous-time (CT) and discrete-time (DT) implementation, and will discuss the key insights behind the contributions and drawbacks of these architectures.

This paper is organized as follows. Section 2 will revisit the basics of the VCO-based integrator to familiarize readers with essential backgrounds. In Sect. 3, a review on CT VCO-based ADC will be presented. The discussion on DT architectures will follow in Sect. 4. On top of the discussion on ADC, Sect. 5 will be dedicated to touch upon other analog circuits that exploit the VCO-based techniques to provide a broader scope. The paper will then be concluded in Sect. 6.

2. Basics of VCO-Based Integrators

2.1 VD Integrator vs. TD Integrator

Integrators are key functional blocks in building the loop filter of a ΔΣ ADC. In classic VD designs, the integrators are generally composed of two operations (from a CT perspective): a transconductor first turns input voltage into current, then a capacitor integrates the current and output the result as voltage. The most commonly used integrator in VD CT ΔΣ ADC is the OTA-based active-RC integrator as shown in Fig. 2 (a). The OTA ideally is to provide a virtual ground, allowing the resistor to serve as a linear transconductor for V_{IN} and hence setting the integration bandwidth by 1/RC. The active-RC integrator is robust against active component (i.e. the OTA) non-idealities and variations. It however has

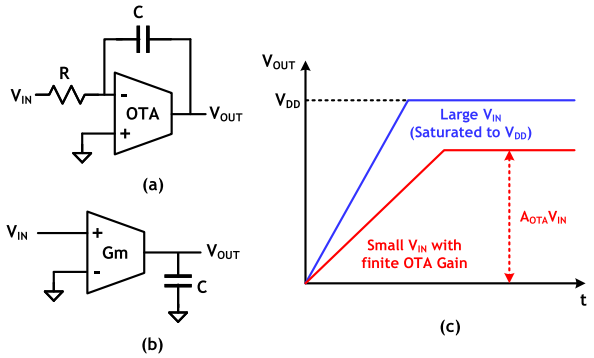


Fig. 2 (a) OTA-based active-RC integrator. (b) Gm-C integrator. (c) Output behavior of a VD integrator with a constant non-zero input.

the drawback of requiring the OTA gain-bandwidth (GBW) to be much larger than 1/RC. Intuitively, it is because the OTA needs to set up its internal voltage fast enough to preserve a good virtual ground, as to avoid disturbing the integration path and causing excess loop delay (ELD). For this reason, active-RC integrators tend to be power hungry. Another type of VD integrator is the Gm-C structure as depicted in Fig. 2 (b). The Gm-C integrator uses the OTA in an open-loop fashion and directly as the transconductor for V_{IN}, defining its integration bandwidth as g_m/C. Alternatively speaking, this integrator uses the OTA's raw frequency response for integration, hence can achieve high speed with much better efficiency compared to active-RC integrators. Nevertheless, the Gm-C integrator has the downside of poor linearity, making them less attractive especially in ΔΣ ADCs using single-bit quantizers.

Regardless of the implementation, VD integrators share two common traits that their output range is practically bounded by the power supply levels and their DC integration is limited by the OTA gain, as suggested in Fig. 2 (c). Relating to the context of the ΔΣ ADC, larger integrator output range and low-frequency gain are utterly helpful to relax the thermal noise budget and improve noise shaping quality. Nevertheless, technology scaling leads both output range and DC gain of the VD integrator to the deteriorating direction, therefore much increasing the design difficulty.

Apart from relying on current and capacitor to obtain integration in the voltage domain, a frequency modulation device, such as a VCO, is an alternative way to implement an integrator by observing the phase, as it is the inherent integration of the frequency. Ring oscillators are mostly used in this regard. Their phase is manifested as the propagation of the interstage node ripple, which can be easily read out through digital logics. Without loss of generality, here we use a three-stage CMOS-input current-starved ring VCO, as shown in Fig. 3 (a), to help elucidate the feature of a TD integrator. In this oscillator, the input voltages are applied to the tail devices. Through this it adjusts the charging and discharging strength of the inverters, so that the gate delay and eventually the frequency can be modulated by the input. The interstage node voltage waveform is illustrated in Fig. 3 (b).

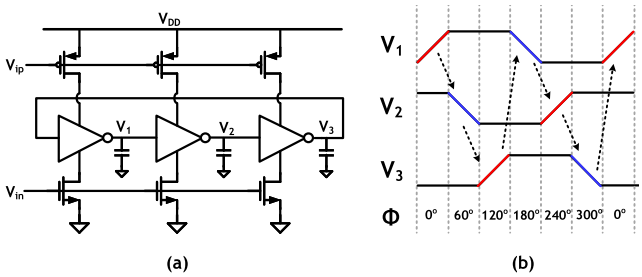


Fig. 3 (a) Example current-starved VCO. (b) Simplified internal node voltages behavior and phase mapping.

Table 1 Comparison of VD and TD integrators.

Integrator type	Active-RC	Gm-C	VCO
Output quantity	Voltage	Voltage	Phase
DC gain	Finite	Finite	Infinite
Saturation-free	No	No	Yes
Low-VDD tolerant	No	No	Yes
Speed-power ratio	Low	High	High
Linearity	High	Low	Low

In this figure, we approximate the charging/discharging of a delay stage to the first order as a constant-slope ramp.

With a closer look into Fig. 3, a subtle connection can be drawn between the VCO-based integrator and the VD counterpart, which offers us insights about their comparison. Firstly, it can be seen that the underlining physics of phase integration is essentially charging/discharging capacitors similar to that of the VD integration. Yet instead of getting the integration result from the voltage quantity itself, VCO-based integration goes after the phase information reflected by the voltage variation. Thus, it does not require low-noise, low-offset comparator to quantize. Secondly, the operation of a single delay cell when transitioning is similar to a Gm-C integrator. But unlike Gm-C integrator whose integration is eventually limited by the power rail or the OTA gain, the VCO delay cell's voltage ramping will be continued by the next stage without saturating. The VCO therefore can be regarded as a distributed Gm-C integrator but with infinite DC gain. *In other words, a VCO integrator share the same efficiency benefits as the Gm-C while obviating the drawbacks of VD integration, making it well suited in deep-scale processes*. The comparison is summarized in Table 1.

2.2 Common Phase Quantizers

While the phase is a continuous quantity, the discrete, stage-by-stage structure and digital-like transition of the ring VCO embeds an intrinsic quantization mechanism for its phase, as suggested in Fig. 3 (b). In a typical VCO-based ADC design, the VCO will generally be followed by a phase quantizer that exploits this mechanism to extract the VCO's phase as digital codes. In this subsection we will go over the most commonly used phase quantizers.

The first and most straightforward phase quantizer is to use an edge-triggered counter, as illustrated in Fig. 4. Under this scheme, the counter will be incremented by one

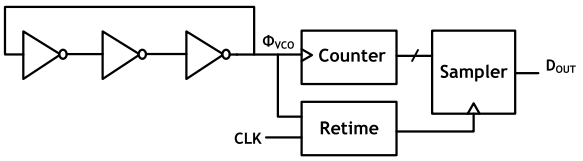
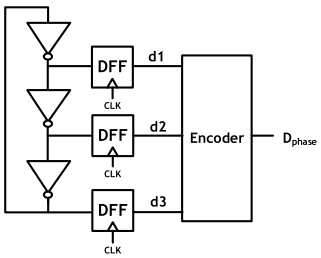


Fig. 4 Phase quantizer using edge counting.



Encoder Truth Table

[d1 d2 d3]	D_{phase}
010	0
110	1
100	2
101	3
001	4
011	5

Fig. 5 Phase quantizer through phase encoding.

in each oscillation cycle, hence the corresponding phase-domain quantization step is 2π. The output range is determined by the bit width of the counter and thus can be flexibly reconfigured even after fabrication. Meanwhile, the counting scheme exhibits several disadvantages. Due to the relatively large quantizer step, it necessitates a VCO free running frequency much higher than the sampling rate in order to get sufficient phase excursion in one sampling period to lower the quantization noise, which makes it power consuming and brings high VCO phase noise. In addition, since the counter runs asynchronously to the sampler clock, a careful handshake is required to prevent sampling at the counter transition. This also brings considerable power and hardware overhead.

Another widely adopted phase quantizer leverages the fact that the spatial bit patterns of the ring VCO nodes are distinct for each transition within an oscillation cycle. Digital representation of the phase can therefore be obtained by encoding the bit patterns, as depicted in Fig. 5. This scheme offers a finer phase quantization step of π/N, where N is the number of ring stages, thus can use a lower VCO free running frequency to reduce noise and power. Handshake is also not required. On the other hand, the output range of this scheme is fixed to 2N. The range can be extended by using the counting scheme together with the encoding scheme. This also help alleviate the former's VCO speed requirements.

A third commonly seen phase quantizer incorporates XOR gates, a usage inherited from the phase-locked loops. As illustrated in Fig. 6, an XOR gate translates the phase difference between the VCO and a reference phase (can be from another VCO) into a pulse-width-modulated (PWM) waveform. By using an array of XOR gates at all nodes of the ring, a series of evenly delayed PWM waveform can be obtained. The combination of all XOR outputs will naturally produce a thermometer-coded representation of the phase as a form of spatial averaging. Similar to the encoder scheme, the XOR approach also does not require high

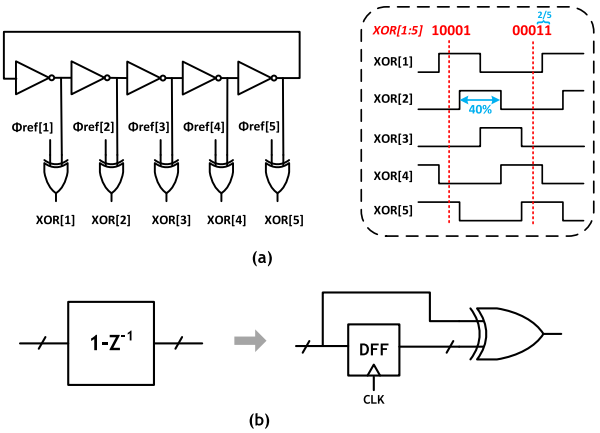


Fig. 6 (a) Phase quantizer using XOR array. (b) Fast phase differentiator (frequency detector) using XOR.

VCO free running frequency. Furthermore, it supports high-speed operation due to its simplicity. It directly performs subtraction on the phase, thus can implement the differentiation block [Fig. 6 (b)] needed in open-loop VCO-based ADCs (more details in Sect. 3) in a highly efficient way. The downside of the XOR-based method is that it only support an output range of N, which is lower than both of the aforementioned methods.

Since each phase quantizer has its pros and cons, it is eventually the VCO-based ADC's architecture choice that determine which phase quantizer suites the best. Generally, the counting and encoder schemes are mostly employed by open-loop VCO-based ADCs, where large latency can be tolerated. For close-loop design that are sensitive to loop delay, the XOR methods are preferred.

3. Review of CT VCO-Based ΔΣ ADCs

Phase by nature is the continuous integration of frequency. If there is no sampling operation between the voltage-to-frequency conversion, the VCO automatically serves as a CT integrator. Owing to this nature, a majority of the VCO-based ADCs reported belong to the category of CT ΔΣ ADC. CT ΔΣ ADCs are attractive candidates for high-bandwidth applications. Their loop filters are free of settling and front-end sampling, thus largely relaxes the device speed and ADC driver complexity. In addition, they also have the benefit of inherent anti-aliasing filtering. In this section, we will review a variety of CT VCO-based ADC implementations. To facilitate a clearer big picture, we will layout the discussion according to the two fundamental architecture choices: open-loop and closed-loop[†].

[†]Terminology explanation: in this paper, the terms open-loop and close-loop are used based on whether the VCO frequency or phase is used as the quantizer output. The frequency-output scheme can attain first-order noise shaping without feedback, while the phase-output scheme requires feedback. For works that use frequency-output VCO as part of a closed-loop ΔΣ ADC, we still categorize them to the discussion of open-loop designs.

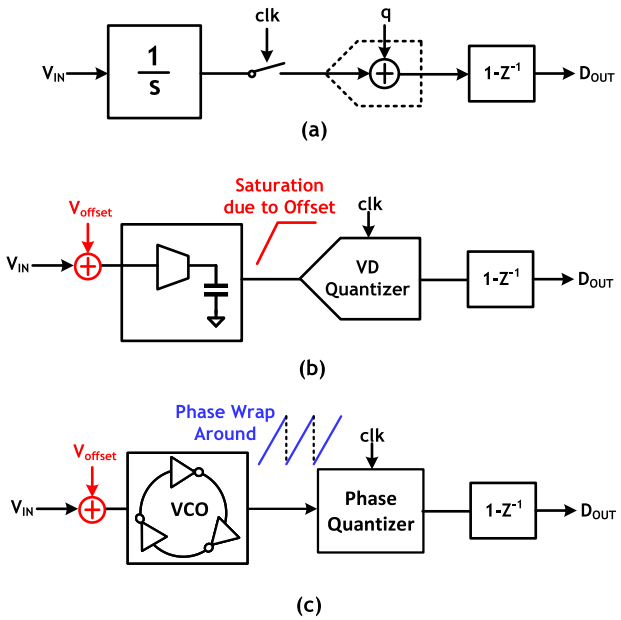


Fig. 7 (a) Conceptual block diagram of a first-order open-loop ΔΣ ADC. (b) VD implementation suffers from saturation due to offset. (c) VCO-based integrator is saturation-free, allows open-loop implementation.

3.1 Open-Loop CT VCO-Based ADC

In theory, ΔΣ modulation or noise shaping can be achieved in an open-loop fashion. A first-order example is illustrated in Fig. 7. In practice, such structure is deemed impractical for VD implementation. This is because any DC offset presented at the integrator input will cause the integrator to ramp and eventually saturate. For this reason, VD ΔΣ ADCs are generally implemented in a closed-loop manner, so that the integrator can be stabilized by the feedback. Yet the feedback path necessitates a digital-to-analog converter (DAC), whose non-idealities (e.g. non-linearity and timing jitter) have a high impact to the ADC's performance. Hence, the design of a classic VD ΔΣ ADC usually involves substantial optimizing effort, power and area cost on the feedback DAC.

On the other hand, unlike the VD integrator, in the VCO integrator the phase will not saturate but only wrap around when it reaches the quantizer output range, hence the integration property can always be preserved. This opens up new possibilities for open-loop ΔΣ ADC to be realized by using a VCO-based integrator, whose block diagram is illustrated in Fig. 7 (c). Due to DAC-less and mostly digital structure, the open-loop VCO-based ADC exhibits great potential in terms of compactness, high speed and simplicity. Hovin *et al.* [3] pioneered an early implementation of such design. In this work, the quantizer was implemented by the encoder scheme. Meanwhile, the measurement results of this work also revealed that the VCO nonlinearity is a key concern. It showed that under a 5-V supply, the linearity of the VCO becomes less than 7 bits when the input amplitude

goes beyond 150 mV.

Back in Hovin's time, the efficiency gap between analog and digital circuits was still narrow. As process scaling rolled on, the benefits of the VCO-based ADC began to attract a rapidly growing attention starting from the mid 2000's and motivated vigorous research efforts. A main pursuit in the open-loop VCO-based ADC research is to address the VCO non-linearity, so that they can be more practical for a wider range of applications that require converting large swing signals.

A direction researchers have explored is to design highly linear VCOs. Wismar *et al.* [4], [5] devised a ring VCO design that uses the transistor bulk as the control node and created a soft supply for the ring using a PMOS buffer similar to that of a low-dropout regulator. The soft supply will reduce as the VCO current increases, so it can compensate the non-linearity in the bulk control. Nevertheless, this approach can only support limited input swing as to avoid turning on the bulk diode, and has only been demonstrated under a 0.2-V-supplied design. Voelker *et al.* [6] identified that the finite input impedance and the short circuit current during transition is two major sources of non-linearity for a drain-injected current-controlled oscillator (CCO). They implemented a feedback loop to reduce the input impedance and developed a break-before-make delay cell topology to reduce the shoot through current, allowing the ADC to achieve 83-dBc supurious-free-dynamic-range (SFDR) with 1-V_{PP} input swing.

Another interesting idea is to use only two levels to control the VCO, such that the effective transfer characteristic is inherently linear. An example implementation is reported in [7], where the input is first turned into a PWM signal, then drive the open-loop VCO-based ADC. However, one must be aware that despite the burden on VCO linearity is relaxed, it is transfered to the PWM generation, which brings its own complexity.

Apart from the focus on VCO design and control method, using calibration to address the non-linearity in the digital domain is another well-known practice for open-loop VCO-based ADCs. Kim *et al.* [8] and Daniels *et al.* [9] reported implementations in a foreground manner, where an explicit ramp signal is used to extract the nonlinearity coefficients, as illustrated in Fig. 8. A lookup table (LUT) will then be generated based on the coefficients to remap the output. While foreground calibration schemes are relatively straightforward and low in hardware complexity, they do not track the coefficient drift over process, PVT variations and device aging. Alternatively, the works reported in [10], [12] moved the nonlinearity estimation from foreground to background by dedicating a replica VCO for the calibration unit, such that the calibration operation does not intervene with the signal path (Fig. 9). Taylor and Galton [10], [11] leveraged dithering to extract the nonlinearity terms while Rao [12] employed a background ramping similar to the aforementioned foreground idea. The dithering method in [10], [11] in theory can work without using the replica, but the calibration convergence will be highly

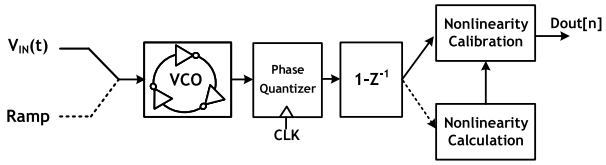


Fig. 8 Open-loop VCO-based ΔΣ ADC using foreground nonlinearity calibration [8], [9].

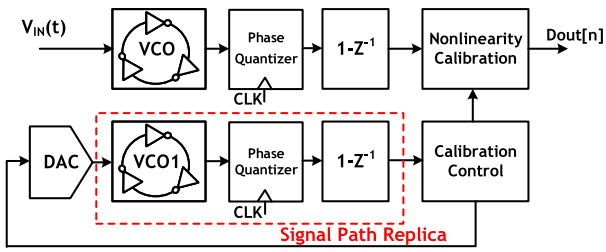


Fig. 9 Open-loop VCO-based ΔΣ ADC using background nonlinearity calibration [10]–[12].

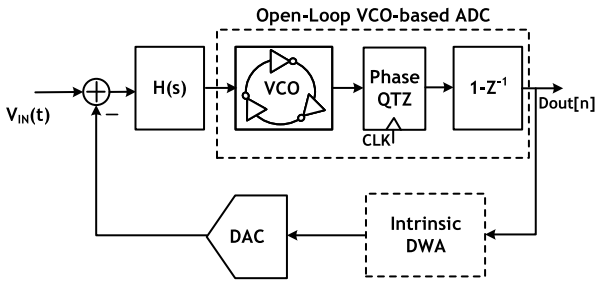


Fig. 10 Using a ΔΣ loop to suppress the nonlinearity of the open-loop VCO-based ADC [14].

elongated in the presence of input signal. The drawback of these works, nonetheless, lies on the difficulty of guaranteeing the replica matches well with the signal-path VCO. The mismatch between the VCOs will lead to degraded correction results. Another background calibration technique reported in [13] suggests using a split ADC method. Under this idea, the signal will be converted in parallel by two VCO-based ADC paths that are complementarily dithered. The nonlinear terms of both paths can be calculated by comparing the difference of the comparison results, hence it is robust against mismatch. Nevertheless, it pays the price of doubling the power and hardware.

Other than using the above methods, Straayer and Perrott [14] embedded the open-loop VCO-based ADC inside a classic OTA-based ΔΣ loop as a quantizer in place of a flash (Fig. 10). The idea is to use the active-RC integrator preceding the VCO-based quantizer to suppress the VCO nonlinearity. The active-RC together with the VCO provide in total second-order noise shaping. This work highlights that by using the XOR-based phase differentiator, the VCO quantizer output can produce an intrinsic data-weighted averaging pattern, allowing feedback DAC nonlinearity to be mitigated without needing any explicit dynamic element match-

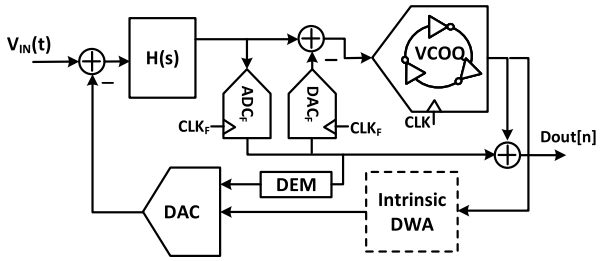


Fig. 11 Using a ΔΣ loop and sub-ranging to suppress the nonlinearity of open-loop VCO-based ADC [15].

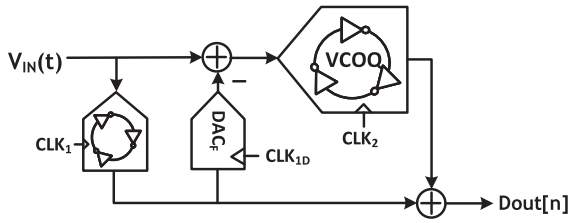


Fig. 12 Two-stage open-loop VCO-based CT ΔΣ ADC [16].

ing (DEM). Yet the use of active-RC loop filter introduces large power overhead and degrades the scaling friendliness. Its non-linearity suppression relying on the front-end integrator will also be ineffective when the oversampling ratio (OSR) is low.

Yet another category of linearizing an open-loop CT VCO-based ADC have been reported is the use of a sub-ranging or two-step structure. Reddy *et al.* [15] presented a implementation that is similar to [14] with a OTA-based ΔΣ loop (Fig. 11). But an extra coarse stage, which is comprised of a flash ADC and current DAC, is inserted in front of the VCO. By doing this, the VCO only needs to handle the small residue voltage from the coarse stage, thus induces a much smaller non-linear effect. The drawback of this work is that it is vulnerable to the interstage gain error between the coarse stage and the VCO, as well as the coarse DAC linearity. In addition, explicit DEM is required for the feedback path from the coarse stage. Another two-stage CT architecture was reported in [16]. In this work, the first-stage quantizer is also implemented by a VCO-based ADC (Fig. 12). This idea allows the design to be insensitive to the gain error (noise leakage) and DAC mismatch, since the first stage quantization noise is shaped and the DAC is intrinsically DWA shuffled. Despite the first-stage VCO sees full signal swing, its harmonics will be largely canceled at the second-stage output, thus incurs minimum impact on the performance.

The open-loop VCO-based ADC we have discuss so far are all first-order implementations (not counting the extra order provided by the active-RC in [14], [15]). In fact, higher-order noise shaping has also been demonstrated in open-loop designs. Recently, a third-order VCO-based ADC is reported in [17], whose block diagram is shown in Fig. 13. An enhanced linearity open-loop VCO is cascaded with a second-order ΔΣ loop consisting of digital con-

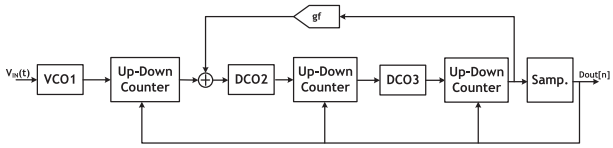


Fig. 13 Mostly digital third-order CT ΔΣ ADC using open-loop VCO, DCO and up-down counters [17].

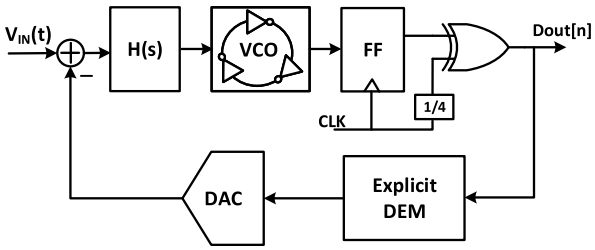


Fig. 14 Closed-loop VCO-based ADC using phase as output [18].

trolled oscillators (DCO) and counters to provide overall third-order shaping. The overall technique is highly digital and very suitable for design in scaled technologies with low supply voltages. Foreground calibration is employed in this work to mitigate the first VCO's nonlinearity.

3.2 Closed-Loop CT VCO-Based ADC

While many techniques have been demonstrated to address the linearity issue of open-loop VCO-based ΔΣ ADCs, the PVT sensitive tuning gain of the VCO is another less addressed concern. Since the full scale of an open-loop VCO-base ADC is defined by the VCO tuning gain, this nonideality leads to a large variation on the analog-to-digital mapping and may result in unexpected over range without sufficient back-off. To further improve the full-scale stability and VCO linearity, another trend of design implemented VCO-based ADC in the closed-loop ΔΣ fashion, as illustrated in Fig. 14. In this case, the VCO phase will serve directly as the output of the ADC, as in contrast to the open-loop case that uses the frequency. Compared to open-loop design, closed-loop VCO-based ADCs provide stable full scales defined by the DAC reference and feedback factor. Park and Perrott [18] reported an early implementation of the closed-loop scheme. Using an extra active-RC loop filter in conjunction with the VCO, this work implemented fourth-order noise shaping.

Despite being more robust against the VCO nonlinearity and PVT variation, using the closed-loop structure raises its own concerns on several fronts, as shown by the work in [18]. Firstly, the need for a feedback DAC apparently adds power and hardware overhead. Furthermore, the phase-based output in this work, which is obtained through XOR logic and internal divided reference phases, does not come with the intrinsic DWA mechanism as the frequency-based output does. It hence costs even more to implement an explicit DEM to reduce the DAC nonlinearity. Reddy *et al.* [19] proposed using frequency output in conjunction with

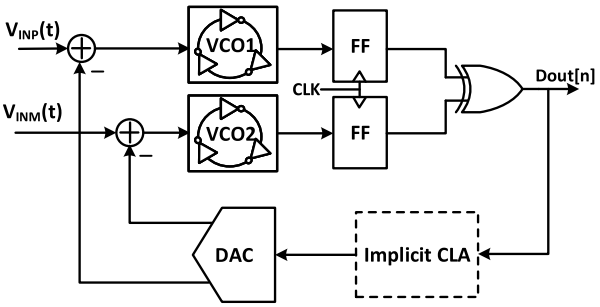


Fig. 15 Closed-loop VCO-based ADC using the dual-VCO architecture [21].

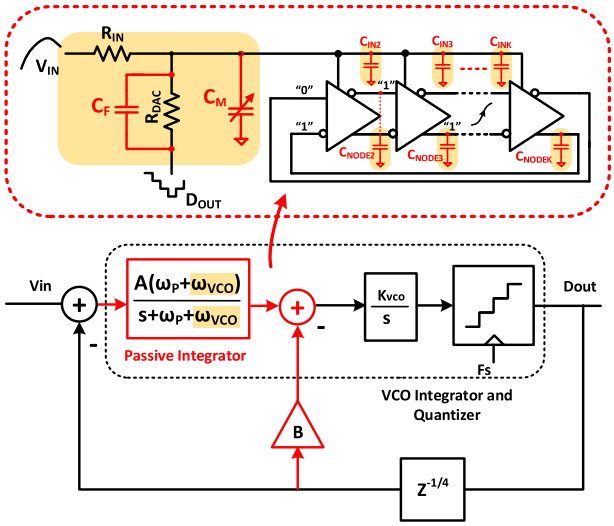


Fig. 16 Second-order VCO-based ADC hybridizing a inherent passive integrator with a VCO integrator [25].

phase output, such that the frequency path can provide a fast feedback to allow more delay on the phase path to generate the DEM. This relaxed the DEM circuit speed; but the complexity is not fully removed. A phase rotator technique was recently reported in [20]. This technique embeds ELD compensation inside the quantizer and facilitate the use of segmented DAC with 7b quantizer resolution.

Lee *et al.* [21] proposed a dual-VCO scheme aiming to overcome the aforementioned drawbacks of the phase-output architecture. In this scheme, two VCOs are used in the quantizer, as depicted in Fig. 15, with their phases serving as reference for the other. The key advantages of the dual-VCO scheme are two-fold. First and foremost, it brings back the intrinsic dynamic element matching mechanism in the form of clock level averaging (CLA). It is qualitatively proved that the phase detector (PD) output of the dual-VCO phase quantizer is a PWM of the ADC input. This PWM waveform has a carrier frequency of $2f_{VCO}$, where f_{VCO} is the VCO free running frequency. The PWM modulates DAC mismatch to $2f_{VCO}$ and away from the signal band. The second key advantage is noise reduction. As phase in the dual-VCO scheme is self-referenced, the free-running frequency of the VCOs can be set arbitrarily, as long as the PWM artifacts are kept away from signal band. This allows the VCO to operate at a low frequency, which lowers the bias power and especially the phase noise. An improved version is reported in [22]. A background calibration methods are proposed to further mitigate DAC mismatch as to allow a more compact design. This work also presented an interesting modular layout approach that facilitate fast redesign and migration.

To further improve the efficiency of the dual-VCO structure, Li *et al.* [23] proposed a phase extended quantization (PEQ) scheme. By using an efficient set of digital gates on top of the XOR phase detector, this technique enables lead-lag detection on the dual VCO phases, which effectively doubles the quantizer resolution without increasing number of the VCO stages and samplers. In addition to resolution doubling, the PEQ also directly facilitates CLA-embedded tri-level DAC control, which enables power reduction for the DAC. A reference-side switching resistor DAC (RDAC) is used in conjunction with the PEQ. This combination introduces a dynamic power scaling mechanism in the feedback DAC, which enables the DAC to burn power only when it is needed. Measurement results of this work demonstrated that the synergy of dual VCO, PEQ and tri-level RDAC enables a closed-loop design to attain leading power efficiency among all VCO-based ADCs and also a broader scope of ΔΣ ADCs.

Another key concern in closed-loop VCO-based ΔΣ ADC design is to realize high-order noise shaping in a power efficient manner. The works reported in [18]–[20] realized high order by employing additional OTA-based loop filter with the VCO. However, due to the involvement of OTAs, their power efficiencies are deteriorated compared to first-order designs, which can be implemented purely by VCO and mostly digital components. The scaling friendliness brought by the VCO is also negated when using OTAs. It is therefore meaningful to seek alternative approach that can extend the merits of the VCO to higher-order designs.

As part of this effort, Young *et al.* [24] proposed using VCOs as the front-end loop filter and minimized the involvement of the OTA by moving it to the last stage only as a summing amplifier. Nevertheless, it sacrifices the inherent TD quantization and requires an explicit VD quantizer. Its implementation of the VCO-based loop also necessitates high-speed charge pumps to convert signal from TD back to VD, which increases the circuit complexity and limits the power efficiency.

Li and Sun [25] proposed a hybrid passive RC and VCO architecture, as shown in Fig. 16. It makes use of the fact that the VCO has infinite DC gain and can achieve high bandwidth easily from its Gm-C-like mechanism (as mentioned in Sect. 2) to support the entire loop gain without needing extra gain block, thus allowing the use of passive network to minimize the power for order boosting. Another highlight of this work is that its passive stage is realized through the inherent parasitic effect of the VCO. By doing so, it not only obviates the need for parasitic mitigation, but

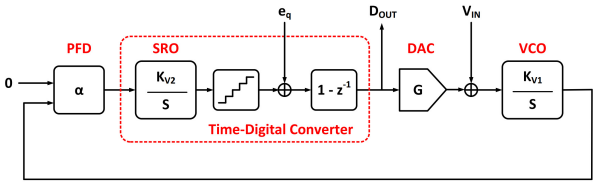


Fig. 17 Second-order VCO-based ADC using a modified DPLL structure [26].

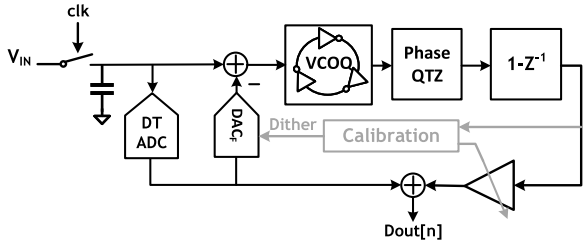


Fig. 18 A generic block diagram of a DT two-stage VCO-based ADC [27]–[30].

also avoids adding noise when forming the parasitic loop filter.

Leveraging the similarity between a digital phase-locked loop (DPLL) and a CT ΔΣ ADC, Zhong *et al.* [26] demonstrated a purely-VCO-implemented second-order design modified from a DPLL structure, whose block diagram in shown in Fig. 17. The idea is to use the PLL's main VCO as the first-stage integrator and uses a noise-shaping TDC, which consists of a switched ring oscillator (SRO), as the quantizer to achieve two noise-shaping order while maintaining a most-digital structure. A highlight of this work is that the noise-shaping TDC can provide tri-level control with intrinsic DWA mechanism, hence allowing the DAC to achieve low noise and low distortion simultaneously.

4. Review of DT VCO-Based ΔΣ ADCs

While the majority of VCO-based ADCs are CT designs, as we have reviewed in the previous section, there are also VCO-based ADCs designed in a DT nature. To be exact, they are generally two-step architectures that hybridize a DT front-end ADC with an open-loop VCO-based ADC as the back-end stage, as depicted in Fig. 18. Due to the noise-shaping nature of the VCO-based ADC, they can also be referred as 0-1 MASH. By using different types of front-end sub ADCs, the hybrid ADC can obtain various extra benefits compared to a standalone VCO-based design. This section will be devoted to review some of the state-of-the-arts belong to this type.

One category of the 0-1 MASH VCO-based ADCs employs flash ADCs as the front-end stage, as reported in [27], [28]. The high-speed nature of the flash ADC adds minimum timing overhead while can effectively reduce the OSR requirement for a given resolution target. Hence, this category is attractive for high-bandwidth purposes. However, due to the relatively low resolution achievable by the flash ADC, the VCO-based back-end needs to process a relatively large residue voltage, making linearity a concern. Ghosh and Pamarti [27] presented a design using a 2b front-end flash. In this design, they leverage dithering to linearize the VCO by randomizing the residue voltage. It makes the spectrum of the residue voltage appear white, so the nonlinearity of the VCO will not cause signal harmonics from the residue voltage. Another work presented by Ragab and Sun [28] used a 14-level flash quantizer. In this work, dither-based background calibration technique, which are similar to those in [10], [11], are employed to mitigate the VCO linearity. But unlike those works that need a replica VCO, this work performs calibration directly on the signal path and thus allows a better calibration accuracy. The reason that direct signal path calibration is practical in this work is because the VCO only process residue voltages that are comparable to the amplitude of the dither, hence adding much less interference to the calibration convergence.

While hybridizing with a flash can promote speed, another category of designs chooses to combine with a successive-approximation-register (SAR) ADC for further improvement in power efficiency and scaling friendliness, as reported in [29], [30]. A SAR ADC is highly digital and is one of the most energy-efficient ADC architectures, specially at medium resolutions (e.g., 6 to 10 bits). A SAR ADC can provide finer quantization of the input signal than a flash ADC while consuming much smaller power. Hence, the residue of the SAR stage is more randomized and smaller than that of the flash, thus obviating the need for calibration/dithering to suppress the VCO nonlinearity. As a trade-off, this category is less suitable for high-speed operation.

As a final remark, like any generic two-stage architectures, these works are not exempt from the influence of interstage gain error, which will lead to noise leakage and nonlinearity. While using the VCO to directly provide the interstage gain can obviate the need for an explicit residue amplifier to save power, it also exacerbates the interstage gain issue due to the PVT-sensitive nature of the VCO. These works generally employed background calibration to mitigate the effect of the VCO gain variation.

5. VCO-Based Analog Circuits beyond ΔΣ ADCs

The main scope of this paper has been focused on the involvement of VCO-based techniques in ADC design. Nonetheless, it is worth noting that under the broad scope of TD analog signal processing, VCO-based techniques have also brought new perspectives in several other applications. This section will touch upon some of the representative works that have contributed to this efforts.

Drost *et al.* [31] proposed a fourth-order Butterworth filter built purely using VCOs, phase detectors and charge pumps. The VCO assumes the role of an integrator in lieu of the OTA in the biquad implementation. This work demonstrated operation under 0.55-V supply with state-of-the-art

total harmonic distortion (THD) and dynamic range (DR).

Lu *et al.* [32] demonstrated using VCO and phase detector in a closed-loop to implement a PWM generator (similar to the closed-loop VCO-based ADC described in Sect. 3 but without sampling). Such implementation obviates the need for a CT comparator and high-linearity ramp generator, allowing a higher speed PWM. This PWM generator is designed to drive a class-D amplifier.

Kim *et al.* [33] presented using VCO and voltage-controlled delay line to realize a proportional-integral-derivative (PID) controller for a DC-DC converter. Similar to [32], the closed-loop context of the VCO-based PID controller allows the PWM switching control to be generated by simply adding a phase detector. It demonstrated an efficient replacement for the classic high-bandwidth error amplifier and analog PWM generator used in DC-DC converter control.

Apart from applications in filter and power management, there also have been vigorous research efforts in using VCO-based techniques in sensor interfaces. Published works have cover temperature sensing [34], current sensing [35], capacitance sensing [36], [37], as well as biomedical and neural interfaces [38]–[40]. Noteworthily, open-loop VCO-based quantizers exhibits high suitability for biomedical sensing, where signal amplitudes are small. Open-loop VCO quantizers can handle such small signal with good linearity without needing calibration. Meanwhile, the high VCO gain available in advanced processes allows small signals to be read out in high resolution.

6. Conclusion

This paper has presented a summary on the advancement of VCO-based ΔΣ ADCs, covering discussions from basic ideas to a survey on recent, state-of-the-art implementations. Currently, VCO-based ADCs have been demonstrated in three major architectures: open-loop CT, closed-loop CT and hybrid DT. Each architecture has its own advantages and drawbacks. From the authors' point of view, there is no architecture that holds an absolute superiority over the others. It is ultimately the context of application that determines which is more appropriate to be adopted. For example, open-loop VCO-based ADCs provides greater benefits in small-input applications, such as bio-signal sensing. This is because with small signal, the non-linearity issue becomes less critical, allowing the fully-digital nature to be effectively harnessed. Closed-loop CT architecture demonstrates better suitability for large signal conversion with their merits in linearity and calibration-free. When it comes to high-resolution purposes, the hybrid DT scheme can provide a better way as they combine sub-ranging, noise-shaping and ease of calibration synergically.

Going beyond the diversity of implementations, with their digital-centric nature in common, VCO-based ADCs' performance is expected to improve as CMOS technology scaling continues. This is still very much an active area of research with many research groups, including the authors, contributing to this area. It is also expected that there will be more innovative architectures that will further extract the merit of this framework and push the envelope of bandwidth and power to unprecedented levels.

References

[1] J.M. de la Rosa, R. Schreier, K.-P. Pun, and S. Pavan, "Next-Generation Delta-Sigma Converters: Trends and Perspectives," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol.5, no.4, pp.484–499, Dec. 2015.
[2] B. Murmann. "ADC Performance Survey 1997-2018". [Online] Available: http://web.stanford.edu/ murmann/adcsurvey.html
[3] M. Hovin, A. Olsen, T.S. Lande, and C. Toumazou, "Delta-sigma modulators using frequency-modulated intermediate values," IEEE Journal of Solid-State Circuits, vol.32, no.1, pp.13–22, Jan. 1997.
[4] U. Wismar, D. Wisland, and P. Andreani, "A 0.2V 0.44 μW 20 kHz Analog to Digital ΣΔ Modulator with 57 fJ/conversion FoM," Proceedings of the 32nd European Solid-State Circuits Conference, pp.187–190, Sept. 2006.
[5] U. Wismar, D. Wisland, and P. Andreani, "A 0.2V, 7.5 μW, 20 kHz ΣΔ modulator with 69 dB SNR in 90 nm CMOS," Proceedings of the 33nd European Solid-State Circuits Conference, pp.206–209, Sept. 2007.
[6] M. Voelker, S. Pashmineh, J. Hauer, and M. Ortmanns, "Current Feedback Linearization Applied to Oscillator Based ADCs," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.61, no.11, pp.3066–3074, Nov. 2014.
[7] S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, and P.K. Hanumolu, "A 71dB SFDR open loop VCO-based ADC using 2-level PWM modulation," IEEE Symposium on VLSI Circuits, pp.270–271, June 2011.
[8] J. Kim, T.-K. Jang, Y.-G. Yoon, and S. Cho, "Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.57, no.1, pp.18–30, Jan. 2010.
[9] J. Daniels, W. Dehaene, M. Steyaert, and A. Wiesbauer, "A 0.02mm^2 65nm CMOS 30MHz BW all-digital differential VCO-based ADC with 64dB SNDR," IEEE Symposium on VLSI Circuits, pp.155–156, June 2010.
[10] G. Taylor and I. Galton, "A Mostly-Digital Variable-Rate Continuous-Time Delta-Sigma Modulator ADC," IEEE Journal of Solid-State Circuits, vol.45, no.12, pp.2634–2646, Dec. 2010.
[11] G. Taylor and I. Galton, "A reconfigurable mostly-Digital Delta-Sigma ADC with a worst-Case FOM of 160 dB," IEEE Journal of Solid-State Circuits, vol.48, no.4, pp.983–995, April 2013.
[12] S. Rao, K. Reddy, B. Young, and P.K. Hanumolu, "A deterministic digital background calibration technique for VCO-Based ADCs," IEEE Journal of Solid-State Circuits, vol.49, no.4, pp.950–960, April 2014.
[13] J. McNeill, R. Majidi, J. Gong, and C. Liu, "Lookup-table-based background linearization for VCO-based ADCs," Proceedings of the IEEE Custom Integrated Circuits Conference, pp.1–4, Sept. 2014.
[14] M.Z. Straayer and M.H. Perrott, "A 12-Bit, 10-MHz bandwidth, continuous-time ΣΔ ADC with a 5-Bit, 950-MS/s VCO-Based quantizer," IEEE Journal of Solid-State Circuits, vol.43, no.4, pp.805–814, April 2008.
[15] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, and P.K. Hanumolu, "A 16-mW 78-dB SNDR 10-MHz BW CTΔΣADC Using Residue-Cancelling VCO-Based Quantizer," IEEE Journal of Solid-State Circuits, vol.47, no.12, pp.2916–2927, Dec. 2012.
[16] X. Xing and G.G.E. Gielen, "A 42 fJ/Step-FoM Two-Step VCO-Based Delta-Sigma ADC in 40 nm CMOS," IEEE Journal of Solid-State Circuits, vol.50, no.3, pp.714–723, March 2015.
[17] A. Babaie-Fishani and P. Rombouts, "A Mostly Digital VCO-Based

CT-SDM With Third-Order Noise Shaping," IEEE Journal of Solid-State Circuits, vol.52, no.8, pp.2141–2153, Aug. 2017.
[18] M. Park and M.H. Perrott, "A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-TimeΔΣADC With VCO-Based Integrator and Quantizer Implemented in 0.13μm CMOS," IEEE Journal of Solid-State Circuits, vol.44, no.12, pp.3344–3358, Dec. 2009.
[19] K. Reddy, S. Dey, S. Rao, B. Young, P. Prabha, and P.K. Hanumolu, "A 54mW 1.2GS/s 71.5dB SNDR 50MHz BW VCO-based CT ΔΣ ADC using dual phase/frequency feedback in 65nm CMOS," IEEE Symposium on VLSI Circuits, pp.C256–C257, June 2015.
[20] S.-J. Huang, N. Egan, D. Kesharwani, F. Opteynde, and M. Ashburn, "28.3 A 125MHz-BW 71.9dB-SNDR VCO-based CT ΔΣ ADC with segmented phase-domain ELD compensation in 16nm CMOS," IEEE International Solid-State Circuits Conference, pp.470–471, Feb. 2017.
[21] K. Lee, Y. Yoon, and N. Sun, "A Scaling-Friendly Low-Power Small-AreaΔΣADC With VCO-Based Integrator and Intrinsic Mismatch Shaping Capability," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol.5, no.4, pp.561–573, Dec. 2015.
[22] Y. Yoon, K. Lee, S. Hong, X. Tang, L. Chen, and N. Sun, "A 0.04-mm^{2}0.9-mW 71-dB SNDR distributed modular AS ADC with VCO-based integrator and digital DAC calibration," IEEE Custom Integrated Circuits Conference, pp.1–4, Sept. 2015.
[23] S. Li, A. Mukherjee, and N. Sun, "A 174.3-dB FoM VCO-Based CT ΔΣ modulator with a fully-Digital phase extended quantizer and tri-Level resistor DAC in 130-nm CMOS," IEEE Journal of Solid-State Circuits, vol.52, no.7, pp.1940–1952, July 2017.
[24] B. Young, K. Reddy, S. Rao, A. Elshazly, T. Anand, and P.K. Hanumolu, "A 75dB DR 50MHz BW 3rd-order CT-Δσ modulator using VCO-based integrators," IEEE Symposium on VLSI Circuits, pp.1–2, June 2014.
[25] S. Li and N. Sun, "A 0.028mm^2 19.8fJ/step 2nd-order VCO-based CT ΔΣ modulator using an inherent passive integrator and capacitive feedback in 40nm CMOS," IEEE Symposium on VLSI Circuits, pp.C36–C37, June 2017.
[26] Y. Zhong, S. Li, A. Sanyal, X. Tang, L. Shen, S. Wu, and N. Sun, "A Second-Order Purely VCO-Based CT ΔΣ ADC Using a Modified DPLL in 40-nm CMOS," IEEE Asian Solid-State Circuits Conference, pp.93–94, Nov. 2018
[27] A. Ghosh and S. Pamarti, "Linearization Through Dithering: A 50 MHz Bandwidth, 10-b ENOB, 8.2 mW VCO-Based ADC," IEEE Journal of Solid-State Circuits, vol.50, no.9, pp.2012–2024, Sept. 2015.
[28] K. Ragab and N. Sun, "A 12-b ENOB 2.5-MHz BW VCO-Based 0-1 MASH ADC With Direct Digital Background Calibration," IEEE Journal of Solid-State Circuits, vol.52, no.2, pp.433–447, Feb. 2017.
[29] A. Sanyal and N. Sun, "A 18.5-fJ/step VCO-based 0-1 MASH ΔΣ ADC with digital background calibration," IEEE Symposium on VLSI Circuits, pp.1–2, June 2016.
[30] S.-E. Hsieh and C.-C. Hsieh, "A 0.4V 13b 270kS/S SAR-ISDM ADC with an opamp-less time-domain integrator," IEEE International Solid - State Circuits Conference, pp.240–242, Feb. 2018.
[31] B. Drost, M. Talegaonkar, and P.K. Hanumolu, "Analog Filter Design Using Ring Oscillator Integrators," IEEE Journal of Solid-State Circuits, vol.47, no.12, pp.3120–3129, Dec. 2012.
[32] J. Lu, H. Song, and R. Gharpurey, "A CMOS Class-D Line Driver Employing a Phase-Locked Loop Based PWM Generator," IEEE Journal of Solid-State Circuits, vol.49, no.3, pp.729–739, March 2014.
[33] S.J. Kim, Q. Khan, M. Talegaonkar, A. Elshazly, A. Rao, N. Griesert, G. Winter, W. McIntyre, and P.K. Hanumolu, "High Frequency Buck Converter Design Using Time-Based Control Techniques," IEEE Journal of Solid-State Circuits, vol.50, no.4, pp.990–1001, April 2015.
[34] T. Anand, K.A.A. Makinwa, and P.K. Hanumolu, "A VCO Based Highly Digital Temperature Sensor With 0.034 °C/mV Supply Sensitivity," IEEE Journal of Solid-State Circuits, vol.51, no.11, pp.2651–2663, Nov. 2016.
[35] P. Prabha, S.J. Kim, K. Reddy, S. Rao, N. Griesert, A. Rao, G. Winter, and P.K. Hanumolu, "A Highly Digital VCO-Based ADC Architecture for Current Sensing Applications," IEEE Journal of Solid-State Circuits, vol.50, no.8, pp.1785–1795, Aug. 2015.
[36] A. Sanyal and N. Sun, "An Energy-Efficient Hybrid SAR-VCO ΔΣ Capacitance-to-Digital Converter in 40-nm CMOS," IEEE Journal of Solid-State Circuits, vol.52, no.7, pp.1966–1976, July 2017.
[37] X. Tang, S. Li, L. Shen, W. Zhao, X. Yang, R. Williams, J. Liu, Z. Tan, N. Hall, and N. Sun, "A 16fJ/conversion-step Time-Domain Incremental Zoom Capacitance-to-Digital Converter," IEEE International Solid-State Circuits Conference, pp.296–297, 2019, to appear.
[38] W. Jiang, V. Hokhikyan, H. Chandrakumar, V. Karkare, and D. Markovic, "A ±50-mV Linear-Input-Range VCO-Based Neural-Recording Front-End With Digital Nonlinearity Correction," IEEE Journal of Solid-State Circuits, vol.52, no.1, pp.173–184, Jan. 2017.
[39] C.-C. Tu, Y.-K. Wang, and T.-H. Lin, "A Low-Noise Area-Efficient Chopped VCO-Based CTDSM for Sensor Applications in 40-nm CMOS," IEEE Journal of Solid-State Circuits, vol.52, no.10, pp.2523–2532, Oct. 2017.
[40] C.-C. Tu, Y.-K. Wang, and T.-H. Lin, "A 0.06mm^2 ±50mV range -82dB THD chopper VCO-based sensor readout circuit in 40nm CMOS," IEEE Symposium on VLSI Circuits, pp.C84–C85, June 2017.

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