# A Second-Order Purely VCO-Based CT ΔΣ ADC Using a Modified DPLL in 40-nm CMOS

Yi Zhong[1,2], Shaolan Li[1], Arindam Sanyal[3], Xiyuan Tang[1], Linxiao Shen[1], Siliang Wu[2] and Nan Sun[1]
[1]The University of Texas at Austin, Austin, TX, USA, [2]Beijing Institute of Tech., Beijing, China, [3]The State University of New York at Buffalo, Buffalo, NY, USA.
Email: zhongyi@utexas.edu, slliandy@utexas.edu, nansun@mail.utexas.edu

***Abstract*—This paper presents a power-efficient purely VCO-based 2nd-order CT ΔΣ ADC featuring a modified DPLL structure. It combines a VCO with an SRO-based TDC, which enables 2nd-order noise shaping without any OTA. The nonlinearity of the front-end VCO is mitigated by putting it inside a closed loop. A multi-PFD scheme reduces the VCO center frequency and power. The proposed architecture also realizes an intrinsic tri-level DWA. A prototype ADC in 40-nm CMOS process achieves a Schreier FoM of 170.3 dB with a DR of 72.7 dB over 5.2-MHz BW, while consuming 0.91 mW under 1.1-V supply.**

## I. Introduction

OTAs are widely used to build integrators in classic ΔΣ ADCs. However, technology scaling makes them difficult to design under low power supply and small transistor intrinsic gain. VCO-based integrators, which are simple, power-efficient, and highly digital, are promising candidates to replace power-hungry active RC integrators in advanced processes. Most existing purely VCO-based ΔΣ ADCs are limited to only 1st-order noise shaping [1]. Therefore, it presents a need to realize high-order VCO-based ΔΣ ADC. Ref. [2], [3] combines the VCO with classic OTA-based integrators to achieve high-order shaping, but they sacrifice the scaling friendliness and the power efficiency due to the use of OTA. The work in [4] demonstrated a low-power passive RC and VCO hybrid. It however renders only 1st-order in-band noise suppression, and thus, has a higher in-band noise floor compared to classic 2nd-order ΔΣ ADCs. A 3rd-order purely VCO-based ADC reported in [5] leverages up-down counters to cascade multiple VCOs. Nevertheless, it suffers from VCO nonlinearity as the first VCO integrator operates in open loop and experiences the full signal swing, thereby requiring nonlinearity calibration.

This paper presents an OTA-free 2nd-order purely VCO-based CT ΔΣ ADC featuring a modified digital phase-locked loop (DPLL) structure. It is inspired by the fact that a DPLL intrinsically exhibits not only the mechanism of ΔΣ modulation, but also a purely time-domain oriented structure. The proposed ADC employs two VCOs, one serving as a phase-domain translator and the other as a switched ring oscillator (SRO)-based time-digital converter (TDC), *to realize true 2nd-order noise shaping by using logic gates and simple analog components.* The outputs of the TDC readily facilitate a tri-level DAC control pattern and maintain an *intrinsic* data-weighted averaging (DWA) capability, removing the need for an explicit DEM block. Compared to existing OTA-free VCO-based ADC, this work is able to not only extend the scaling-friendly merits to high-order, but also maintains both high linearity and 2nd-order in-band noise shaping performance simultaneously without needing calibration.

## II. Proposed 2nd-Order Purely VCO-Based ΔΣ ADC

The key concept of the proposed ADC is to leverage the loop mechanism of a DPLL [6], [7], that the control voltage will be enforced to cancel any phase perturbation in the system. As graphically represented in Fig. 1, under this idea, the input ($V_{in}$) is inserted as an intentional perturbation to the VCO, which triggers the phase variation. The phase difference is detected by the phase/frequency detector (PFD), which is assumed to have a reference phase of 0, and subsequently digitized by the TDC. Since the control voltage tracks the perturbation and is mapped directly to the TDC code, the TDC output ($D_{out}$) therefore can readily serve as a digital representation of the input signal. In this work, the TDC is designed to provide one extra order of noise shaping through using a reset-less SRO followed by a digital differentiator. Based on impulse-invariance transform [8], the noise transfer function (NTF) of the system is expressed as:

$$NTF = \frac{2\cdot(1-z^{-1})^2}{2+(k_{v1}k_{v2}\alpha G{T_s}^2-2)\cdot z^{-1}+k_{v1}k_{v2}\alpha G{T_s}^2\cdot z^{-2}} \quad (1)$$

where $k_{v1}$ and $k_{v2}$ are the gain of VCO and SRO respectively, $\alpha$ is the gain of PFD, $G$ is the DAC gain, and $T_s$ is the sampling period. Based on (1), as $G$ increases, the NTF poles move out of the unit circle. For a fixed $G$, increasing $k_{v1}$ and $k_{v2}$ also leads to instability of the ADC. Therefore, $k_{v1}$, $k_{v2}$ and $G$ should be carefully chosen to ensure stable operation. Equation (1) also indicates the in-band quantization error is 2nd-order shaped. The proposed ADC has lower in-band quantization error than the technique of [4] which only has 1st-order noise shaping at low frequency. Compared to [5], the proposed ADC has feedback at the back-end stage which makes the signal swing at the first VCO integrator input very small, and thus, it is immune to VCO nonlinearity.

The schematic of the proposed 2nd-order purely VCO-based CT ΔΣ ADC is presented in Fig. 2. The input currents are injected into two differential current controlled oscillators (CCOs) whose phase difference is quantized by PFD. The two CCOs serve as reference to each other, which removes the need for an externally derived reference in the PFD. Note that if a single PFD is used as in a classic PLL, the CCO's free running frequency would have to be higher than the sampling frequency as the phase information needs at least one rising edge within each sampling period to update, leading to high power penalty. By contrast, the proposed work utilizes 6 PFDs to speed up the phase information update, and thus, relaxes the CCO free-running frequency requirement. Despite using multi-PFD introduces both V/I mismatch error and SRO non-linearity in the back-end stage, these non-idealities are strongly attenuated by the front-end CCO-based integrator when input referred. Based on the post-layout simulation result, compared with the single

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PFD scheme, the power consumption of the first stage CCOs drops from 616 μW to 210 μW with a power penalty of only 61uW for 5 extra PFDs. Although the discrete nature of the CCO and PFD incurs a quantization behavior at the first stage output, the absence of sampling allows the artifact energy to concentrate at high frequencies. It brings negligible impact on the in-band noise as the back-end TDC filters it before sampling [9].

The back-end stage consists of a pair of pseudo-differential SRO-based TDC with 15 quantization levels. This structure provides immunity to even-order non-linearity. However, the asymmetry between PFDs' "UP" and "DN" pulses would introduce common mode modulation if applied to the SROs separately, causing harmonic leakage. This work addresses this concern by cross feeding "UP" and "DN" to ensure the TDC inputs are fully differential. By using the XOR-based differentiator, the TDC provides an intrinsic data-weighted averaging (DWA) behavior [2]. A tri-level DAC control can be derived easily through the tri-level generator in Fig 2. Fig. 3(a) intuitively illustrates an example that tri-level DAC is split into 2 DWA pattern outputs. The behavioral simulation spectrum in Fig. 3(b) proves that this tri-level DAC retains the intrinsic DWA mechanism as 1st-order element mismatch shaping.

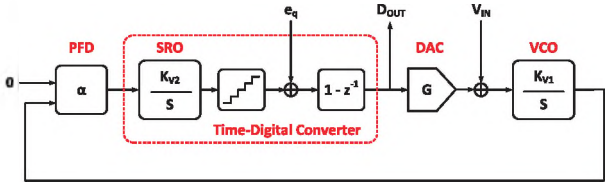


Fig. 1. Architecture of proposed purely VCO-based 2nd-order ΔΣ ADC.

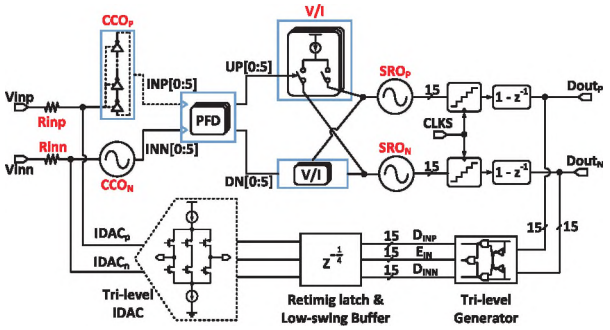


Fig. 2. Schematic of proposed purely VCO-based 2nd-order ΔΣ ADC.

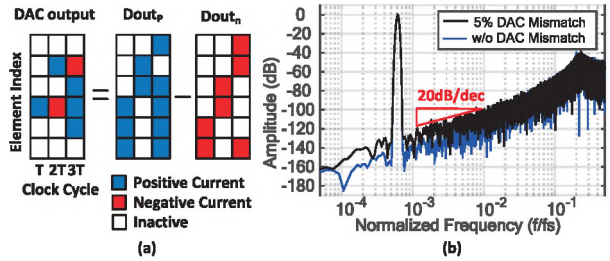


Fig. 3. (a) Tri-level generator element selection pattern example and (b) behavioral simulation results showing 1st-order mismatch error shaping.

## III. Measurement Results

The proposed 2nd-order VCO-based CT ΔΣ ADC occupies an area of 0.086 mm² in 40-nm CMOS process. Die photo is shown in Fig. 4(a). It operates at 260MS/s under 1.1-V supply and consumes 906 μW in total, where 376 μW for digital logics, 368 μW for two VCO-based integrators and 162 μW for DAC. The measured SNDR and SNR across input amplitude is shown in Fig. 4(b). This work achieves a DR of 72.7 dB and Schreier FoM of 170.3 dB with the full scale of 1.0 $V_{p-p}$ (equivalently 500 $\mu A_{p-p}$) in 5.2-MHz BW. The measured output PSD shown in Fig. 4(c) proves 2nd-order noise shaping. At 5.2-MHz BW, the ADC achieves SNDR and SNR of 69.6 dB, 72.1 dB, respectively. As shown in Table I, the proposed ADC demonstrates in-line performance to other state-of-the-art high-order VCO-based ΔΣ ADCs. To the best knowledge of the authors, this work is the first to demonstrate a calibration-free high-order purely VCO-based CT ΔΣ ADC with chip measurement results.

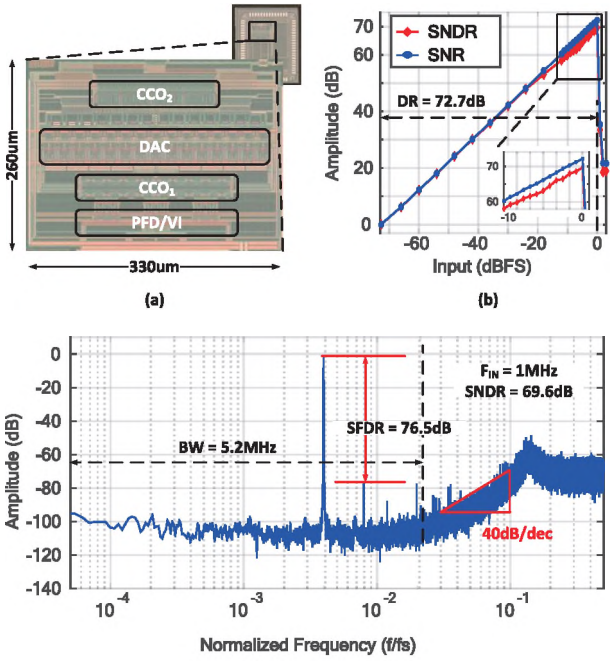


Fig. 4. (a) Die photo. (b) SNDR/SNR vs input amplitude. (c) Measured ADC output spectrum.

TABLE I. Performance Comparision

| | This work | [3] | [4] | [5] | [10] |
|---|---|---|---|---|---|
| Loop order | **2nd** | 4th | 2nd | 3rd | 3rd |
| Purely VCO | √ | × | × | √ | × |
| OTA-free | √ | × | √ | √ | × |
| Calibration-free | √ | √ | √ | × | √ |
| Process(nm) | **40** | 65 | 40 | 65 | 65 |
| Fs(MS/s) | **260** | 1200 | 330 | 1600 | 1280 |
| Power (mW) | **0.91** | 54 | 0.524 | 3.7 | 38 |
| BW (MHz) | **5.2** | 50 | 6 | 10 | 50 |
| SNDR (dB) | **69.6** | 71.5 | 68.6 | 65.7 | 64 |
| DR (dB) | **72.7** | 72 | 70.8 | 71 | 75 |
| FoM_s* (dB) | **170.3** | 161.7 | 171.4 | 165.3 | 166.2 |

* *FoM_s = DR + 10*log10 (BW/Power)*

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