Ring Oscillator Based Delta-Sigma ADCs

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***Abstract*—In this work, we will review recent advances in VCO based low power ADCs as well as present a summary of our recent and on-going works. We will present a 18.5fJ/step discrete-time VCO-based 0-1 MASH ADC as well as a continuous-time, third-order purely VCO-based ADC architecture. We will also present applications of our ADCs for sensing, such as capacitance-to-digital conversion and current-to-digital conversion.**

***Index Terms*—time-domain ADC, voltage-controlled oscillator, noise shaping, $\Delta\Sigma$ ADC**

I. Introduction

$\Delta\Sigma$ ADCs are widely used for applications requiring high resolution. As CMOS technology scales, design of conventional $\Delta\Sigma$ modulators using operational amplifiers become energy inefficient due to reduction in transistor intrinsic gain and supply voltage. In recent years, ring voltage-controlled oscillator (VCO) based ADCs have emerged as prime contender for $\Delta\Sigma$ design in advanced CMOS technologies. A VCO acts as an ideal integrator in phase domain and can be easily constructed using a chain of inverters. In addition, VCO phase can be easily quantized by sampling the output of each inverter in the chain with an edge-triggered flip-flop. Thus, VCO-ADC has a highly digital nature and can work from low supply voltages. Quantization noise in VCO reduces naturally with technology scaling which provides an added incentive to use VCOs as building blocks of high-precision $\Delta\Sigma$ ADCs. Fig. 1 compares state-of-the-art VCO-ADCs with conventional $\Delta\Sigma$ ADCs. Energy-efficiency of different ADCs is compared using the well known Walden figure-of-merit (FoM) given by $\text{FoM}_\text{w} = \text{Power}/\left(2^{\text{ENOB}} \times 2 \times \text{BW}\right)$ where ENOB is the effective number of bits of the ADC and BW is the nyquist bandwidth of the ADC. Fig. 1 shows that state-of-the-art VCO-ADCs can achieve better energy-efficiency than conventional $\Delta\Sigma$ ADCs.

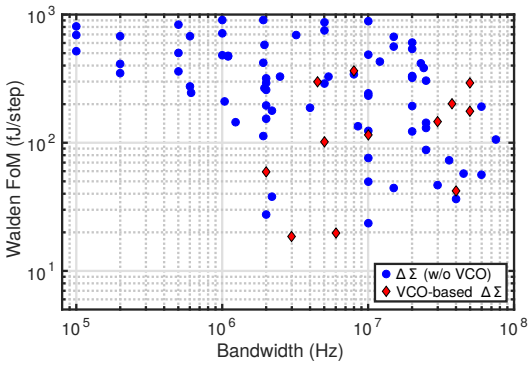

Fig. 1. Comparison of VCO-ADC with conventional $\Delta\Sigma$ ADC

Despite the many advantages of VCO-ADCs, VCO is nonlinear and its gain is highly sensitive to variations in process, voltage and temperature (PVT). There have been many attempts to address VCO nonlinearity and PVT sensitivity with the main techniques being to embed the VCO inside a loop with high linear gain, calibration for nonlinearity and PVT sensitivity and using the VCO as the back-end for a two-stage architecture. In this paper, we will provide a brief survey of existing VCO-ADCs. We will also present our contributions towards VCO-based $\Delta\Sigma$ ADCs. This paper is organized as follows: Section II presents a brief review of state-of-the-art VCO ADCs, Section III presents our previous work on a SAR+VCO architecture, Section IV presents our current work on a continuous-time, higher-order VCO ADC, Section V presents a brief discussion on application of VCO architectures for capacitance and current sensing applications, and Section VI brings up the conclusion.

II. Review of VCO-ADCs

There have been many excellent VCO-ADCs developed over the years. The classic VCO-ADC architecture embeds the VCO quantizer in a loop with opamp integrators [1]. The loop suppresses VCO nonlinearity and PVT sensitivity at the cost of power hungry opamps. [2] presents an all-digital VCO-ADC in which calibration is used to suppress VCO nonlinearity. A pseudo-random sequence is injected into a replica VCO through a DAC and correlated at the output to extract coefficients of nonlinearities in the VCO transfer function. [3] calculates the inverse of the VCO transfer function and adds the inverse function to the signal path to cancel VCO nonlinearity. However, accuracy of nonlinearity suppression for both [2], [3] depends on accuracy of replica matching. [4] presents a current feedback technique which linearizes delay cell in ring oscillator by reducing short circuit current. A two-stage architecture is presented in [5] that uses a coarse flash ADC and sends the residue to VCO quantizer to suppress nonlinearity. The two-stage ADC is embedded inside a high-gain loop to reduce PVT sensitivity and interstage gain mismatch without requiring calibration. Open-loop two-stage architectures do away with opamp based loop filter. [6] uses a 2-bit flash as coarse quantizer and a VCO as fine quantizer. A filtered dither sequence is fed to the input to randomize the signal swing seen by the VCO. A digital background calibration is used to suppress interstage gain variation. [7] presents a 12-b flash+VCO ADC. A 14-level flash ADC is used as coarse quantizer with a VCO as fine quantizer. Digital background calibration is used to suppress interstage gain

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mismatch as well as VCO nonlinearity. A purely VCO-ADC is presented in [8] which achieves first-order noise shaping and inherent static and dynamic error shaping in the multi-element digital-to-analog converter (DAC). The work in [9] improves upon the design of [8] by extending the phase detection range and using a tri-level DAC to achieve high energy-efficiency. Higher-order quantization noise shaping has been achieved by using a passive integrator [10] in front of the dual-VCO design of [9] or using $\Delta\Sigma$ architectures with VCOs acting as phase domain integrators and quantizers. [11], [12] uses an open-loop VCO followed by a second-order $\Delta\Sigma$ loop, while [13] uses two stage architecture with VCOs as both coarse and fine quantizers. While [11] uses special design techniques to linearize the open-loop VCO, in general, use of open-loop VCO as the first integrator/quantizer makes the ADC susceptible to PVT sensitivity and reduces signal handling capability.

III. Discrete-time 0-1 MASH ADC

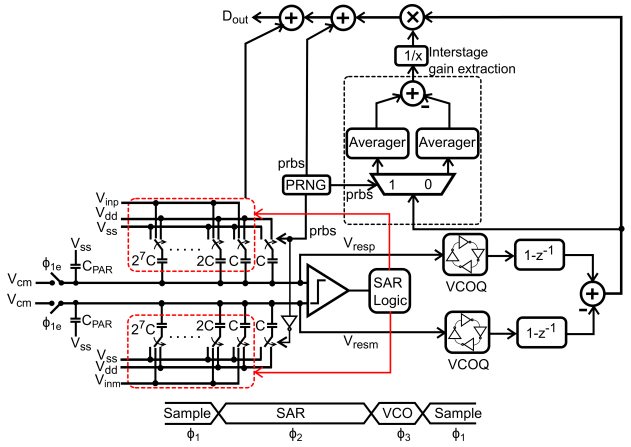
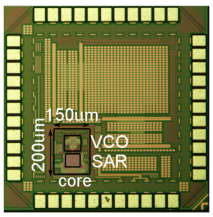


Fig. 2. SAR+VCO 0-1 MASH DT $\Delta\Sigma$ ADC



Process (nm)	40
Area (mm²)	0.03
Fs (MHz)	36
Power (mW)	0.35
BW (MHz)	3
SNDR (dB)	71.4
Walden FoM(fJ/step)	18.5
Schreier FoM(dB)	171

Fig. 3. Die photo and performance summary of SAR+VCO ADC

A two-stage SAR+VCO DT ADC [14] is shown in Fig. 2. Analog input is sampled during the phase ϕ_1 on the capacitive digital-to-analog converter (DAC) of the SAR stage. The SAR performs an 8-bit quantization of the sampled input during the phase ϕ_2. After SAR quantization is over, the residue is available at the comparator input and is fed back to the second-stage VCO. SAR+VCO architecture combines the advantages of both SAR and VCO. SAR has very high energy-efficiency at medium resolutions (6 $\sim$ 10 bits) and is very good at quantizing rail-to-rail signal swings. On the other hand, VCO is very good at performing fine quantization of small signals. The VCO sees the small swing SAR residue and does not require any nonlinearity calibration. In addition, the VCO stage absorbs decision errors in the SAR stage as long as the errors do not overload the VCO, and thus allows a low power comparator in the SAR stage. The VCO phase output is digitally differentiated and added with the digital outputs from the SAR stage. The noise from the SAR stage (quantization noise + comparator thermal noise) are canceled at the output and the ADC noise is dominated by the VCO thermal noise and first-order shaped quantization noise as long as both SAR and VCO stages are sufficiently linear.

Since the VCO gain varies with PVT, first stage noise can leak into the ADC output as the interstage gain changes with variations in PVT. A simple digital calibration technique is used to correct interstage gain variation. A pseudo-random sequence, *prbs*, is generated using linear-feedback-shift register (LFSR) and fed to the capacitive DAC using an additional LSB capacitor. The interstage gain can be extracted by correlating the injected pseudo-random sequence with the second-stage output. Interstage gain variation with PVT can be corrected by running the correlation in background. The background calibration has a very fast convergence [14] since the first-stage has 8-bit resolution.

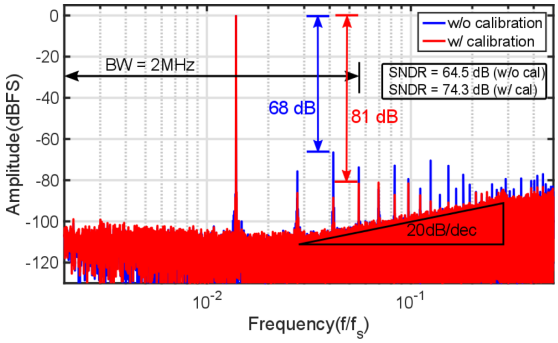


Fig. 4. Measured spectra of SAR+VCO ADC

A prototype ADC was fabricated in a 40nm CMOS process. The chip photograph and performance summary are shown in Fig. 3. The core circuit occupies an area of only 0.03mm^2. The prototype consumes a power of 350μW from a 1.1V supply while running at a sampling frequency of 36MHz. Out of 350μW, SAR comparator consumes 40μW, the DAC switching power is 10μW and the VCO consumes 50μW. The remaining 250μW is consumed by digital logic in SAR and VCO stages and clock generator. The SAR DAC has a low switching power thanks to the bi-directional single-sided switching technique [15] used in this work. The ADC achieves an SNDR of 71.4dB at an oversampling ratio (OSR) of 6 leading to Walden FoM of 21.3fJ/step and Schreier FoM of 171dB. Schreier FoM is defined as FoM = SNDR + $10\log_{10}$(Bandwidth/Power). Fig. 4 shows the measured ADC spectrum without and with background calibration. A 2.2V peak-to-peak input signal at 0.5MHz frequency was used. The ADC output spectrum clearly shows first-order noise shaping. At an oversampling ratio (OSR) of 9, the ADC has an SNDR

of 64.5dB without calibration. The ADC SNDR is primarily limited by distortion tones arising out of SAR quantization noise leaking into the ADC output. Background calibration suppresses quantization noise leakage and improves the SNDR to 74.3dB. The SFDR is also improved to >80dB with background calibration. The remaining distortion tones are due to capacitance mismatch in the SAR DAC. The SAR+VCO architecture presents a highly digital technique for quantization of analog signals and the ADC power will naturally reduce as CMOS technology advances.

IV. Continuous-time purely VCO ADC

While the SAR+VCO architecture in Section III achieves very good energy efficiency, the noise-shaping is limited to first-order. We propose a continuous-time purely VCO based single-loop ADC which can shape quantization noise to higher-order. The proposed VCO architecture is shown in Fig. 5. Current-starved ring oscillators are used as phase-domain integrators. The front-end integrator is a current-

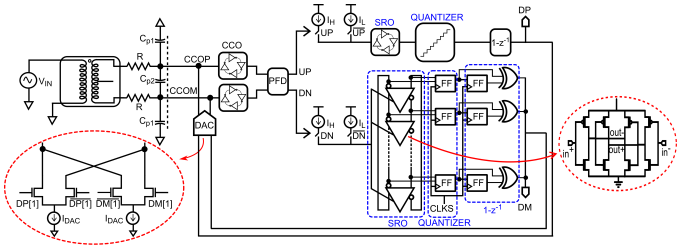


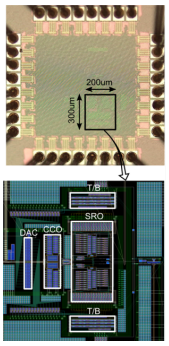
Fig. 5. Proposed third-order CT VCO-ADC

controlled oscillator (CCO). A tri-state phase/frequency detector (PFD) is used to extract the phase difference of the 2 CCOs. The use of differential CCOs and PFD ensures that the CCO phase difference is extracted in a continuous-time fashion. If the CCO phases were sampled using a clock, quantization noise from the CCOs would have dominated the in-band noise and the overall quantization noise shaping would only be of the first order.

The PFD outputs are used as 1-bit DAC to modulate the current to another pair of ring oscillators which act as the second integrator. Since the ring oscillators switch between 2 currents, I_H and I_L, they are denoted as switched ring oscillators (SROs) in Fig. 5. The SROs have very high linearity as they oscillate at only 2 frequencies. The SRO phase outputs are quantized and digitally differentiated before being fed back through current steering non-return-to-zero (NRZ) DACs. The barrel-shifting element selection pattern associated with digital differentiation using XOR gates results in intrinsic first-order high-pass shaping of static element mismatch in the DAC. A passive integrator comprising of off-chip resistor R and capacitances C_{p1} and C_{p2} results in third-order quantization noise shaping. The feedback loop ensures that the current swing seen by the CCO is much smaller than the input swing and thus, CCO nonlinearity is suppressed without calibration.

The ADC loop gain is chosen carefully to prevent instability. ADC instability may arise due to excess loop delay (ELD) which increases the modulator order, or due to saturation in the two integrators. The proposed architecture can tolerate ELD of upto a full sampling period by tuning of the CCO and SRO gains [16]. SRO saturation or phase overflow can be prevented by ensuring $(I_H - I_L)k_{sro}T_s \leq 0.5$ where k_{sro} is the SRO gain and T_s is the ADC sampling period. The CCO input swing is primarily dominated by out-of-band quantization noise and the quantization step is selected to ensure that the CCO phase does not overflow.

A prototype ADC is fabricated in 65nm CMOS process and the die microphotograph and performance summary are shown in Fig. 6. The active core occupies an area of 0.06mm^2. The test chip consumes 1mW power operating from 1.2V supply at a sampling frequency of 205MHz. The quantizer outputs are converted from thermometer to binary code before being brought out of the chip. Measurement on the prototype has indicated that a large portion of the ADC power is due to the static current in the DAC which in turn increases the CCO power. The ADC test chip achieves an SNDR of 57dB and a Schreier FoM of 151dB. Fig. 7 shows the ADC output spectrum for an input of $70\mu\text{A}_{pk-pk}$ at a frequency of 300KHz. The spectrum shows a third-order noise shaping due to the front-end passive integrator. The ADC shows distortion tones due to mismatch and nonlinearity of the off-chip discrete resistors (R) which are used to convert the input voltage to current. The mismatch in the resistors biased the two CCOs at different center frequencies leading to inadequate suppression of even-order harmonic distortion tone. In addition to distortion tones, the mismatch between the resistors also reduced the ADC dynamic range. The ADC SNDR is 57dB over a bandwidth of 2.5MHz. While the ADC testchip demonstrates the effectiveness of the proposed CT VCO-ADC architecture, the energy efficiency can be significantly improved by small modifications in the CCO and DAC architectures which will be undertaken in future.



Process (nm)	65
Area (mm²)	0.06
Fs (MHz)	205
Power (mW)	1
BW (MHz)	2.5
SNDR (dB)	57
Schreier FoM(dB)	151

Fig. 6. Die photo and performance summary for CT VCO-ADC

V. Application of VCO ADCs

In addition to ADCs, the SAR+VCO and the CT VCO-ADC architectures presented in Sections III and IV can also be used for sensing applications. The SAR+VCO architecture is used as a capacitance-to-digital converter (CDC) [17] with minor modifications. Instead of differential SAR, a single-ended SAR is used and the sensing capacitance is added in parallel to the SAR capacitive DAC. A prototype CDC in 40nm CMOS is

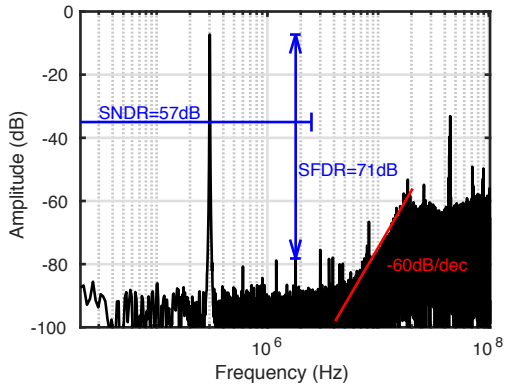
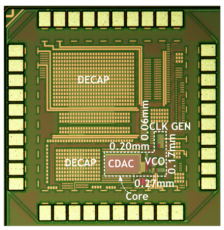


Fig. 7. Measured spectrum for CT VCO-ADC

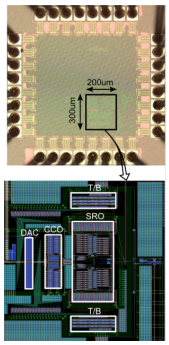
shown in Fig. 8 alongwith measured performance summary. The highly digital SAR+VCO architecture resulted in a CDC with excellent energy efficiency of 55fJ/step which is among the best in literature.



Process (nm)	40
Input range (pF)	0-5
Meas. time (us)	1
Resolution (fF)	1.1
Energy (nJ)	0.075
SNR (dB)	64.2
FoM (fJ/step)	55

Fig. 8. SAR+VCO capacitance-to-digital converter

The CT VCO-ADC architecture is modified for a current-to-digital converter design. The proposed converter digitizes currents in the range of 0.25μA to 96μA in a single-ended manner. The converter requires only 0.5μs for digitization and achieves an energy efficiency of 1.2pJ/step which is almost 10 times better than state-of-the-art current-to-digital converters. A testchip fabricated in 65nm CMOS process is shown in Fig. 9 alongwith the measured performance summary.



Process (nm)	65
Area (mm^2)	0.06
Conv. time	0.5us
Energy	0.43nJ
Range(uA)	0.25-96
DR (dB)	55
FoM(pJ/step)	1.2

Fig. 9. CT-VCO based current-to-digital converter

VI. Conclusion

A brief review of low-power high performance VCO-ADCs is presented in this paper. A SAR+VCO based discrete-time and a third-order continuous-time VCO-ADC are also presented. A capacitance-to-digital converter and a current-to-digital-converter which uses modified VCO-ADC architectures are also presented. It is expected that VCO-ADCs will exhibit natural improvement in energy-efficiency and bandwidth with technology scaling.

VII. Acknowledgment

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