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Highly Digital Second-Order ΔΣ VCO ADC

Akshay Jayaraj, Mohammadhadi Danesh, Sanjeev Tannirkulam Chandrasekaran, and Arindam Sanyal, *Member, IEEE*

***Abstract*— A continuous-time second-order ΔΣ analog-to-digital converter (ADC) is presented in this paper. The proposed ADC is based on a novel architecture and uses current starved ring oscillators as integrators to achieve the second-order noise shaping. The proposed architecture does not require excess loop delay compensation or nonlinearity calibration. Static element mismatch in the multi-bit current digital-to-analog converter is high-pass shaped by intrinsic data-weighted averaging. Detailed analysis and insights on the various trade-offs involved in the design of the proposed ADC are presented in this paper. A prototype ADC is implemented in 65-nm CMOS and achieves 64.2-dB SNDR at a bandwidth of 2.5 MHz and a Schreier FoM of 158.2 dB. The ADC operates at 205 MHz and consumes 1 mW of power. The measured power supply rejection ratio is 56.2 dB.**

***Index Terms*— Voltage controlled oscillator (VCO), analog-to-digital converter, noise shaping, continuous-time ΔΣ.**

I. Introduction

VOLTAGE-CONTROLLED oscillator (VCO) based ADCs have attracted a lot of attention from the research community over the last decade. This is because ring VCOs can potentially replace conventional operational amplifier based integrators which are challenging to design in scaled CMOS technology nodes. In addition to being highly digital, ring VCOs come with inherent multi-bit quantization. VCO output can be quantized by sampling the phase of each inverter stage with edge-triggered flip-flops. VCO quantization noise depends on gate delay which scales down with technology, thus providing additional incentive to using VCOs as ΔΣ ADCs. Despite all these advantages, VCOs are highly nonlinear and sensitive to variations in process, voltage, and temperature (PVT).

There have been many excellent techniques which attempt to address nonlinearity and PVT sensitivity of VCO-ADCs. The classic VCO-ADC architecture embeds the VCO quantizer in a loop with opamp integrators [1]. The loop suppresses VCO nonlinearity and PVT sensitivity at the cost of power hungry opamps. Reference [2] presents an all-digital VCO-ADC in which calibration is used to suppress VCO nonlinearity. A pseudo-random sequence is injected into a replica VCO through a DAC and correlated at the output to extract coefficients of nonlinearities in the VCO transfer function. Reference [3] calculates the inverse of the VCO transfer function and adds the inverse function to the signal path to cancel VCO nonlinearity. However, accuracy of nonlinearity suppression for both [2] and [3] depends on accuracy of replica matching. Reference [4] presents a current feedback technique which linearizes delay cell in ring oscillator by reducing short circuit current. A two-stage architecture is presented in [5] that uses a coarse flash ADC and sends the residue to VCO quantizer to suppress nonlinearity. The two-stage ADC is embedded inside a high-gain loop to reduce PVT sensitivity and interstage gain mismatch without requiring calibration. Open-loop two-stage architectures do away with opamp based loop filter. Reference [6] uses a 2-bit flash as coarse quantizer and a VCO as fine quantizer. A filtered dither sequence is fed to the input to randomize the signal swing seen by the VCO. A digital background calibration is used to suppress interstage gain variation. Reference [7] presents a 12b flash+VCO ADC. A 14-level flash ADC is used as coarse quantizer with a VCO as fine quantizer. [8] presents a 12b SAR+VCO ADC with an 8-b SAR as coarse quantizer. Digital background calibration is used to suppress interstage gain mismatch as well as VCO nonlinearity in both [7] and [8]. A purely VCO-ADC is presented in [9] which achieves first-order noise shaping and inherent static and dynamic error shaping in the multi-element digital-to-analog converter (DAC). The work in [10] improves upon the design of [9] by extending the phase detection range and using a tri-level DAC to achieve high energy-efficiency. Higher-order quantization noise shaping has been achieved by using a passive integrator [11] in front of the dual-VCO design of [10] or using ΔΣ architectures with VCOs acting as phase domain integrators and quantizers. References [12] and [13] use an open-loop VCO followed by a second-order ΔΣ loop, while [14] uses two stage architecture with VCOs as both coarse and fine quantizers. While [12] uses special design techniques to linearize the open-loop VCO, in general, use of open-loop VCO as the first integrator/quantizer makes the ADC susceptible to PVT sensitivity and reduces signal handling capability.

In this work, we propose a second-order, purely VCO-based continuous-time (CT) ADC. The proposed ADC uses two VCOs as integrators to realize second-order quantization noise shaping. The preliminary architecture was presented in [15] and [16] and also used as a time-to-digital converter (TDC) in [17]. In this work, we expand on the work in [15]–[17] and present detailed discussion and insights on designing the

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The authors are with the Electrical Engineering Department, University at Buffalo, Buffalo, NY 14260 USA (e-mail: akshayja@buffalo.edu; mdanesh@buffalo.edu; stannirk@buffalo.edu; arindams@buffalo.edu).

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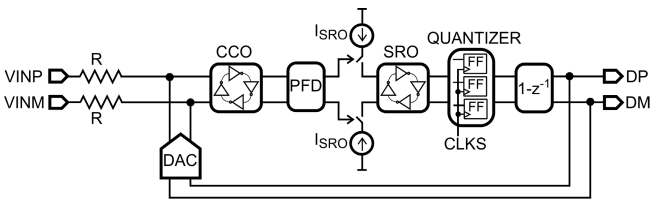

Fig. 1. Architecture of proposed VCO-ADC.

second-order ADC as well as present measurement results on a 65nm CMOS prototype. The rest of this paper is organized as follows: Section II presents the ADC architecture as well as discussion on how to choose the loop parameters and oscillator center frequencies, Section III presents the circuit schematic and noise analysis, Section IV presents measurement results on 65nm prototype and Section V brings up the conclusion.

II. Proposed ADC Architecture

Fig. 1 shows the proposed continuous-time second-order VCO ADC. The ADC uses two differential VCOs as phase-domain integrators. The first integrator is a current-controlled oscillator (CCO) [9]. Output phase of the CCO is extracted using a tri-state phase/frequency detector (PFD). The PFD outputs two 1-bit pulses, UP and DN, which encode the CCO phase information in their pulsewidth. The UP and DN pulses drive two current-controlled oscillators, labeled as SRO in Fig. 1. Since UP and DN pulses are either '1' or '0', the SROs switch between two frequencies, hence, the name switched controlled oscillator or SRO. The phase output of the SROs are sampled, digitally differentiated using XOR gates and fed back to the CCO input through a current steering, non-return-to-zero (NRZ) digital-to-analog converter (DAC). The XOR gates scramble the element selection pattern in the DAC in such a way that static element mismatch in the multi-element DAC is first-order shaped [1]. As will be shown later, the ADC loop parameters are designed to ensure that the ADC can tolerate excess loop delay (ELD) of up to a full sampling period without explicit delay compensation.

A. ADC Model

As shown in Fig. 1, the CCO output is not sampled immediately after the CCO but is sampled down the chain after going through the SRO. To analyze the continuous-time CCO output, we will use the pulse-frequency modulation (PFM) model presented in [18]–[20]. We will briefly present the PFM model, with respect to the CCO, for sake of completeness. Fig. 2 shows the PFM model of differential CCO and the associated signals.

When the CCO is fed an input of $x_i(t), i \in [1,2]$, it outputs a square-wave $v_i(t)$ with rising edges of $v_i(t)$ corresponding to CCO phase crossing of 2π. Thus, the rising edges of CCO output encode all the information that we need from the CCO. Consider an edge-detector ($\delta(t)$ in Fig. 2) that generates Dirac delta impulses at rising edges of $v_i(t)$. The output of the edge-detector is a PFM signal and contains i) a dc term proportional to CCO center frequency, f_{cco}

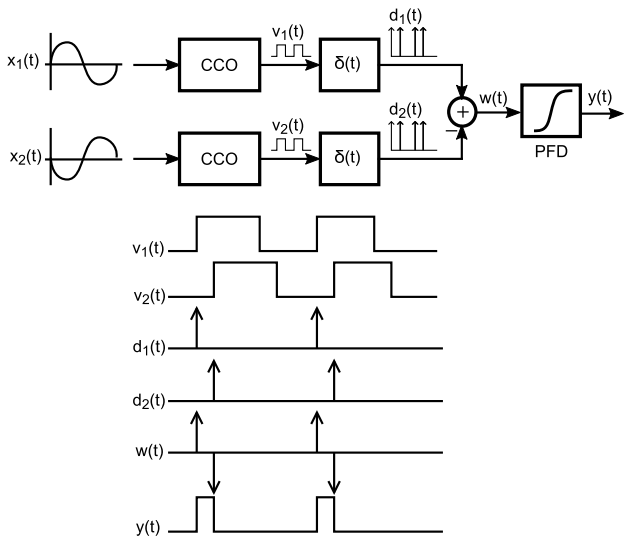

Fig. 2. Pulse-frequency modulation interpretation of CCO.

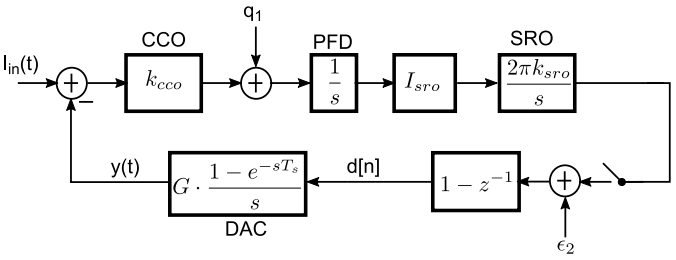

Fig. 3. Block diagram of proposed VCO-ADC.

ii) the input signal multiplied by CCO tuning gain, k_{cco} and iii) distortion terms with modulation side-bands centered around harmonics of f_{cco} [18]–[21]. The PFM signal is integrated by a PFD which gives a pulse-width modulated output. The phase difference between the differential CCO outputs is encoded in the pulse-width of the PFD output.

Fig. 3 shows the block diagram of the proposed ADC. A single-ended model is shown for the sake of simplicity. $I_{in}(t)$ denotes the analog input and $d[n]$ is the sampled ADC output. We have used PFM+integrator model to replace the CCO+PFD combination in the proposed architecture. The PFM distortion in the CCO is denoted by q_1. The SRO output is sampled immediately after, and so we use phase-domain integrator model for the SRO. The SRO tuning gain is denoted by k_{sro}. The PFD output pulse is converted into current through a 1-bit DAC with gain I_{sro}. The NRZ DAC is modeled by a zero-order hold in Fig. 3 with a gain G. Quantization noise of SRO is denoted by ϵ_2 and the ADC sampling period is T_s. The ADC output d can be written as

$$d = [I_{in} \cdot STF(s)]^* + [q_1 \cdot NTF_1(s)]^* + \epsilon_2 \cdot NTF_2(z) \quad (1)$$

where STF is the signal transfer function, NTF_1 is the transfer function from q_1 to ADC output and NTF_2 is the transfer function from ϵ_2 to ADC output. Sampling operation is denoted by $[]^*$. NTF_2 can be calculated by finding the discrete-time equivalent loop-filter [22] and can be shown to

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be

$$NTF_2(z) = \frac{2(1-z^{-1})^2}{2+\left(GHT_s^2-2\right)z^{-1}+(GHT_s^2)z^{-2}} \quad (2)$$

where $H = 2\pi k_{cco} k_{sro} I_{sro}$. It can be seen from (2) that quantization noise from SRO is second-order shaped. The signal transfer function can then be written as

$$\begin{aligned} STF(s) &= \frac{H}{s^2} \cdot NTF_2(e^{sT_s}) \\ &= H_1(s) \cdot \frac{(1-e^{-sT_s})^2}{(sT_s)^2} \end{aligned} \quad (3)$$

where $H_1(s) = \frac{2HT_s^2}{2+(GHT_s^2-2)e^{-sT_s}+(GHT_s^2)e^{-2sT_s}}$. It can be seen from (3) that the input signal is filtered by a second-order sinc function, with nulls at multiples of $1/T_s$ before getting sampled. This second-order sinc-filter results in intrinsic anti-aliasing which is characteristic of CT ΔΣ ADC. Transfer function of PFM distortion, q_1 can be similarly written as

$$NTF_1(s) = \frac{H_1(s)}{k_{cco}} \cdot \frac{(1-e^{-sT_s})^2}{(sT_s)^2} \quad (4)$$

Hence, the PFM distortion tones are second-order sinc-filtered before getting sampled and aliased to signal-band. Since the distortion tones are centered around harmonics of f_{cco}, setting $f_{cco} = f_s$ ($f_s = 1/T_s$) results in maximum suppression of the distortion tones. The modulation side-bands of the PFM tones are second-order shaped by the sinc filter before sampling. Thus, after sampling, the PFM tones appear as second-order shaped in the signal band. In practice, it is hard to maintain f_{cco} to be exactly f_s without using background calibration [23]. Later in the Section, we will discuss the optimal choice of f_{cco} that does not significantly corrupt in-band spectrum.

As is evident from the analysis of the ADC model, not directly sampling the CCO output allows suppression of PFM distortion tones. We will briefly examine the result of directly sampling the CCO output. Since both CCO and SRO outputs are directly sampled in this case, we will use phase-domain integrator model for both CCO and SRO. In addition, we will denote CCO quantization noise by ϵ_1. The block diagram of the ADC with sampling after both CCO and SRO is shown in Fig. 4. Since the CCO output is sampled, we add another NRZ DAC after the PFD. The ADC output can now be written as

$$d = \left[I_{in} \cdot STF'(s)\right]^* + \epsilon_1 \cdot NTF_1'(z) + \epsilon_2 \cdot NTF_2'(z) \quad (5)$$

Converting the continuous-time filters to their discrete-time equivalents [22], NTF_2' can be shown to be

$$NTF_2'(z) = \frac{(1-z^{-1})^2}{1-z^{-1}+(GHT_s^2)z^{-2}} \quad (6)$$

NTF_1' and STF' can be similarly shown to be

$$NTF_1'(z) = \frac{HT_s}{2\pi k_{cco}} \cdot \frac{z^{-1}(1-z^{-1})}{1-z^{-1}+(GHT_s^2)z^{-2}} \quad (7)$$

$$\begin{aligned} STF'(s) &= \frac{2\pi k_{cco}}{s} \cdot NTF_1'(e^{sT_s}) \\ &= \frac{HT_s^2 e^{-sT_s}}{1-e^{-sT_s}+GHT_s^2 e^{-2sT_s}} \cdot \frac{1-e^{-sT_s}}{sT_s} \end{aligned} \quad (8)$$

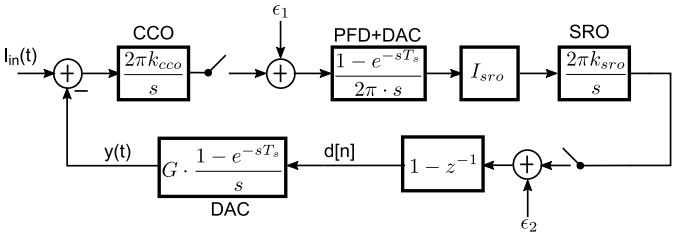

Fig. 4. Block diagram of VCO-ADC with sampling after both CCO and SRO.

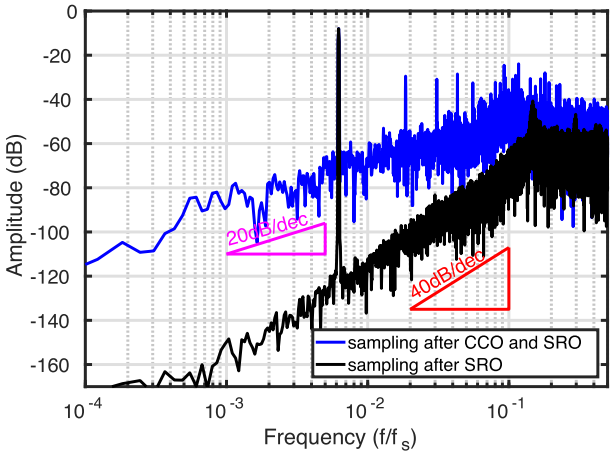

Fig. 5. ADC spectra with and without sampling after CCO.

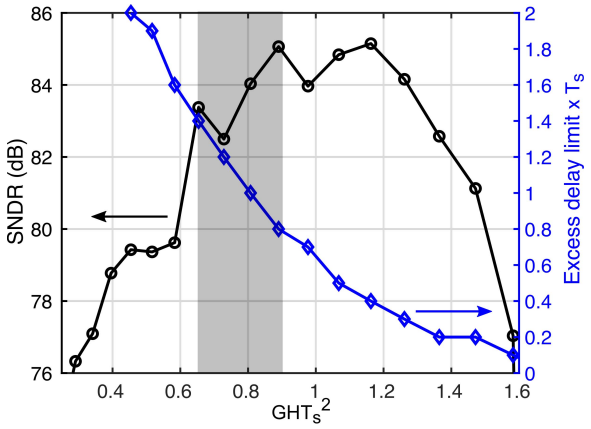

Fig. 6. Excess loop delay and SNDR vs ADC loop parameter.

In contrast to the proposed VCO-ADC, it can be seen from (6-8) that the input signal is filtered by a first-order sinc filter, i.e., sampling after CCO reduces the intrinsic anti-alias filter to first order. In addition, the CCO quantization noise shows up as first-order shaped noise in the in-band and will dominate the second-order shaped SRO quantization noise. Fig. 5 compares the effect of sampling the CCO output with a fixed clock versus the proposed architecture in which the sampler follows the SRO. A sinusoidal current source of frequency 1.23MHz and amplitude of -8dBFS is used as the input. The ADC sampling frequency is set to 200MHz. For this simulation, the CCO and SRO center frequencies are set to 200MHz each. Thermal noise is not considered for

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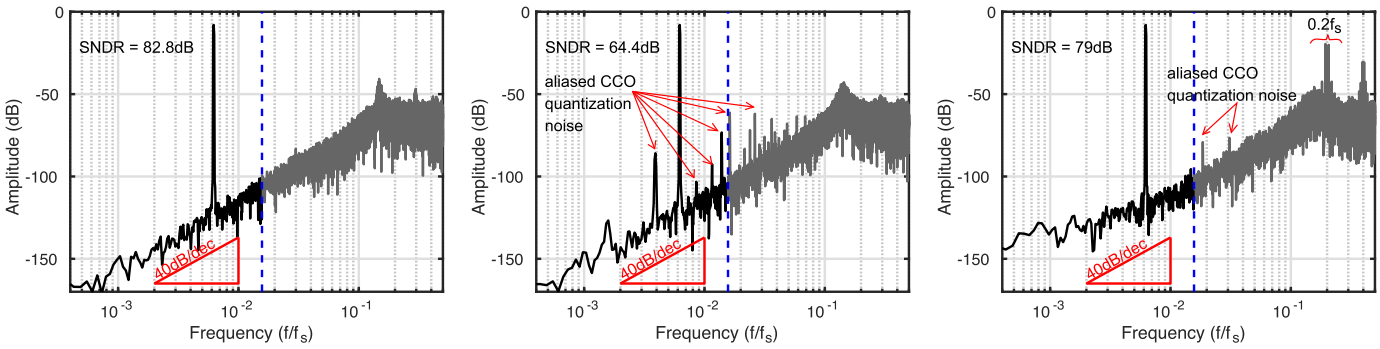

Fig. 7. FFT of the proposed ADC for (a) $f_{cco} = f_s$; (b) $f_{cco} = 1.01\,f_s$; and (c) $f_{cco} = 1.2f_s$.

this simulation. The CCO and SRO tuning gains are set to 2.3MHz/μA. It can be seen from Fig. 5 that the proposed ADC exhibits second-order noise shaping at in-band frequencies and achieves an SNDR of 83dB at an OSR of 40. In contrast, once the CCO output is directly sampled, the CCO quantization noise dominates and the ADC output exhibits only first-order shaped noise and distortion tones. Directly sampling the CCO output reduces the SNDR to 36dB.

B. Excess Loop Delay

As with any continuous-time $\Delta\Sigma$ modulator with NRZ DAC, the proposed ADC is also susceptible to excess loop delay [24]. Assuming that the proposed ADC has an ELD of τ, $NTF_2(z)$ can be written as

$$NTF_2(z) = \frac{2(1-z^{-1})^2}{2+\alpha z^{-1}+\beta z^{-2}+(GHT_s^2\tau^2)z^{-3}} \qquad (9)$$

where $\alpha = \{GHT_s^2(1-\tau)^2 - 2\}$, $\beta = (1+2\tau-2\tau^2)GHT_s^2$ and τ is normalized with respect to T_s. (9) shows that ELD adds an additional pole to the ADC noise transfer function and converts the second-order ADC into a third-order system. Thus, ELD degrades stability of the system.

CT $\Delta\Sigma$ modulators typically use an auxiliary DAC around the quantizer to compensate for ELD. For the proposed architecture, we set the loop parameters such that the ADC can absorb ELD up to a full sampling period without any DAC around the SRO. This is motivated by the fact that adding a DAC around the SRO will force it to oscillate over a span of frequencies rather than only two frequencies, thus degrading its linearity. Fig. 6 plots the SNDR and maximum ELD that the ADC can tolerate without going unstable, as a function of GHT_s^2. We choose GHT_s^2 as the tuning knob because it encompasses parameters from all elements in the ADC. As shown in Fig. 6, the maximum ELD that the ADC can tolerate reduces as GHT_s^2 increases, while the SNDR reduces if GHT_s^2 is outside a certain window. The gray rectangle in Fig. 6 indicates the region where the SNDR is close to the maximum while the ADC can tolerate an ELD in the range of $0.8-1.2$ times the sampling period T_s. For this design, GHT_s^2 is set to 0.8 such that the proposed ADC can tolerate an ELD of one sampling period.

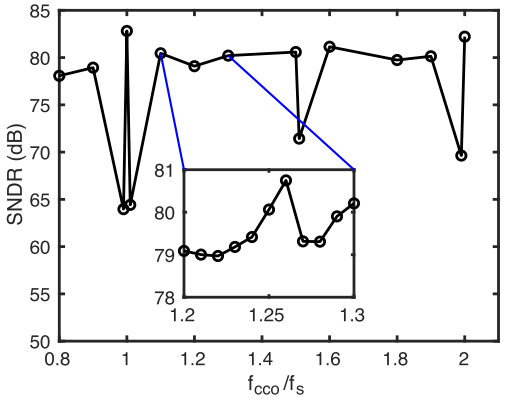

Fig. 8. ADC SNDR vs CCO center frequency.

C. Choice of CCO and SRO Center Frequency

The importance of selecting the proper CCO center frequency, f_{cco}, is evident from the previous analysis. Fig. 7 shows the spectrum of the proposed ADC for three different CCO center frequencies. The SRO center frequency is kept constant at f_s for this simulation. From (4) it can be seen that PFM tones are filtered by second-order sinc function with nulls at multiples of f_s. Hence, setting $f_{cco} = f_s$ maximally suppresses PFM tones before sampling which significantly reduces aliasing of PFM tones into signal band. Fig. 7(a) shows the ADC spectrum for $f_{cco} = f_s$ and it can be seen that quantization noise is second-order shaped in the signal band and there are no visible distortion tone in the signal band, indicating that PFM tones do not degrade ADC performance. However, ensuring $f_{cco} = f_s$ is difficult due to PVT variations. Fig. 7(b) shows the ADC spectrum for $f_{cco} = 1.01\ f_s$. It can be seen that the PFM tones alias into the signal band and reduces SNDR to 64.4dB. If f_{cco} is set to $1.2f_s$, the PFM tones are again not adequately suppressed by the sinc filter, but many of these quantization tones alias out-of-band, unlike $f_{cco} = 1.01f_s$. As can be seen from Fig. 7(c), the in-band noise floor is slightly raised due to aliasing of some PFM tones but the SNDR is still significantly improved to 79dB.

Fig. 8 shows the variation of SNDR as f_{cco} is varied as function of f_s. It can be seen that while $f_{cco} = n \cdot f_s$ ($n = [1, 2, \ldots]$) results in the best SNDR, the SNDR degrades

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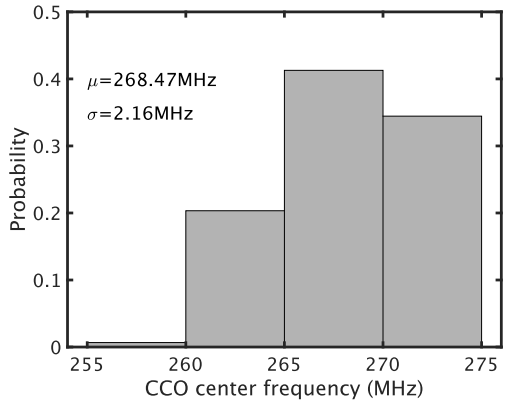

Fig. 9. Histogram of CCO center frequency.

rapidly with small variations in f_{cco} due to aliasing of PFM tones into the signal band. In contrast, setting f_{cco} in the range of $(1.1+k)f_s \leq f_{cco} \leq (1.4+k)f_s, k \in [0, 1, 2, \ldots]$, results in slightly lower SNDR but more stable operating range. Since a lower CCO center frequency results in lower thermal noise, the CCO center frequency is set to $1.25f_s$ in this design. Fig. 9 shows the variation of CCO center frequency versus Monte-Carlo runs across PVT. Standard deviation of the CCO center frequency is less than 1%. Thus, if the CCO center frequency is set to $1.25f_s$, it is expected to remain within the correct operating range.

We define the SRO center frequency f_{sro} as the arithmetic mean of f_H and f_L where f_H and f_L are the high and low frequencies respectively at which the SRO oscillate. f_H and f_L should be set such that the difference $f_H - f_L$ is large for obtaining a high SNDR without resulting in SRO overload. For the ADC to be stable, $(f_H - f_L) < f_s/2$ [1]. The SRO performs modulo integration and the XOR gates perform modulo differentiation. Thus, as long as f_H and f_L satisfy $(k+0.5f_s) < (f_L, f_H) < (k+1.5f_s), k \in [0, 1, 2, \ldots]$, the ADC will be stable [23]. Thus, setting $f_{sro} = (k+1) \cdot f_s$ allows f_H and f_L to be maximally separated which maximizes the output swing. Since the SRO center frequency can change due to PVT variations, we set $(f_H - f_L) = 0.4f_s$, thus allowing the SRO center frequency to vary by ±15% without de-stabilizing the ADC.

D. Effect of Mismatches

Since the proposed ADC architecture uses differential CCOs, mismatch in center frequencies of the two CCOs will affect the performance of the ADC. As has been shown in [19], the pulse-frequency modulated CCO output has a dc term which is proportional to the CCO center frequency. If the differential CCOs have the same center frequency, this dc term is canceled at the output. In presence of mismatch in center frequencies, the dc term does not cancel and shows up at the ADC output. In addition, shift in center frequency of a CCO will result in inadequate filtering and subsequent aliasing of its quantization noise into signal band, thus degrading ADC SNDR. Mismatch in center frequencies for the two CCOs will also result in non-perfect cancellation of even-order harmonics resulting from CCO nonlinearity, but the feedback loop reduces the CCO input swing such that the even-order harmonics arising out of unequal CCO center frequencies do not degrade ADC SNDR significantly [9]. Fig. 10(a) shows the variation of SNDR versus mismatch in CCO center frequencies. The nominal CCO center frequency is set to $1.25f_s$. The errorbar shows the standard deviation of SNDR as CCO mismatch is varied. As is expected, the mean SNDR reduces with mismatch in CCO center frequencies. Fig. 10(b) and (c) shows the ADC spectrum for CCO center frequency mismatch of 1% and 5% respectively. The ADC spectrum is averaged 5 times for each mismatch value. It can be seen from Fig. 10(b) and (c) that ADC SNDR and SFDR reduces as CCO mismatch increases. The aliasing of PFM tones can also be seen in the form of deviation of the ADC in-band noise floor from the ideal second-order shaped noise floor.

Similar to the CCOs, the two SROs can also have mismatch in their center frequencies. If the SROs have different center frequencies, their quantized outputs will exhibit gain mismatch. This is because the SRO with higher center frequency will have more transitions than the SRO with lower center frequency over a sampling cycle. The gain mismatch can be referred back to the SRO input such that the SROs can be considered to be perfectly matched but the PFD has different gains for the UP and DN paths. The PFD performs a linear transformation of the differential CCO phase output ϕ_{cco} such that the time difference between rising edges of the two CCOs is encoded in the width of PFD output pulses. The PFD performs this encoding such that pulse-width of UP is given by $t_{up} = T_s \cdot \max(0, \phi_{cco})/2\pi$ and pulse-width of DN is given by $t_{dn} = -T_s \cdot \min(0, \phi_{cco})/2\pi$. Thus, while $t_{up} - t_{dn}$ is linear, UP and DN pulses encode the positive and negative halves of ϕ_{cco} respectively and are nonlinear. Since ϕ_{cco} contains PFM tones, these tones pass through nonlinearity in UP and DN paths and create additional harmonics, which are canceled at the output as long as the blocks that follow the PFD are linear and matched. However, mismatch in SRO center frequencies create a gain mismatch in the UP and DN paths. Thus, the additional harmonics created by nonlinearity in the UP and DN paths are not adequately suppressed by sinc-filter and show up at the ADC output. However, if the CCO center frequency is ϕ_{cco}, harmonics of ϕ_{cco} created by UP and DN path nonlinearity will still be placed around nulls of sinc filter and will be suppressed. Thus, if the CCO center frequency can be set to exactly f_s, mismatch in SRO center frequencies will not degrade ADC SNDR. Fig. 11(a) shows the SNDR versus mismatch in SRO center frequencies. The errorbar shows the standard deviation of SNDR as SRO mismatch is varied. As is expected, the mean SNDR reduces with mismatch in SRO center frequencies. Fig. 11(b) and (c) shows the ADC spectrum for SRO center frequency mismatch of 1% and 5% respectively. The CCO center frequency is set to $1.25f_s$ for this simulation. The ADC spectrum is averaged 5 times for each mismatch value. It can be seen from Fig. 11(b) and (c) that SRO mismatch results in aliasing of PFM tones which can be seen in the form of deviation of the ADC in-band noise floor from the ideal second-order shaped noise floor. Fig. 12 shows the ADC FFT for SRO center frequency mismatch of 5% but $f_{cco} = f_s$. Compared to Fig. 11(c), the FFT in Fig. 12 does

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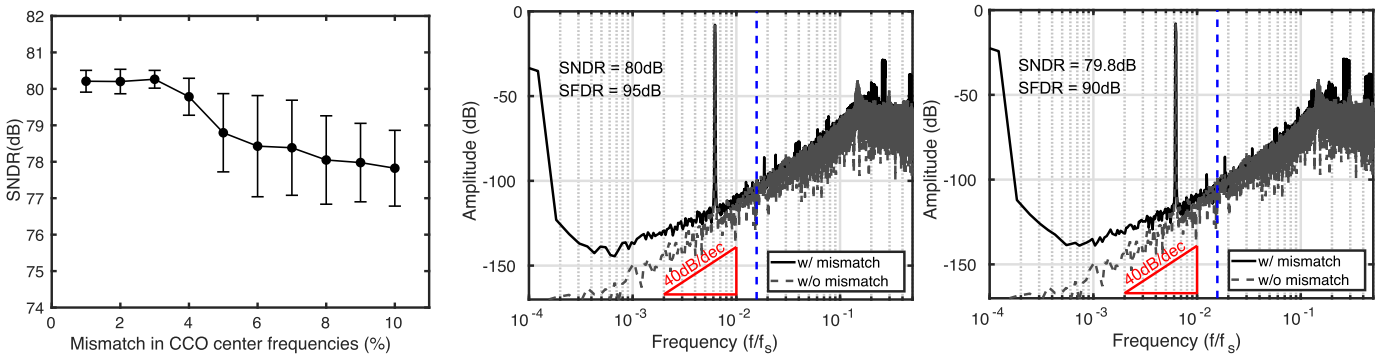

Fig. 10. (a) SNDR vs CCO center frequency mismatch, and FFT of the ADC for CCO center frequency mismatch of (b) 1% and (c) 5%.

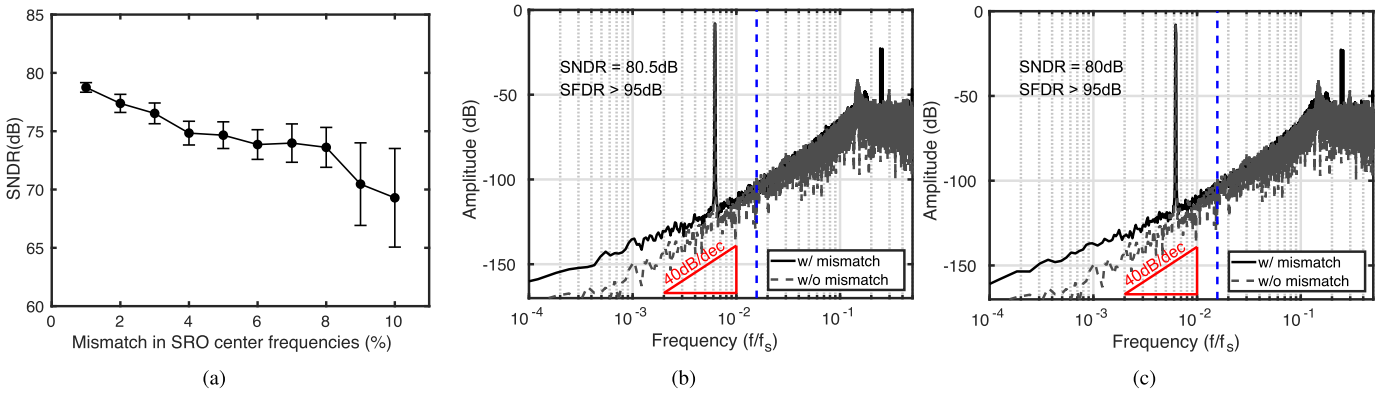

Fig. 11. (a) SNDR vs SRO center frequency mismatch, and FFT of the ADC for SRO center frequency mismatch of (b) 1% and (c) 5%.

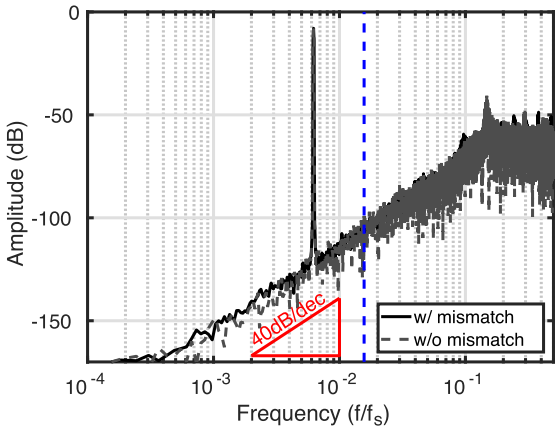

Fig. 12. FFT for SRO center frequency mismatch of 5% and $f_{cco} = f_s$.

not show aliased PFM tones in the signal band and has almost the same performance as the ADC without mismatch. This confirms that the ADC will be immune to mismatch in SRO center frequency if f_{cco} can be set to f_s.

III. ADC Circuit Design

A. Oscillator and DAC Design

Fig. 13 shows the circuit schematic of the proposed ADC. The CCO and SRO are both 17 stage pseudo-differential current-starved inverter based ring oscillators. The CCO center frequency is set to 260MHz while the SRO center frequency is set to 180MHz. Both the CCO and the SRO are designed to have tuning gain of 2.3MHz/μA. A pseudo-differential structure is used for the ring oscillators in both CCO and SRO to improve power supply rejection. PMOS tail current is used to reduce flicker noise. A cascode PMOS tail current source is used for the CCO. Output from one inverter stage of the CCO is used to drive the PFD. The SRO phase output is captured by sense-amplifiers (SA) on positive edges of sampling clock. Current starved buffers are used to isolate the SRO cells from the SAs to reduce kickback noise. At any given time only one of the 17 inverters in each VCO stage is undergoing transition, rising or falling. A rising transition occurs when the positive input of an inverter cell is greater than switching threshold of the buffer and the positive output is less than switching threshold of the buffer. Similarly, a falling transition occurs when the positive input of an inverter cell is less than switching threshold of the buffer and the positive output is greater than switching threshold of the buffer. Since each transition state depends on both rising and falling edges of the inverters, non uniform quantization of phase is avoided which would otherwise lead to significant distortion in the ADC output [23]. The quantized phase is sampled by the sense amplifiers, and then differentiated digitally using XOR gates.

In order to ensure that the CCO is linear, the quantization step needs to be small. We have chosen 17 stages for the SRO

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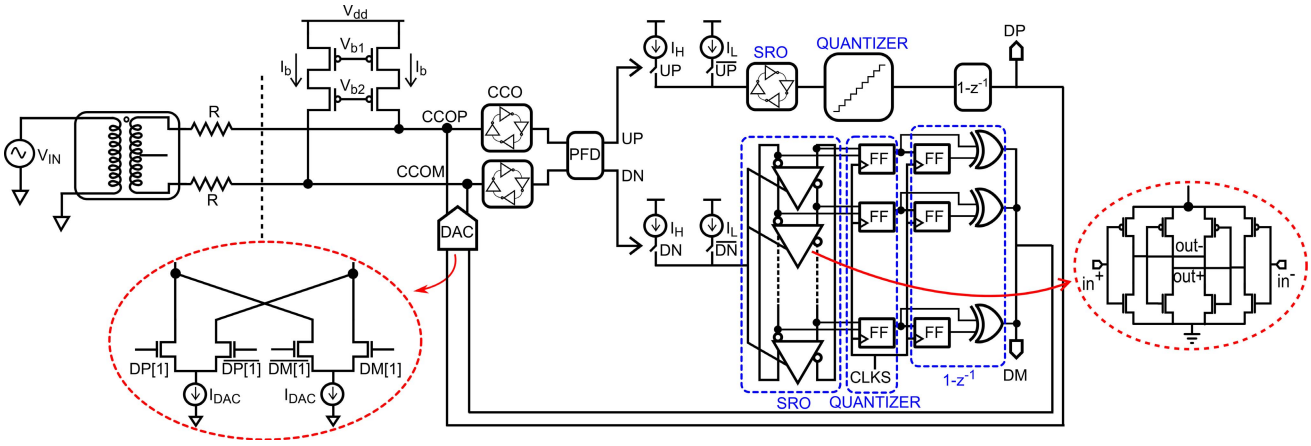

Fig. 13. VCO ADC circuit.

to ensure that the input current swing is large while allowing the quantization step to be small. The quantization step for this design is $2I_{DAC}$ where I_{DAC} is the current through unit DAC slice. Cascode NMOS current sources are used for DAC element. There is a trade-off between CCO linearity and ADC SNR. If the CCO is non-linear, it can result in folding of out-of-band quantization noise into the signal band which will significantly increase ADC noise floor and degrade ADC SNR. For better CCO linearity, I_{DAC} should be small. However, for each 2X reduction in I_{DAC}, ADC SNR reduces by a factor of 3dB. Based on behavioral level simulations, we have chosen $I_{DAC} = 4.5\mu A$ for optimum SNR.

For testing the circuit, sinusoidal voltage input is converted into current through off-chip resistors (R in Fig. 13). In order to reduce signal attenuation at the CCO input, R should be larger than CCO input impedance [9]. R cannot be very large as it will reduce SNR of the ADC. Based on the measured CCO input impedance of 660Ω, we have chosen $R = 1k\Omega$.

B. Noise Analysis

ADC noise is dominated by thermal and flicker noise from the input CCOs, thermal noise from the DAC, and quantization noise from SRO. Thermal noise from the SRO is high-pass shaped and does not dominate the ADC noise. The CCO is biased with PMOS tail current source to reduce flicker noise. Noise from CCO and DAC is calculated by referring the phase noise at the CCO output back to the ADC input. The simulated phase noise plot for CCO+single-ended DAC is shown in Fig. 14. Simulated flicker noise corner of the CCO+DAC combination is close to 100KHz. The input referred noise due to CCO+DAC is given by

$$\sqrt{\overline{i_{th,n}^2}} = \sqrt{2} \cdot \frac{\sqrt{2DT_s}}{2\pi k_{cco} T_s} \cdot \frac{1}{\sqrt{OSR}} \tag{10}$$

where the factor $\sqrt{2}$ takes into account the noise from differential CCO and DAC. The phase diffusion constant [25], D is given by $D = \mathcal{L}(\Delta\omega) \cdot (\Delta\omega)^2/2$ where $\mathcal{L}(\Delta\omega)$ is the phase noise at an offset frequency of $\Delta\omega$. At an offset frequency of 0.43MHz, the phase noise is -94.1dBc/Hz. For k_{cco} of 2.3MHz/μA, sampling frequency of 200MHz and

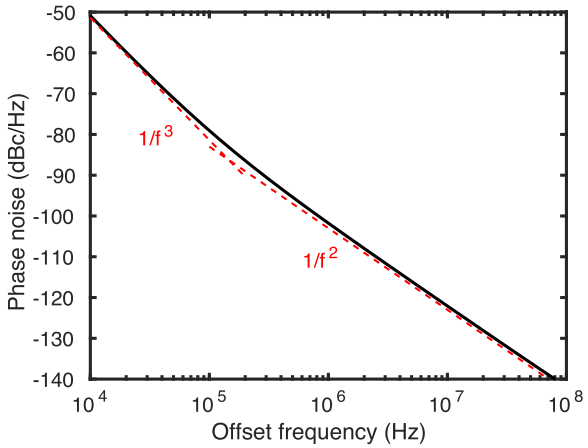

Fig. 14. Simulated CCO+DAC phase noise.

OSR of 40, the input referred CCO+DAC noise is given by 11.8nA,rms with a noise power spectral density of (PSD) of 7.5pA/$\sqrt{Hz}$. Out of the 11.8nA,rms noise current, the DAC contributes 5.1nA,rms with a noise PSD of 3.2pA/$\sqrt{Hz}$ and the PMOS current sources contribute 6.2nA,rms with a noise PSD of 4pA/$\sqrt{Hz}$.

Input referred quantization noise is given by

$$\sqrt{\overline{i_{q,n}^2}} = \frac{2I_{DAC}/N}{\sqrt{12}} \cdot \frac{\pi}{\sqrt{5}} \cdot (OSR)^{-5/2} \tag{11}$$

While calculating the input referred quantization noise, we take into account only the second-order shaped noise from SRO since the PFM tones can be adequately suppressed through proper design, as has been previously shown. The equation for input referred quantization noise is based on the assumption that quantization noise is uniformly distributed. This assumption may not be mathematically accurate but provides an easy way to estimate effect of quantization noise. For OSR of 40 and I_{DAC}/N of 4.5μA, input referred quantization noise is given by 0.36nA,rms. The in-band input referred noise is dominated by noise from CCO and DAC. This is because the proposed architectures high-pass shapes quantization noise to second order even at dc. While the

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TABLE I
INPUT-REFERRED NOISE BREAKDOWN

Source	PSD (pA/$\sqrt{Hz}$)	Percentage
Input resistor	0.9	1.4%
PMOS current source	4	27.9%
NMOS DAC	3.2	17.9%
CCOs	5.5	52.8%
Total	7.58	100%

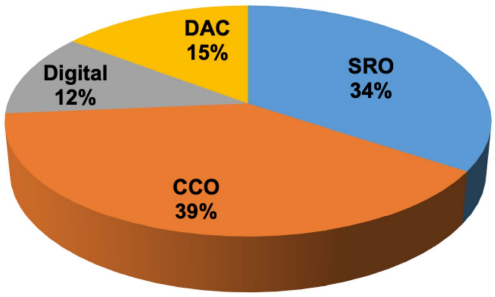

Fig. 15. ADC power breakdown.

in-band quantization noise is 32 times smaller than the ADC thermal noise, if the quantization noise was shaped only to the first-order, the in-band quantization noise would have been 1.6 times larger than ADC thermal noise. The off-chip resistor has a noise PSD of 0.9pA/$\sqrt{Hz}$ and an input-referred noise current of 1.4nA,rms.

SNR for the ADC is given by

$$SNR = 10 \times \log_{10}\left[\frac{I_{in}^2/8}{\overline{i_{th,n}^2} + \overline{i_{q,n}^2} + \overline{i_{R,n}^2}}\right] \quad (12)$$

For an input current of 70μA$_{pk-pk}$, the SNR is calculated to be 66.3dB. Table I shows the summary of input-referred noise from the different contributors. The CCO noise is by far the largest contributor to the ADC noise.

Fig. 15 shows the post-layout simulated power breakdown of the ADC. CCO consumes 39% of the ADC power while SRO consumes 34% of the total power. The DAC consumes 15% of the total power while the digital logic, which includes XOR gates, clock generator logic and thermometer-to-binary converter for bringing ADC output off-chip, consumes 12% of the total power. The power consumed by buffers driving the output pads is not included in this power breakdown.

IV. MEASUREMENT RESULTS

A prototype ADC is fabricated in 65nm CMOS process and the die microphotograph and chip layout are shown in Fig. 16. The active core occupies an area of 0.06mm^2. The test chip consumes 1mW power operating from 1.2V supply at a sampling frequency of 205MHz. The quantizer outputs are converted from thermometer to binary code before being brought out of the chip. Measurement on the prototype has indicated that a large portion of the ADC power is due to the static current in the DAC which in turn increases the

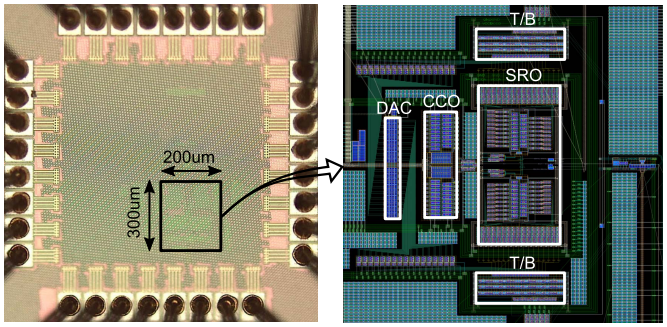

Fig. 16. Chip microphotograph and layout.

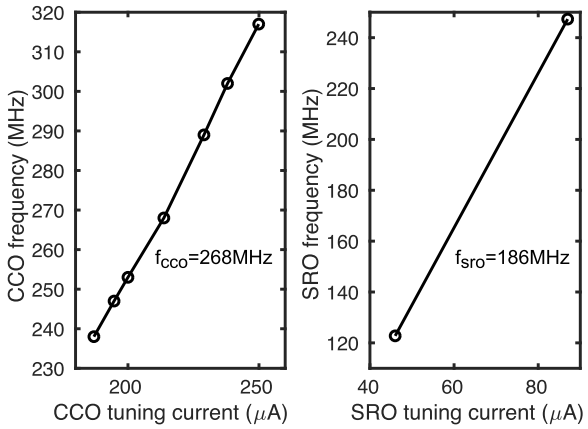

Fig. 17. Measured CCO and SRO frequency tuning curve.

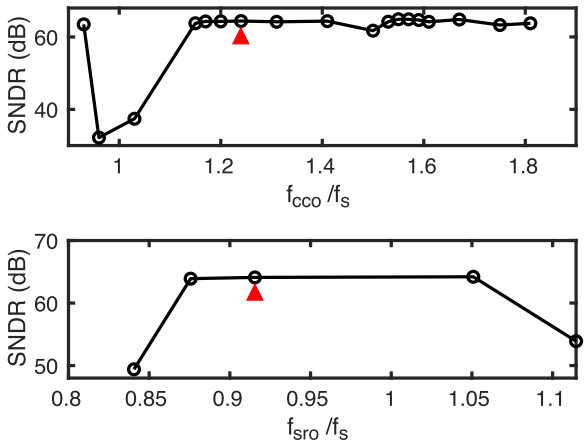

Fig. 18. Measured SNDR vs CCO and SRO center frequencies.

ADC power. This is because the NMOS DAC draws the static current away from the CCO which has to be supplied by the PMOS tail current sources to maintain the CCO center frequency close to 260MHz. In future iterations of the ADC, we will use a PMOS DAC to reduce ADC power consumption.

Fig. 17 shows the measured tuning curves of the CCO and SRO. The measured CCO center frequency is 268MHz. The measured SRO center frequency is 186MHz. Fig. 18 shows the measured SNDR versus CCO and SRO center frequencies. The CCO and SRO center frequencies selected for this design

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TABLE II
COMPARISON WITH STATE-OF-THE-ART VCO ADCS

	[5]	[26]	[27]	[28]	[2]	[29]	[12]	[14]	[30]	[13]	**This Work**
Process(nm)	90	90	90	65	65	65	65	40	65	130	**65**
Area (mm^2)	0.36	0.170	0.120	0.150	0.075	0.020	0.010	0.017	0.03	0.02	**0.06**
OTA used	Yes	Yes	Yes	Yes	No	No	No	No	No	No	**No**
Calibration[1]	No	Yes	Yes	Yes	Yes	Yes	No	No	No	No	**No**
NTF order	2^{nd}	3^{rd}	3^{rd}	3^{rd}	1^{st}	1^{st}	3^{rd}	2^{nd}	1^{st}	3^{rd}	**2^{nd}**
Fs (MHz)	600	480	300	250	1600	300	1000	1600	205	20	**205**
Power (mW)	16	14.3	4.3	10.5	17.5	11.4	1.5	2.6	3.3	0.28	**1**
BW (MHz)	10	10	8.5	20	12.5	30	10	40	25.6	0.02	**2.5**
SNDR (dB)	76.6	70.3	67.2	60	74	64	55.1	59.5	50.3	69.6	**64.2**
FoM_S[2](dB)	164	158.5	160	153	162.5	158	153.5	161.4	149	148	**158.2**
FoM_W[3](fJ/step)	144.8	267.3	135.1	321.3	170.9	146.7	161.4	42.1	241	2836	**150.9**

[1]includes calibration and explicit ELD compensation DAC; [2]FoM_S = SNDR + $10\log_{10}$(BW/Power); [3]FoM_W = Power/(2^{ENOB}x2BW)

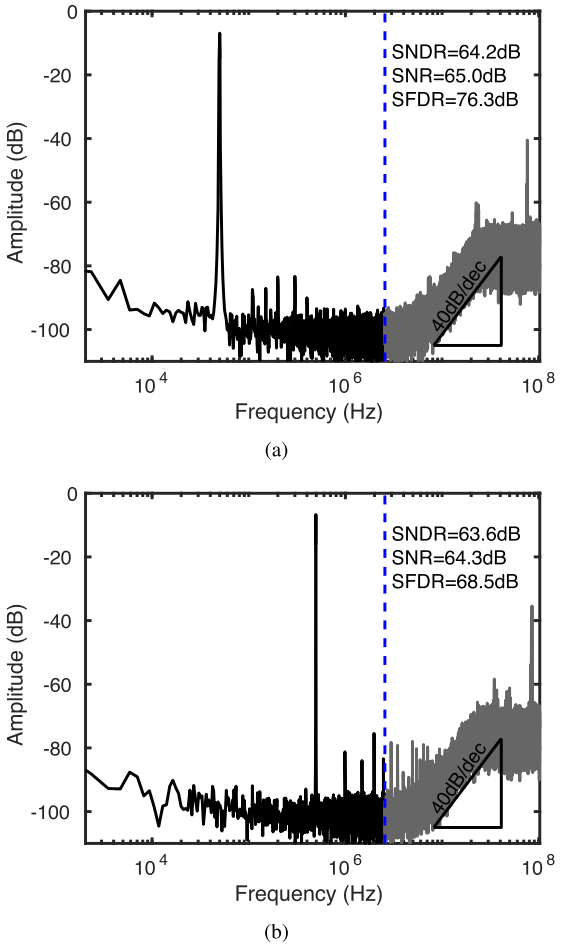

Fig. 19. ADC spectrum for (a) f_{in} = 50kHz and (b) f_{in} = 500kHz.

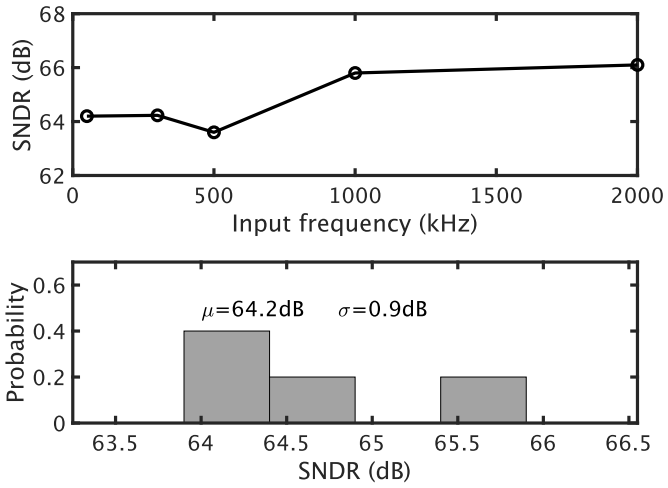

Fig. 20. (a) Measured SNDR versus input frequency. (b) Histogram of SNDR across 5 chips.

are highlighted by red triangle underneath the frequency point. As discussed in Section II, the ADC SNDR drops when f_{cco} is close to f_s, but increases and remains around 64dB when f_{cco} is less than $0.9f_s$ or is in the range of $1.1f_s - 1.8f_s$. As long as f_{sro} is in the range of $0.87f_s$ and $1.05f_s$, the SRO does not overflow and the ADC has high SNDR.

Fig. 19 shows the ADC spectrum for input frequencies of 50kHz and 500kHz and amplitude of $70\mu A_{pk-pk}$. The FFT is plotted for 2^{16} points with 5 times averaging of the PSD. The ADC spectrum clearly shows second-order noise shaping. The ADC has an SNDR of 64.2dB at f_{in} = 50kHz and 63.6dB at f_{in} = 500kHz. The SNR at these frequencies are 65dB and 64.3dB respectively. The ADC shows in-band even-order distortion tones with SFDR greater than 68dB. Even-order distortion tones indicate mismatch between the differential paths in the circuit. Mismatch in SRO center frequencies is measured to be 1.2%. Mismatch in CCO center frequencies could not be measured for this prototype.

Fig. 20(a) shows the variation of SNDR versus input frequency. The SNDR improves at input frequencies of 1MHz and 2MHz since the distortion tones fall out of band. Fig. 20(b) shows the histogram of SNDR measured across 5 chips. The average SNDR is 64.2dB with standard deviation of 0.9dB. The measured SNDR and SNR versus input amplitude is shown in Fig. 21(a). The ADC has a dynamic range of 69dB. Fig. 21(b) shows the SNDR as a function of supply voltage.

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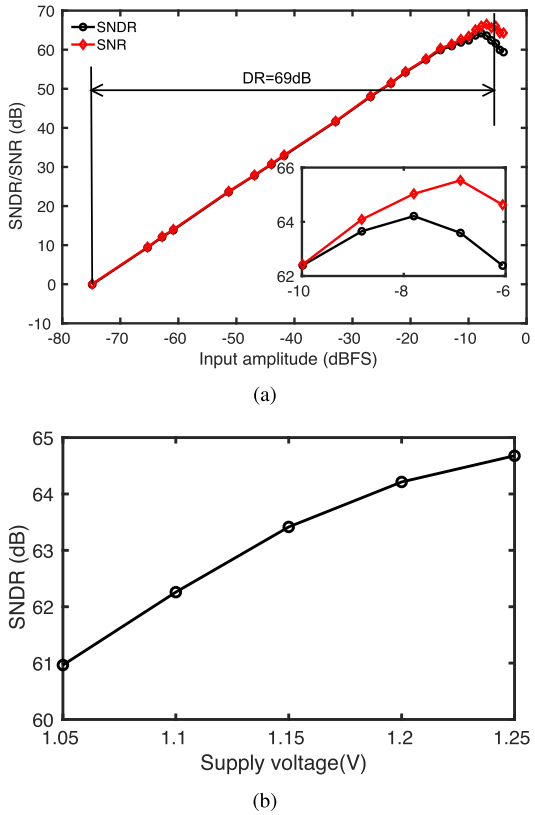

Fig. 21. ADC SNDR versus (a) input amplitude; and (b) supply voltage.

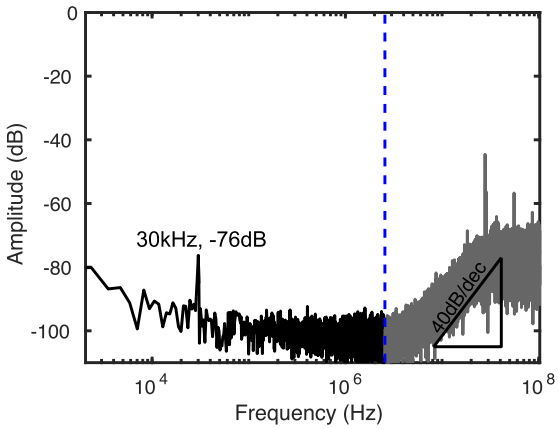

Fig. 22. Measured PSRR of the ADC.

The ADC SNDR drops from 64.8dB to 61dB as the supply voltage is reduced from 1.25V to 1.05V. Fig. 22 shows the measured power supply rejection performance of the ADC. A 30kHz, 11mV, rms sine-wave is injected into the analog power supply and appears as a tone at 30kHz at the ADC output spectrum shown in Fig. 22. The CCO and SRO share the same analog power supply. The -76dB tone at the ADC output when referred to the power supply is equivalent to 17μV. Thus, the power supply rejection ratio (PSRR) of the ADC is 56.2dB.

Table II compares our work with state-of-the-art VCO-ADCs. While the proposed ADC compares favorably with the state-of-the-art ADCs, there is a lot of room for improvement. The prototype ADC has a large in-band thermal noise which degrades energy efficiency of the ADC and is due to non-optimal design of the CCO. For this first prototype, we used the same 17 stage architecture for both CCO and SRO which led to a low tuning gain for the CCO. Since the phase information of only one inverter from the CCO is used, the number of inverters in the CCO can be reduced. For the same tuning gain, we can reduce CCO power consumption by reducing its number of inverter stages and improve energy efficiency. By increasing the number of quantizer levels while keeping the input swing constant, the CCO center frequency can be reduced which will reduce CCO input referred noise. Alternatively, we can use phase output from all the CCO inverters which will effectively allow reduction in CCO center frequency, and, CCO input referred noise. However, this comes at the cost of reduced linearity of the SRO. As mentioned earlier, we can also reduce power consumption by changing to PMOS DAC instead of NMOS DAC. For our future prototypes, we will incorporate these architectural modifications to improve energy efficiency.

V. Conclusion

This paper presented a novel architecture for VCO-based second-order CT $\Delta\Sigma$ ADC. The proposed architecture does not require any nonlinearity calibration or excess loop delay compensation. The highly digital nature of the proposed ADC means that its energy efficiency will naturally improve with technology scaling.

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Akshay Jayaraj received the B.E. degree from the Madras Institute of Technology, Anna University, Chennai, India, in 2016. He is currently pursuing the M.S. degree in electrical engineering with University at Buffalo, Buffalo, NY, USA. In 2018, he was an Intern with the Analog/Mixed Signal Design Group, MACOM, Santa Clara, CA, USA. His current research interests include data converters, mixed signal machine learning circuits, and high-speed transceivers.

Mohammadhadi Danesh graduated from the Iran University of Science and Technology. He is currently pursuing the Ph.D. degree in electrical engineering with University at Buffalo. During his master's degree, he was involved in such low-power analog current-mode computational circuits. He was with IDEX America Inc., as a Mixed-Signal Circuit and Behavioral Model Designer. His research interests include VCO-based ADC design and analog current-mode circuits design.

Sanjeev Tannirkulam Chandrasekaran received the B.Tech. degree in instrumentation technology from SASTRA University, Thanjavur, India, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with University at Buffalo, Buffalo, NY, USA. His research interests include the development of low-power, scaling friendly high-resolution ADCs incorporating time-assisted data conversion techniques for applications in the Internet of Things and biomedical systems. In 2018, he interned with the Mixed-Signal Circuit Laboratory, GE Global Research, Niskayuna, NY, USA, designing a high-resolution ADC for ultrasound imaging and exploring analog front-end architectures for CMUT transducer arrays.

Arindam Sanyal (M'14) received the B.E. degree from Jadavpur University, India, in 2007, the M.Tech. degree from IIT Kharagpur in 2009, and the Ph.D. degree from The University of Texas at Austin in 2016.

He is currently an Assistant Professor with the Electrical Engineering Department, The State University of New York at Buffalo. Prior to this, he was a Design Engineer involved in low-jitter PLLs at Silicon Laboratories, Austin. His research interests include analog/mixed signal design, bio-medical sensor design, analog security, and on-chip artificial neural networks. He received the Intel/Texas Instruments/Catalyst Foundation CICC Student Scholarship Award in 2014 and the Mamraj Agarwal Award in 2001.