# A Highly Digital Second-Order Oversampling TDC

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***Abstract*—A second-order, single loop $\Delta\Sigma$ time-to-digital converter (TDC) is presented in this paper. The proposed TDC uses 2 differential current-controlled oscillators as phase domain integrators. The proposed architecture does not require excess loop delay compensation or nonlinearity calibration. Digital differentiation using XOR implements an intrinsic first-order high-pass shaping of static element mismatch in the current steering digital-to-analog converter. A prototype TDC in 65nm CMOS process has linearity of 8.1bits, integrated noise of 3.8ps and energy efficiency of 0.45pJ/code over a bandwidth of 2.5MHz.**

***Index Terms*—time-to-digital converter, delta-sigma, current-controlled oscillator, noise shaping**

## I. Introduction

Accurate measurement of time-difference between two events is required for a wide variety of applications such as time-of-flight measurements [1] and positron emission tomography (PET) imaging. While time-to-digital converters (TDCs) in the past decade often had resolutions in the range of a few nanoseconds to hundreds of picoseconds, advances in CMOS technology scaling and the recent innovations in time-domain signal processing has led to TDCs with resolutions in the range of few picoseconds. Similar to analog-to-digital converters (ADCs), nyquist rate TDCs can operate at higher bandwidths while oversampling TDCs generally have finer resolution. Delay line and vernier delay line [2] based TDCs are some of the most popular flash architectures for high conversion rate applications. In addition, successive approximation register (SAR) [3], two-step [4] and pipelined architectures have also been proposed for nyquist rate TDCs. While vernier TDCs can achieve fine resolution at small input range, two-step and pipelined TDCs can achieve fine resolution at large input range but require complicated calibration and/or time-amplifier which is non-trivial to design. Gated and switched ring oscillator architectures [5], [6] have been proposed for oversampling $\Delta\Sigma$ TDCs, but these architectures provide only first-order quantization noise shaping. Higher-order $\Delta\Sigma$ TDCs use either a time-to-voltage converter (TVC) followed by a voltage-domain $\Delta\Sigma$ ADC [7] or use multi-stage noise shaping (MASH) TDCs [8] operating in time-domain. TVCs are usually not very linear and often require operational amplifiers to improve linearity at the cost of increased power consumption. On the other hand, MASH TDCs require extraction of time-domain quantization error which is not trivial.

In this work, we propose a single-loop $\Delta\Sigma$ TDC based on current-controlled oscillators (CCOs) as phase domain integrators. While an ADC architecture was presented in [9], [10], this work extends the architecture for TDC and presents measurement results on a 65nm prototype. A feedback loop using current-steering digital-to-analog converter (DAC) reduces CCO nonlinearity and no nonlinearity calibration is required. The proposed architecture does not require excess loop delay (ELD) compensation. Static element mismatch in the DAC is high-pass shaped without requiring any explicit calibration/dynamic element matching. For the proposed TDC, frequency of input pulse is independent of sampling frequency. A prototype TDC has been fabricated in 65nm and has an integrated noise of 3.8ps at 0.45pJ/code. The rest of this paper is organized as follows: Section II presents the proposed architecture and design insights, and Section III presents measurement results on the test chip.

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## II. Proposed TDC

### A. Architecture

Fig. 1(a) shows the proposed TDC architecture. The time difference, $t_{in}$, between two input pulses START and STOP are sent to a tri-state phase/frequency detector (PFD). The PFD outputs modulate the current input to differential CCOs between a high current, $I_{H1}$, and a low current, $I_{L1}$ depending on $t_{in}$. The CCOs perform a phase domain integration of the PFD output. A second PFD extracts the time instants when outputs of the two CCOs cross $2\pi$ and encodes this information in the form of UP and DN pulses. This operation is equivalent to having an edge detector after the CCO which outputs dirac delta impulses co-incident with rising edges of CCO output. The impulses are then converted into pulses by the PFD. As shown in [11], a CCO with an edge detector represents a pulse-frequency modulator. Since the CCO sees a multi-tone input, its spectral response is non-trivial to calculate [12]. The CCO quantization tones pass through the SRO and XOR gates, which act as a sinc filter with nulls at multiples of sampling frequency, $f_s$, before getting sampled. If the CCO center frequency, $f_{cco}$, is chosen properly, CCO quantization noise can be adequately suppressed before aliasing into signal band. An optimal choice is selecting $f_{cco}$ such that the quantization aliases remain out-of-band even if $f_{cco}$ varies due to PVT changes. Based on behavioral simulations, setting $f_{cco} = 1.3f_s$ adequately suppresses in-band CCO quantization noise while providing robustness against variations.

The PFD phase output is integrated by a differential switched ring oscillator (SRO). The SRO switches between two currents, $I_{H2}$ and $I_{L2}$, depending on the polarity of the PFD output. Thus, the SRO has very high linearity. SRO phase is multi-bit quantized, digitally differentiated using XOR gates and fed back to the CCOs using a multi-bit DAC. As shown in Fig. 1, the DAC consists of 17 NMOS cascode current sources. Similar to the CCO, the SRO can also be modeled by a PFM with the digital differentiation acting as a sinc filter [11]. The SRO sees unfiltered CCO quantization tones at its input and as

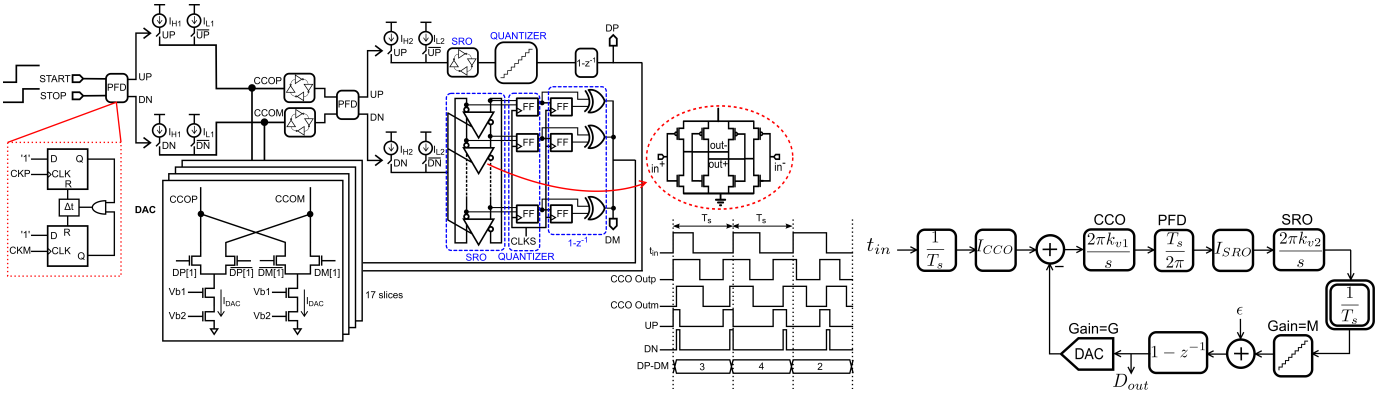


Fig. 1. (a) Proposed TDC schematic and timing diagram (b) linear model of proposed TDC

such its spectral response contains contributions from a large number of inter-modulation products which makes it non-trivial to choose an optimal SRO frequency, $f_{sro}$. Behavioral simulations show that in-band quantization noise is dominated by second-order shaped SRO quantization noise if $f_{sro}$ is set the same as $f_{cco}$. Based on simulations, both $f_{cco}$ and $f_{sro}$ can vary by $\pm 10\%$ before the SNDR starts to drop significantly.

Fig. 1(b) shows the frequency domain linear model of the proposed TDC. The front-end PFD is modeled by time input $t_{in}$ and a gain $I_{CCO}/T_s$ where $I_{CCO} = I_{H1} - I_{L1}$. The CCO and SRO gains are denoted by $k_{v1}$ and $k_{v2}$ respectively. The PFD is modeled by a linear subtractor in phase domain with a gain of $T_s/2\pi$ where $T_s$ is the sampling period. The SRO current is modeled by $I_{SRO}$ where $I_{SRO} = I_{H2} - I_{L2}$. The sampling operation after the SRO is modeled by a gain of $1/T_s$. The multi-bit quantizer is assumed to have a linear gain of $M$ and the multi-bit DAC is modeled with a linear gain of $G$. The TDC quantization noise is denoted by $\epsilon$. Using impulse-invariance transform, the digital output, $D_{out}$ can be written as

$$D_{out} = \frac{HI_{CCO}\left(z^{-1}+z^{-2}\right)t_{in}/T_s + 2\epsilon\left(1-z^{-1}\right)^2}{2+\left(HG-2\right)z^{-1}+\left(HG\right)z^{-2}} \quad (1)$$

where $H = 2\pi I_{SRO} k_{v1} k_{v2} M T_s^2$. It can be seen from (1) that the proposed TDC high-pass shapes quantization noise to the second-order. It should be pointed out here that $\epsilon$ is the SRO quantization noise. It can be shown through rigorous mathematical analysis that CCO quantization noise appears at the output as first-order shaped but it is made much smaller than second-order shaped SRO quantization noise through our choice of CCO and SRO center frequencies. However, the complete analysis is out of scope of this letter.

### B. Circuit Design

A 17 stage ring oscillator is used for both CCO and SRO stages with $k_{v1} = k_{v2}$. The CCO and SRO stages are designed with identical parameters except for $(I_{H1}, I_{L1})$ and $(I_{H2}, I_{L2})$. As shown later, $I_{H2}$ and $I_{L2}$ are set by SRO stability considerations. The DAC in Fig. 1(a) draws an average current of $17 \cdot I_{DAC}$ away from the CCO and hence $I_{H1}$ is set to $(I_{H2} + 17 \cdot I_{DAC})$ and $I_{L1}$ is set to $(I_{L2} + 17 \cdot I_{DAC})$. The circuit design involves balancing the trade-offs between noise, stability and linearity. The TDC input-referred noise is dominated by thermal and flicker noise from CCO+DAC and shaped quantization noise from SRO. Static mismatch in the NMOS current sources in the multi-bit current steering DAC are first-order high-pass shaped by intrinsic data weighted averaging (DWA) pattern in SRO output. A non-return-to-zero (NRZ) DAC is used to reduce clock jitter.

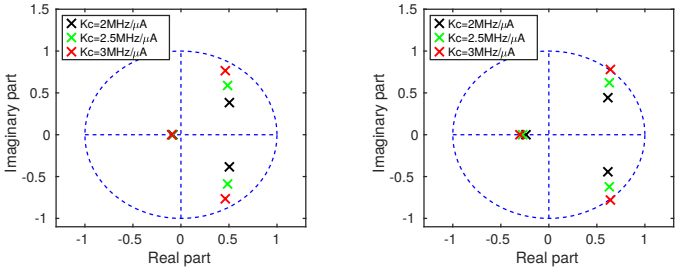


Fig. 2. z-domain poles of $NTF$ for (a) $\tau = 0.4T_s$; and (b) $\tau = 0.8T_s$

For the second-order loop to be stable, the PFD after CCO and the SRO should not overflow. In addition, ELD can introduce additional pole in a system with NRZ DAC and degrade stability. Higher-order, continuous-time modulators typically introduce an auxiliary DAC around the quantizer to compensate for ELD. For the proposed architecture, ELD is compensated by tuning the CCO and SRO gains and no auxiliary DAC is needed. Fig. 2 shows z-domain poles of the noise-transfer function (NTF) versus ELD for different values of $k_c$=$k_{v1}$=$k_{v2}$. As can be seen from Fig. 2, as long as CCO and SRO gains remain below 2.5MHz/$\mu$A, the NTF poles remain inside the unit circle and the loop can absorb an ELD of $0.8T_s$. The upper bound on the SRO gain, $k_{v2}$, for no phase overflow is given by $(I_{H2} - I_{L2}) \cdot k_{v2} \cdot T_s \leq 0.5$. For $k_{v2} = 2.5$MHz/$\mu$A and $T_s = 5$ns, $I_{H2} - I_{L2} \leq 40\mu$A. For the PFD after CCO to not overflow, the input current swing seen by the CCOs cannot exceed a certain limit. The input swing of the CCOs is given by $(D_{out} \cdot G - I_{CCO} t_{in}/T_s)$ and from (1), it can be seen that the input swing of the CCOs is set primarily by the out-of-band quantization noise. In order to find the maximum input handling capability of the CCOs, a simulation was performed by sweeping LSB step size $(I_{DAC})$ and recording CCO input swing. The input time difference

between START and STOP pulses is kept fixed for the $I_{DAC}$ sweep. The CCO gain was kept at 2.5MHz/$\mu$A. The results are shown in Fig. 3(a). It can be seen that as $I_{DAC}$ exceeds 5$\mu$A, the CCO input swing rises sharply which causes PFD overflow and makes the loop unstable. Higher $I_{DAC}$ reduces input-referred DAC noise and improves TDC jitter but setting $I_{DAC}$ too high makes the loop unstable. In order to not exercise the nonlinear region of the CCO, $I_{DAC}$ is set to $4.5\mu$A for this design. Another source of non-ideality is the mismatch between the differential paths in the TDC. Difference in CCO free-running frequencies due to mismatch in current sources driving the CCO results in TDC offset. Fig. 3(b) shows the effect of mismatch in CCO free-running frequencies when the START signal is pulse-width modulated using a sine wave of $0.5T_s\cos(2\pi f_{in}t)$ where $f_{in} = f_s/2110$. Mismatch in CCO free-running frequencies result in TDC offset, which can be canceled through foreground calibration. In addition, mismatch between CCOs results in inadequate suppression of CCO quantization noise which can degrade TDC linearity. For this design, the distortion tones are below noise floor even with 5% mismatch in CCO free-running frequencies. Mismatches between the SROs is first-order high-pass shaped by the TDC loop. Fig. 3(c) shows that there is no significant change in TDC spectra even with 5% mismatch between SRO center frequencies.

### C. Noise Analysis

Noise from CCOs and DAC, and quantization error dominate the TDC noise. Noise from CCO and DAC is calculated by referring the phase noise at the CCO output back to the ADC input. Simulated flicker noise corner of the CCO+DAC combination is close to 100kHz. The input referred noise due to CCO+DAC is given by

$$\sqrt{\overline{i_{th,n}^2}} = \frac{T_s}{I_{CCO}} \cdot \sqrt{2} \cdot \frac{\sqrt{2DT_s}}{2\pi k_{v1} T_s} \cdot \frac{1}{\sqrt{OSR}} \tag{2}$$

where the factor $\sqrt{2}$ takes into account the noise from differential CCO and DAC. The phase diffusion constant, $D$ is given by $D = \mathcal{L}(\Delta\omega) \cdot (\Delta\omega)^2/2$ where $\mathcal{L}(\Delta\omega)$ is the phase noise at an offset frequency of $\Delta\omega$. At an offset frequency of 0.16MHz, the phase noise is -81.5dBc/Hz. For $k_{v1}$ of 2.2MHz/$\mu$A, $I_{CCO} = 35\mu$A, $T_s = 5$ns and OSR of 40, the input referred noise due to CCO+DAC is given by 2.8ps. Quantization noise of the TDC is second-order shaped and can be calculated from

$$\sqrt{\overline{i_{q,n}^2}} = \frac{T_s}{I_{CCO}} \cdot \frac{2I_{DAC}/N}{\sqrt{12}} \cdot \frac{\pi}{\sqrt{5}} \cdot (OSR)^{-5/2} \tag{3}$$

However, this does not take into account the in-band folding of quantization noise due to CCO nonlinearity. Fig. 4 shows the TDC spectrum assuming that the START signal is pulse-width modulated using a sinewave of $0.5T_s\cos(2\pi f_{in}t)$ where $f_{in} = f_s/2110$. In the absence of thermal noise and with an ideal CCO, SQNR of the TDC is 76dB. Nonlinearity of 6-bit CCO folds quantization noise into the signal band, and the SQNR is degraded to 72dB. In the presence of thermal noise, the SNR is reduced to 56dB. The folded in-band quantization noise is 0.1ps and is negligible compared to thermal noise.

## III. Measurement Results

Fig. 5 shows die photograph and layout of the prototype TDC fabricated in 65nm process. The active core occupies an area of $0.06\text{mm}^2$. The test chip consumes 0.63mW power operating from 1.2V supply at a sampling frequency of 205MHz. Dynamic test is performed to measure the noise performance of the prototype. The TDC receives a clock and a phase-modulated clock as START and STOP inputs. A 100kHz sine wave with 100ps peak-to-peak amplitude modulates the phase of a 100MHz clock. A small modulating signal is used as the signal generators in our lab cannot generate phase-modulated signal with good linearity. On-chip buffers convert the TDC inputs to square wave. Fig. 6 shows the measured spectrum of the TDC with phase-modulation. The second-order noise shaping can be clearly seen. The spectrum shows distortion tones from the signal generator. The integrated noise is 3.8ps over 1kHz-2.5MHz bandwidth.

Static measurement is performed to test the linearity of the prototype. As explained before, dynamic measurement cannot be used to test TDC linearity due to distortion from signal generator. For static test, the start and stop frequencies are set to 100MHz and 100.01MHz respectively. This results in a ramp input for the TDC. The TDC digital output is low-pass filtered with 2.5MHz digital filter and rounded to 10-bits. Fig. 7(a) shows the TDC low-pass filtered output versus time input. The TDC has a linear response with a conversion range of $\pm$4.5ns. As shown in Fig. 7(a), the TDC has an integral nonlinearity (INL) of 2.7LSB which indicates that the TDC has an equivalent linearity of 8.1bits.

Single shot precision (SSP) measurement is performed to measure the clock jitter free noise performance of the TDC. For SSP test, a clock signal is split into two and applied to the TDC using wires of different lengths to create an input time difference. Since both the inputs are from the same clock, SSP test removes clock jitter. Fig. 7(b) shows the measured histogram of the TDC. Similar to static measurement, the TDC output is low-pass filtered with 2.5MHz digital filter and rounded to 10-bits. The standard deviation of the TDC output corresponds to 9.7ps which is SSP precision of the test chip.

The prototype TDC is compared with state-of-the-art TDCs in Table I. The test chip has good linearity and achieves similar figure-of-merit (FoM) as state-of-the-art. Jitter from on-chip buffers used to convert sine wave inputs from signal generator to square wave resulted in relatively large resolution of 13ps for the current test chip. In future iterations, we will reduce thermal noise from CCO and DAC to improve FoM.

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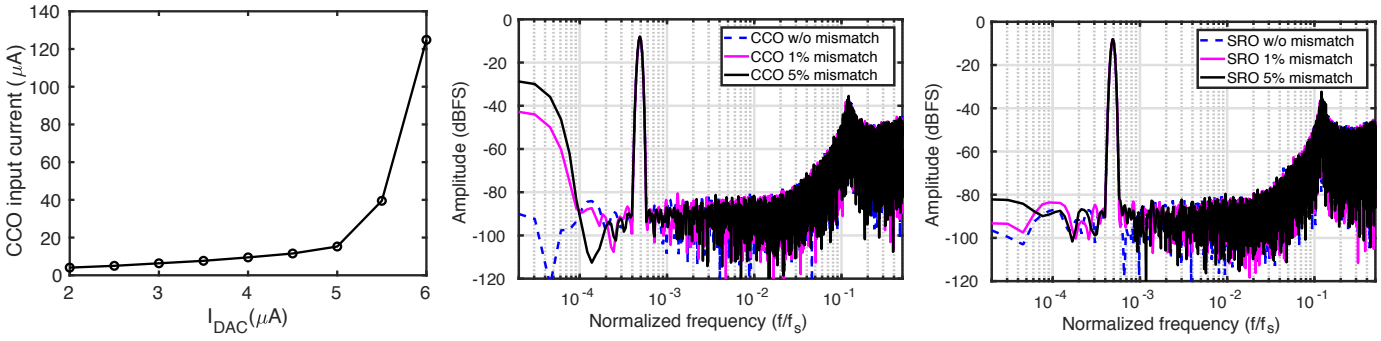



(a) (b) (c)

Fig. 3. (a) CCO input swing versus $I_{DAC}$; and TDC spectra for (b) CCO mismatch (c) SRO mismatch

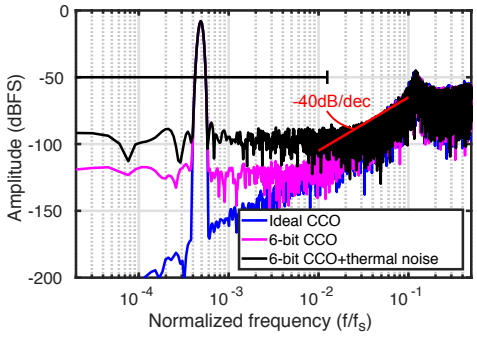



Fig. 4. TDC spectra with PWM input

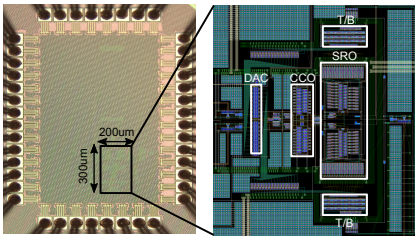



Fig. 5. Chip microphotograph and layout

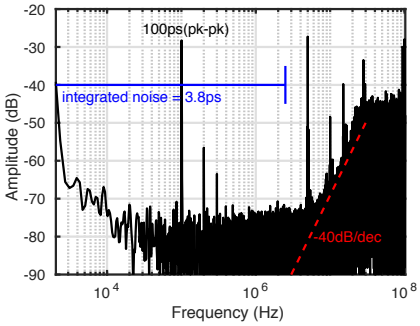
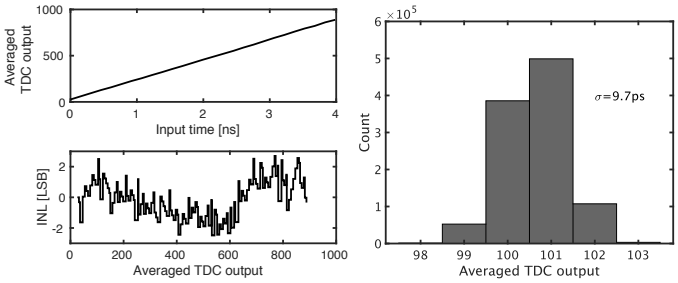



Fig. 6. TDC spectrum for $100\text{ps}_{pk-pk}$ input




(a) (b)

Fig. 7. (a) TDC transfer function and INL plot, and (b) SSP measurement result

TABLE I
COMPARISON WITH STATE-OF-THE-ART TDCS.

| | [4] | [13] | [6] | [14] | **This work** |
|---|---|---|---|---|---|
| Process(nm) | 130 | 65 | 90 | 65 | **65** |
| BW(MHz) | 0.5 | 25 | 1 | 4 | **2.5** |
| Power(mW) | 0.33 | 1.7 | 2 | 4.3 | **0.63** |
| Fs(MHz) | 1 | 50 | 500 | 200 | **205** |
| Range(ns) | 14 | 0.6 | ±2 | 4 | **±4.5** |
| Bits | 11 | 7 | 13 | 11 | **10** |
| Resolution[1](ps) | 6.98 | 4.8 | 1.1 | 1.58 | **13** |
| INL(LSB) | 1.5 | 3.3 | 5 | 2 | **2.7** |
| $N_{linear}$ | 9.7 | 4.9 | 0.4 | 9.4 | **8.1** |
| FoM[2](pJ/code) | 0.4 | 1.14 | 0.74 | 0.8 | **0.45** |

[1]Resolution $= \sqrt{\text{integrated noise}^2 \times 12}$; [2]FoM $= \frac{\text{Power}}{2^{N_{linear}} \times 2 \times \text{BW}}$
where $N_{linear} = \text{Bits} - \log_2(\text{INL} + 1)$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