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Maximum Likelihood Estimation Based SAR ADC

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***Abstract*—A 10-bit successive approximation register (SAR) ADC with maximum likelihood estimation (MLE) is presented in this work. After SAR quantization is finished, the comparator is fired 18 times and the outputs are sent to the estimator for calculation of the residue voltage. The estimator output is subtracted from the SAR output to form the overall output. MLE improves the ADC SNR by more than 8dB without the need for prior knowledge of SAR noise distribution. A prototype ADC in 65nm process achieves an average SNR of 64.5dB at sampling frequency of 1.28MHz and power supply of 1V while consuming 5.6fJ/conversion-step. The estimation accuracy is consistent across voltage and temperature ranges.**

***Index Terms*—successive approximation register (SAR), analog-to-digital converter (ADC), maximum likelihood estimation, stochastic ADC**

I. Introduction

Successive approximation register (SAR) is a widely used architecture for low power analog-to-digital converters (ADCs). SAR ADC has a highly digital nature and very good energy efficiency for medium resolutions. Novel algorithms [1]–[4] have reduced SAR switching energy to be a small fraction of the overall energy, and energy efficiency of high resolution SAR ADC is now limited by comparator thermal noise. Hence, considerable research effort has been made towards improving SAR energy efficiency at high resolution. Noise-shaping SAR improves resolution by high-pass shaping quantization and thermal noise. Both active and passive integrators are used to high-pass shape SAR noise. Active integrators use operational amplifiers [5] which are challenging to design in advanced CMOS nodes, while passive integrators [6] cannot achieve high-pass shaping at very low frequencies. Another technique to improve energy efficiency at high resolution is to use a second-stage ring oscillator [7] which cancels the thermal and quantization noise of the SAR stage. However, accuracy of SAR noise cancellation is sensitive to variations in process, voltage and temperature (PVT) and requires background calibration. Recent techniques use stochastic principles to estimate SAR residue and increase resolution of the ADC by subtracting the estimated residue from SAR output. This is similar to a two-stage ADC architecture in that the estimator acts as second-stage quantizer and the overall ADC resolution is determined by accuracy of the estimator, but at a much lower power than conventional two-stage ADC architectures.

The main motivation behind stochastic estimation is that statistical analysis of SAR residue provides an accurate quantization of the input signal at a lower power than analog scaling [8]. In addition, stochastic estimation reduces both quantization and thermal noise while analog scaling can reduce only thermal noise. Stochastic estimation is usually done after the SAR has finished quantization. Since the residue voltage is available at the comparator inputs after quantization, the comparator can be fired multiple times and the residue can be estimated from the statistics of comparator outputs. An intuitive way to estimate the residue is to apply majority voting [9]. [8] developed a data-driven technique to employ majority voting only when the input is close to comparator decision level, but requires a metastability detector. As shown in [10], [11], much better estimate can be obtained if more refined estimators, like bayesian or maximum likelihood estimation (MLE), are used. While classical estimation techniques, like maximum likelihood (ML), do not require prior knowledge of probability distribution function (PDF) of the residue voltage, bayesian estimators require prior knowledge of the PDF and may not have a closed-form expression.

In this work, we propose an MLE based data-driven noise reduction technique which does not require prior knowledge of noise distribution. The decoupling of estimation accuracy from noise distribution is a key contribution of this work. As will be shown, the proposed technique is robust against variations in supply voltage and temperature. While the preliminary architecture was presented in [12], a more detailed analysis of the architecture as well as measurement results are presented in this paper. A 10-b prototype ADC is designed in 65nm process. ADC SNR is increased by 8dB through the use of MLE. The rest of this paper is organized as follows: Section II presents the proposed architecture. Measurement results for the 65nm prototype and comparison with state-of-the-art is presented in Section III. Finally, the conclusion is brought up in Section IV.

II. Proposed Architecture

The proposed SAR ADC architecture and mathematical model are shown in Fig. 1. A single-ended SAR is shown for simplicity in Fig. 1(a) even though a differential architecture has been used in the design. The ADC uses a 10-bit capacitive DAC and bottom-plate sampling. After the SAR has finished quantization of the sampled input, the residue is estimated using an ML estimator. The ADC output is obtained by

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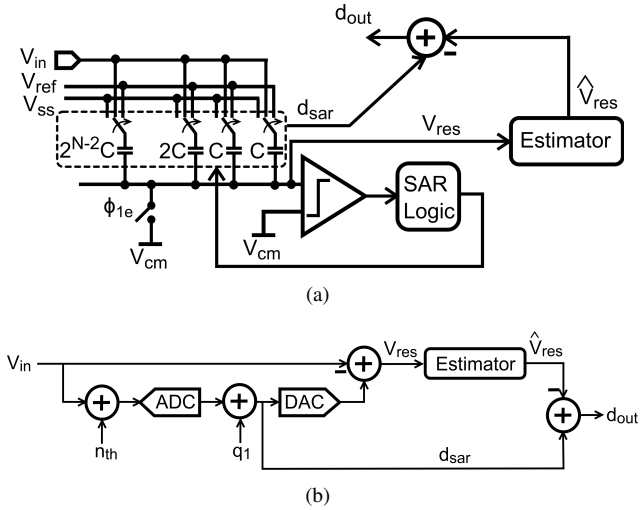

Fig. 1. (a) Circuit diagram, (b) mathematical model of proposed technique

subtracting the estimated residue from the 10-b SAR output. Fig. 1(b) shows the mathematical model of the proposed architecture. The digital output from SAR is given by

$$d_{sar} = V_{in} + n_{th} + q_1 \equiv V_{in} + V_{res} \tag{1}$$

where n_{th} is thermal noise of the comparator and DAC, q_1 is the SAR quantization noise, and V_{res} is residue after 10-bit quantization. After the SAR has finished quantization, the comparator is fired M times and the comparator outputs, $d[i]$, are used for estimating V_{res}. Using MLE, the likelihood function is designed to be the joint density of V_{res} and $d[i]$ such that

$$L(V_{res}|d[1], d[2], ..., d[M]) = \frac{1}{\sqrt{(2\pi\sigma^2)^M}} \prod_{i=1}^{M} e^{-\frac{(d[i]-V_{res})^2}{2\sigma^2}} \tag{2}$$

where σ is the standard deviation of V_{res}. Estimate of V_{res} can be obtained by setting the derivative of log-likelihood to zero and is given by

$$\hat{V}_{res} = -\frac{1}{2} + \sqrt{\frac{1}{M}\sum_{i=1}^{M} d[i]^2 + \frac{1}{4}} \tag{3}$$

The overall ADC output is given by $d_{out} = d_{sar} - \hat{V}_{res}$. Thus, the ADC resolution depends only on the accuracy of estimation and the overall ADC resolution can be higher than the number of bits in the ADC. It should be pointed out here that unlike bayesian estimation, the proposed ML estimation is independent of comparator noise distribution. $\hat{V}_{res}$ does not have to be computed every conversion cycle, but the $M+1$ possible values of $\hat{V}_{res}$ can be pre-computed, stored in a look-up table (LUT) and accessed depending on the summation of $d[i]$. Thus, from the point of hardware implementation of MLE, we need an LUT, a thermometer-to-binary converter (T/B) which sums $d[i]$ and forms the index to LUT, and a subtractor to subtract MLE output from SAR digital output. While the T/B and subtractor are not implemented on-chip, the T/B consumes 0.1μW power and published carry-select 12/13b adders [13] consume less than 0.1μW power at 1.28MHz (sampling frequency for this work). The T/B and subtractor power is 2% of the ADC power and will not degrade ADC energy efficiency if implemented on-chip.

An ML estimation technique was proposed in [10] that modeled the comparator outputs $d[i]$ as outcomes of bernoulli trials. ML estimate of the mean of bernoulli trial is given by its probability of success, which is probability of '1' of comparator output. Assuming the comparator noise is dominant and has a gaussian distribution with a standard deviation of σ_n, the mean of bernoulli trial is given by

$$\mu_m = \frac{1}{M}\sum_{i=1}^{M} d[i] = \frac{1}{2}\left[1 + \text{erf}\left(\frac{\hat{V}_{res}}{\sqrt{2}\sigma_n}\right)\right] \tag{4}$$

Thus, the residue can be estimated by

$$\hat{V}_{res} = \sqrt{2}\sigma_n \cdot \text{erf}^{-1}\left(2\mu_m - 1\right) \tag{5}$$

As can be seen from (5), the key limitation of the estimation technique used in [10] is the dependence of $\hat{V}_{res}$ on the standard deviation of comparator noise, which is also the case for bayesian estimation technique of [11]. Comparator noise can vary by a significant amount over PVT. For the comparator used in this design, σ_n is 250μV under nominal conditions. Over corners, temperature variation from -40°C to 80°C and supply voltage variation of $\pm 10\%$, σ_n varies from 190μV to 420μV. This large variation is consistent with the results reported in [11]. Simulation with a 10-bit SAR model was performed to assess the impact of σ_n variation on different estimation techniques. Fig. 2 shows SNR for different estimation techniques as a function of $\sigma_{n,estim}/\sigma_n$ where $\sigma_{n,estim}$ is the estimated value of comparator noise standard deviation calculated under nominal conditions, and σ_n is the actual value of comparator noise standard deviation. For this simulation, the comparator is fired 18 times for

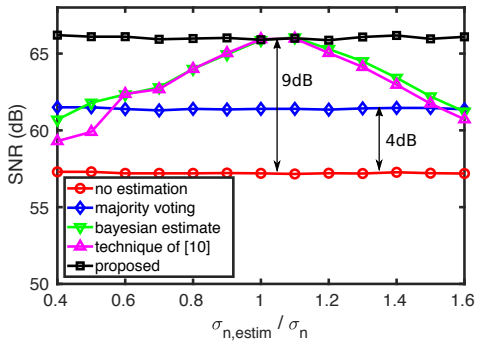

Fig. 2. SNR vs σ_n variation for different estimators

estimation of residue. When $\sigma_{n,estim} = \sigma_n$, technique of [10], bayesian [11] and the proposed technique achieve 9dB better SNR than without estimation, while majority voting improves SNR by 4dB. As $\sigma_{n,estim}$ starts to deviate from σ_n, the SNR estimated by the techniques of [10] and [11] starts to drop and eventually their accuracy becomes worse than majority voting. The estimated accuracy of the proposed MLE technique does not degrade with $\sigma_{n,estim}/\sigma_n$. This is a major advantage of the proposed technique over existing estimation techniques. [11] sought to address the dependence of estimation accuracy on PVT by creating look-up tables for different σ_n values and using a periodic foreground tracking of σ_n to choose the

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correct look-up table. The energy to track comparator noise across PVT is not reported in [11] but such a tracking circuit is likely to significantly degrade the energy-efficiency of low energy SAR ADCs.

Fig. 3 shows the spectra of 10-bit SAR with and without the proposed estimation technique. A 0dBFs input signal at frequency of $f_s/160$ is used for the simulation. The comparator noise standard deviation is set to 0.4 LSB. It can be seen that the proposed ML estimation uniformly reduces the noise floor.

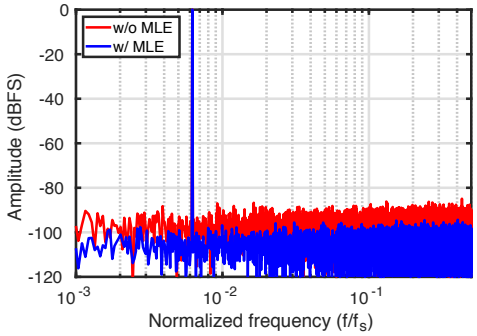

Fig. 3. ADC spectra with and without proposed estimation

A source of non-ideality that has not been considered so far is the presence of parasitic capacitance, C_p, at the comparator input. The parasitic capacitance scales the residue voltage by $G \equiv C_{DAC}/(C_p + C_{DAC})$ where C_{DAC} is the total capacitance in the DAC. For perfect estimation, $\hat{V}_{res}$ should be scaled by $1/G$. Fig. 4 shows the effect of gain error $1-G$ on estimation accuracy of proposed ML technique if $\hat{V}_{res}$ is not scaled by $1/G$. It can be seen that even with relatively large gain error of 10%, the estimated SNR is degraded by less than 0.5dB. For the proposed design using MLE, the comparator is sized small to consume low power and, hence gain error due to C_p is much less than 10%. Thus, gain error correction is not used in this design. In addition, parasitic capacitance at comparator input introduces nonlinearity. However, the small comparator size used in this design results in a small comparator input capacitance which is only 0.05% of C_{DAC} and, thus, does not affect ADC linearity.

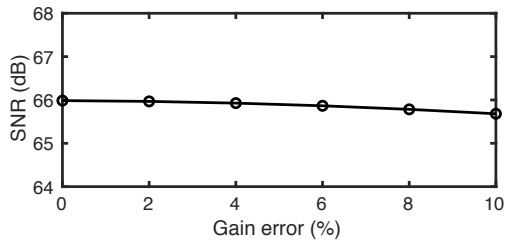

Fig. 4. ADC SNR versus gain error

Bi-directional switching technique [3] with bottom-plate sampling is used in the design to reduce switching power by 86% compared to conventional SAR. For 11-bit linearity, capacitance mismatch has to be less than 0.5%. Based on foundry mismatch data, a 4.8fF unit metal-on-metal (MOM) capacitor is used for the capacitive DAC to ensure 11-bit linearity. The total capacitance in each DAC is 2.4pF. A strong-arm latch is used as comparator. For the 10-bit ADC, switching power is calculated to be 3.8μW according to [2].

III. Measurement Results

A prototype ADC is fabricated in 65nm CMOS process and the die microphotograph and layout are shown in Fig. 5. 64-pin TQFP package is used for the prototype. The core circuit occupies an area of 350μm by 350μm. The test chip consumes a power of 9μW operating from a 1V supply at sampling frequency of 1.28MHz, and the comparator is fired 18 additional times after quantization for ML estimation. Out of 9μW power, 5μW is consumed by the comparator and SAR logic, while the DAC consumes 4μW. The DAC switching power agrees very well with the switching power estimated in Section II.

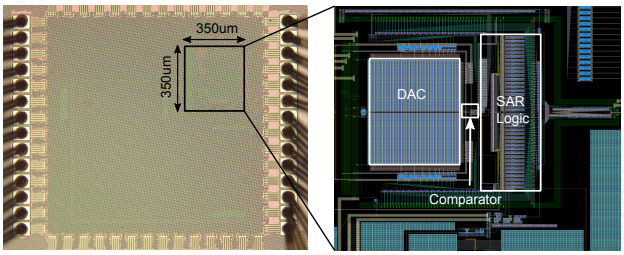

Fig. 5. Chip microphotograph and layout

Fig. 6 shows the distribution of the ADC digital output for $V_{in} = 0$. As shown in Fig. 6, application of MLE reduces ADC noise standard deviation from 0.49 LSB to 0.21 LSB. kT/C noise for this design is much smaller than thermal and quantization noise. The comparator noise is approximately 0.4 LSB and quantization noise is 0.29 LSB (assuming quantization noise is almost white for 10-b ADC). Without ML estimation, even if the comparator noise is reduced to zero (by increasing the comparator power infinitely), the ADC noise will still be limited by quantization noise to 0.29 LSB. Thus, measurement results clearly demonstrate that application of MLE can increase ADC resolution beyond the limits imposed by quantization noise. With MLE, the comparator is fired 18 more times, which increases the ADC power by a factor of 1.4, but reduces the noise by 8dB. MLE is better than oversampling as oversampling will increase ADC power by a factor of 7 to achieve the same 8dB noise reduction as MLE. Measurement results indicate that the comparator was over-designed and in future prototypes, a lower power and higher noise comparator will be used to improve ADC energy efficiency further.

Fig. 7 shows the FFT of the ADC with and without MLE. An input frequency of 50kHz at $1.6V_{pk-pk}$ corresponding to -1.9dBFS is used for the FFT plot. MLE improves SNR by 8dB. MLE reduces noise floor as well distortion tones from quantization noise. The SNR enhancement is better than that in [11] without requiring calculation of comparator noise at different operating points. The SFDR is $>$ 70dB and is limited by second-order distortion tone that comes from off-chip TTE filter used to reduce thermal noise of the input signal generator. Fig. 8 plots the variation of SNR and SNDR versus input amplitude. The ADC achieves a high dynamic range of 70dB. Fig. 9 shows the DNL and INL plot for the ADC. The ADC

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has a DNL of $+0.86/-0.44$ LSB and an INL of $+0.78/-0.54$ LSB. Fig. 10 shows the SNDR and energy efficiency versus the number of times, M, the comparator is fired for ML estimation. SNDR keeps increasing as M is increased but energy efficiency is the highest for $M = 6$. $M = 18$ is chosen in this design for obtaining higher SNDR.

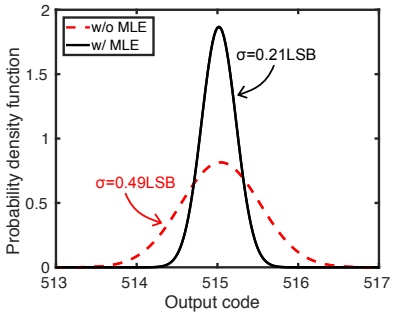

Fig. 6. Distribution of ADC output for $V_{in} = 0$

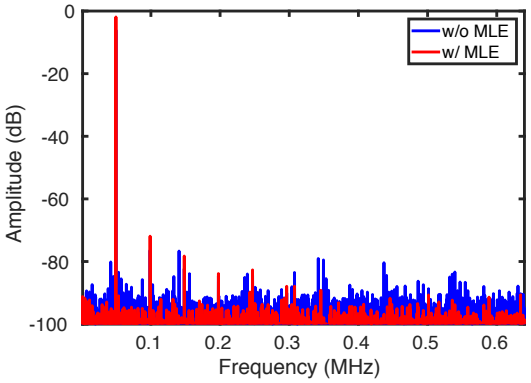

Fig. 7. FFT of ADC at $V_{in} = 1.6V_{pp}$

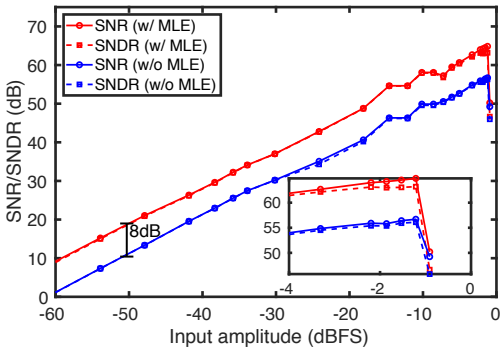

Fig. 8. SNR/SNDR versus input amplitude sweep

To test the robustness of the proposed estimation technique, the ADC was tested at different sampling frequencies, power supply voltages and temperatures. The measurements are performed with an input signal of frequency 50kHz and an amplitude of $1.6V_{pk-pk}$. Fig. 11 plots the ADC SNR and SNDR with and without MLE for sampling frequencies from 1MHz to 2.2MHz. MLE consistently improves SNR by 8dB across the different sampling frequencies. MLE also improves SNDR across sampling frequency. Fig. 12(a) shows the variation of SNDR as a function of supply voltage for 3 chips. MLE

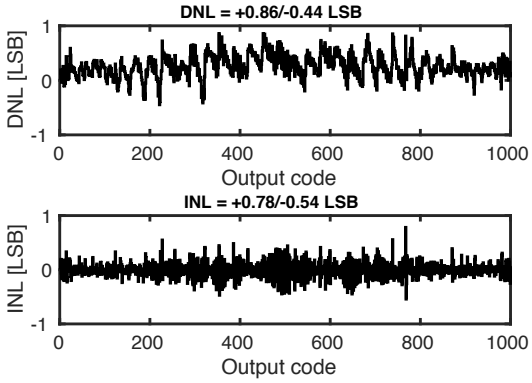

Fig. 9. DNL and INL plot of ADC

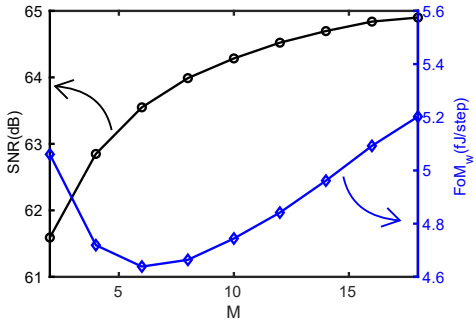

Fig. 10. SNR and energy-efficiency vs M

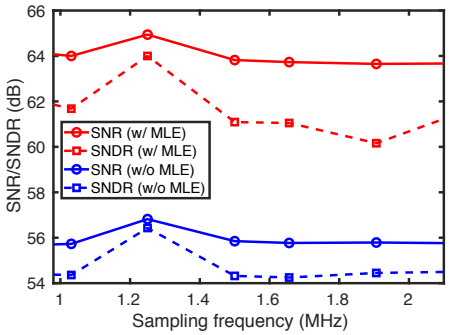

Fig. 11. ADC SNR and SNDR versus sampling frequency

consistently improves SNDR over the supply voltage range of $0.9 - 1.1$V. The ADC was kept inside a temperature oven and the temperature was swept from $-5°$C to $50°$C. The oven temperature was kept lower than $60°$C to protect components on the test board with plastic packaging. Fig. 12(b) shows the variation of SNDR versus temperature for 3 chips. Use of MLE results in 6.5-8dB improvement in SNDR over the temperature range. All the measurements were performed without having to compute standard deviation of ADC noise at different operating points. This is an important advantage of the proposed technique over estimation techniques [10], [11] that require prior knowledge of noise distribution.

Table I compares our work with state-of-the-art SAR ADCs designed in CMOS technologies from 90-45nm. It can be seen that ADCs with stochastic estimation typically has better energy efficiency than ADCs without estimation. The proposed ADC achieves a walden FoM of 4.9fJ/conversion for $M = 6$ and 5.6fJ/conversion for $M = 18$ averaged over 3 chips, which compares favorably with state-of-the-art SAR ADCs, while

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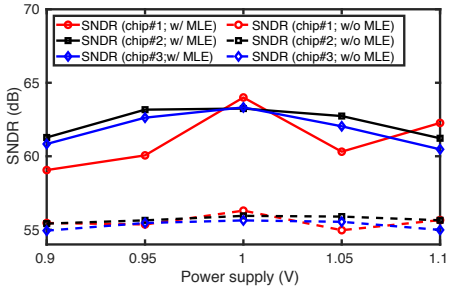
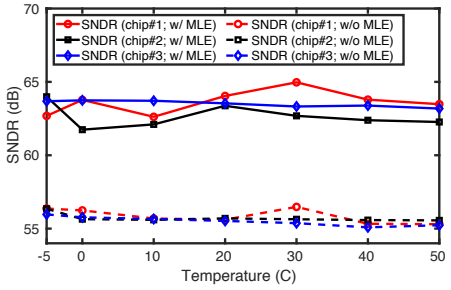
TABLE I
COMPARISON WITH STATE-OF-THE-ART SAR ADCS.

	[14]	[4]	[15]	[16]	[9]	[11]	[8]	[10]	**This work**	
Process(nm)	90	65	65	65	65	65	90	40	**65**	
Power supply (V)	1.1	1	0.55	0.6	0.5	0.7	1	1.1	**1**	
Area (mm^2)	0.047	0.026	0.21	0.08	0.07	0.03	0.05	0.05	**0.12**	
Fs (MHz)	4	1	0.02	0.04	0.25	0.1	10.2	35	**1.28**	
Stochastic estimation	No	No	No	M=5	M=11/27	M=16	No	M=16	**M=6**	**M=18**
Power (μW)	17.44	1.9	0.2	0.07	0.29	0.6	26.3	420	**7**	**9**
SNR (dB)	–	55.6	–	–	–	65	–	–	**63.2**[3]	**64.5**[3]
SNDR (dB)	56	54.4	55	58.2	46.8	64.5	52.5	> 60	**62.5**[3]	**63.5**[3]
ENOB	9.4	8.7	8.8	9.4	7.5	10.5	8.4	> 9.7	**10.1**[3]	**10.3**[3]
FoM_w[1](fJ/step)	6.5	4.4	22.4	2.7	3.3	4.5	12	< 15	**4.9**[3]	**5.6**[3]
FoM_s[2](dB)	166.6	168.6	161.9	172.7	168.8	173.7	161.5	> 166	**172.1**[3]	**172**[3]

[1] $\text{FoM}_w = \dfrac{\text{Power}}{2^{\text{ENOB}} \times \text{Sampling Frequency}}$; [2] FoM_s = SNDR + 10log$_{10}$(Bandwidth/Power); [3] averaged over 3 chips



(a)



(b)

Fig. 12. ADC SNDR versus (a) supply voltage (b) temperature for 3 chips

not requiring prior knowledge of ADC noise distribution. The ADC energy efficiency can be improved further by optimizing the comparator and migrating to advanced technology nodes.

IV. CONCLUSION

This paper presented an MLE based stochastic technique to reduce ADC noise and improve energy efficiency. The proposed estimation technique does not require prior knowledge of ADC noise distribution and measurement results have shown the proposed technique to be robust against variations in supply voltage and temperature.

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