A Digital PLL Based 2nd-Order $\Delta\Sigma$ Bandpass Time-Interleaved ADC

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***Abstract*—This paper presents a time-interleaved (TI) VCO-based band-pass ADC with a second-order bandstop noise transfer function. The proposed ADC uses a digital phase-locked loop (PLL) based architecture and employs current starved ring-oscillator as integrator which provides inherent multi-bit quantization. Thus, the proposed band-pass ADC does not need op-amps for integration and consumes low power and area. The proposed ADC is designed in 65nm CMOS and Matlab and Spectre simulations were performed to characterize the ADC. The proposed ADC achieves 61dB SNDR while consuming 0.44mW and has a Walden FoM of 63fJ/conv. step.**

I. Introduction

Owing to the rapid growth in Internet-of-Things (IoT), there is an increase in smart devices that acquire and transmit data using multi-standard re-configurable radios [1]. Depending on power consumption, IoT radios can work at different frequency bands from 100MHz-5.8GHz. A band-pass ADC can be placed directly after the low-noise amplifier (LNA) in the receiver chain in re-configurable radios. A widely used ADC topology for direct sampling of IF and RF frequencies is the bandpass $\Delta\Sigma$ ADC architecture which allows high resolution. A fundamental limitation in the design of high-frequency $\Delta\Sigma$ ADCs is the need for high speed analog circuits which consume large power. InP and SiGe Bi-CMOS transistors have been used to design band-pass ADCs for digitizing intermediate frequencies (IF) [2]–[4], and direct RF sampling in the GHz ranges [5], [6]. Time interleaving provides a viable alternative to a high-speed single channel ADC by operating multiple ADCs at a lower frequency. Previous works based on time-interleaving have proposed various techniques to increase the overall sampling rate of the ADC in order to accommodate a larger input bandwidth [7], [8]. [9] proposes a time-interleaved $\Delta\Sigma$ VCO-based ADC architecture [10]–[12] which leverages lower operating frequency from time-interleaving to improve the ADC resolution, while simultaneously modifying the first-order noise transfer function (NTF) of the ADC from a high-pass to bandstop characteristic. However, [9] employs an open-loop VCO-based ADC which limits noise-shaping of each ADC to first-order.

We propose a time-interleaved 2nd-order $\Delta\Sigma$ bandpass ADC with four interleaved VCO-based ADCs. Apart from increasing the order of noise shaping, the proposed ADC also improves linearity due to feedback loop. Each sub-ADC comprises a VCO-based ADC based on a digital PLL architecture with current starved ring-oscillator as integrator which provides inherent multi-bit quantization and consumes low power and area. The proposed architecture obviates the need for op-amps, bulky passive components and does not require VCO non-linearity calibration or excess loop delay compensation. The proposed architecture also performs an intrinsic data weighted averaging on the static element mismatch present in the digital-to-analog converter (DAC), thereby high-pass shaping the DAC mismatch. The rest of the paper is organized as follows: the proposed time-interleaved ADC design is discussed in Section II, with simulation results in Section III and conclusion in Section IV.

II. Proposed Architecture

A. Circuit Design

Fig. 1 depicts the proposed time-interleaved ADC architecture. Each sub-ADC comprises a VCO-based ADC operating at a sampling frequency of f_s/N where N is the number of interleaved ADCs. The required clock phases for interleaving the four ADCs are generated on-chip by a clock generator comprising a LVDS receiver, clock divider and high strength buffers for driving each sub-ADC. Each of the clocks are phase shifted by 90°, and have 50% duty cycle. During the rising edge of the clock (ϕ_1), each ADC sees the input signal and quantizes it. After quantization of the input signal, the output from the interleaved ADCs are multiplexed at a frequency of f_s. Architecture of VCO-based ADC is discussed in more detail in [13]. This paper further extends upon the idea presented in [13] by time interleaving four VCO-based ADCs and operating them in four distinct phases thereby improving the effective sampling rate of the overall ADC. Each sub-ADC high-pass shapes the quantization noise to second-order owing to two integrators in the signal chain (see Fig. 1). Both the VCO and SRO comprises a 13-stage pseudo-differential current starved ring oscillator, in a fully differential configuration. The phase difference between the differential VCOs is subtracted with a tri-state phase frequency detector (PFD), and the SRO is switched between two current sources, I_{H} and I_{L}, depending on the polarity of the PFD output. Since the SRO only switches between two frequencies, it has very high linearity. The sub-ADC consists of a non-return to zero (NRZ) DAC. Owing to the intrinsic barrel shifting pattern at the SRO output, static element mismatch of the DAC is high-pass shaped [14].

Even though the sub-ADC has relaxed linearity requirements owing to the feedback loop, careful design considerations should be made while designing the sub-ADC as it

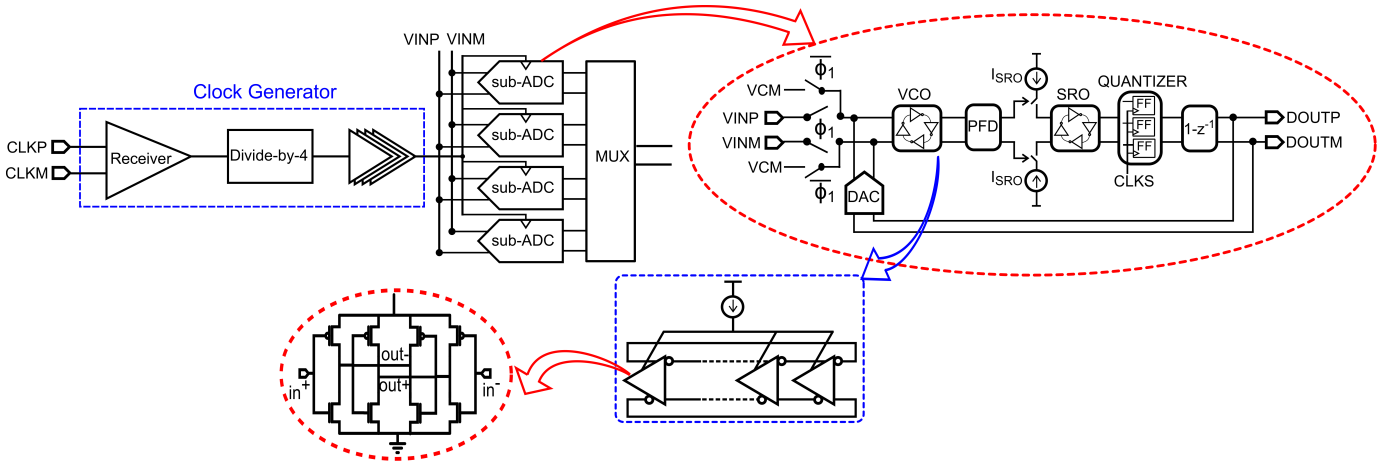

Fig. 1. Architecture of the proposed TI ADC

has a direct effect on the overall performance of the time-interleaved ADC. A key stability constraint in the design of sub-ADC is to prevent PFD and SRO overflow during any sampling period. The stability bound for the SRO can be represented mathematically as $\{(I_{\rm H} - I_{\rm L}) \cdot k_{sro} \cdot T_s \leq 0.5\}$ where k_{sro} denotes the SRO gain. For the PFD to not overflow, the VCO input swing, which is determined primarily by the out-of-band quantization noise, has to be within a certain limit. The LSB step size of the quantizer, $2 \cdot I_{\rm DAC}$, is determined on the basis of behavioral simulations such that the PFD input phase does not exceed $[-2\pi, 2\pi]$. It has been shown in [13], by choosing the VCO and SRO gains carefully, the sub-ADC loop obviates the need for an auxiliary DAC for excess loop delay compensation. Since each sub-ADC operates at 100MHz, the effective sampling rate (f_s) of the entire ADC is 400MHz, allowing, the ADC to quantize signals around DC, 100MHz and 200MHz. Each sub-ADC only sees the input during the ϕ_1 phase. In order to conserve power, during $\bar{\phi_1}$ phase, each sub-ADC sees the common-mode voltage and runs at a very low center frequency.

B. SNR Analysis

The primary sources of noise in each sub-ADC arise from the VCO, DAC, and quantization noise. Thermal noise from the VCO and DAC can be estimated by referring the phase noise of the VCO to the input. Hence, input-referred thermal noise arising from the VCO and DAC is represented as;

$$\sqrt{\overline{i_{th,n}^2}} = \sqrt{2} \cdot \frac{\sqrt{2Dt_s}}{2\pi k_{vco} t_{vco}} \cdot \frac{1}{\sqrt{OSR}}$$

where t_s is the sampling period, D is the phase diffusion constant of the VCO [15] during the ϕ_1 phase. D can be estimated as $D = \left\{\mathcal{L}(\Delta\omega) \cdot (\Delta\omega)^2\right\}/2$. At a sampling frequency of 102.4MHz, OSR of 30, k_{vco} of 4MHz/μA, the input referred thermal noise is 1.17nA,rms. Input referred quantization noise is given by;

$$\sqrt{\overline{i_{q,n}^2}} = \frac{2I_{\rm DAC}}{N_1} \cdot \frac{\pi}{\sqrt{5}} \cdot OSR^{-5/2}$$

where N_1 is the number of stages of the VCO. At an OSR of 30 and $I_{\rm DAC}/N_1$ of 1μA, the input referred quantization noise is 0.16nA,rms. The PMOS tail current source has a g_m of 240μS. Thus, the total input-referred noise is 4.9μV. Above calculations reveal that input referred thermal noise is dominated by VCO and DAC, since, most of the in-band quantization noise has been high-pass shaped to second-order. For an input of 18mV$_{\rm pk\text{-}pk}$, the SNR is calculated to be 61.5dB.

III. Simulation Results

Preliminary simulations were performed on the proposed time-interleaved ADC using Matlab Simulink and Spectre. A 13-stage VCO with a gain k_{vco}=4MHz/μA was used in the ADC. All simulation results are taken from a 2^{11} point FFT of the ADC output spectrum. Initial simulations estimated the robustness of the proposed ADC to mismatches that would occur during fabrication, namely, timing mismatches and gain mismatches. The most probable sources of timing mismatches that can occur in the circuit are (i) DAC jitter and (ii) timing mismatches in the clock path. Fig. 2 depicts

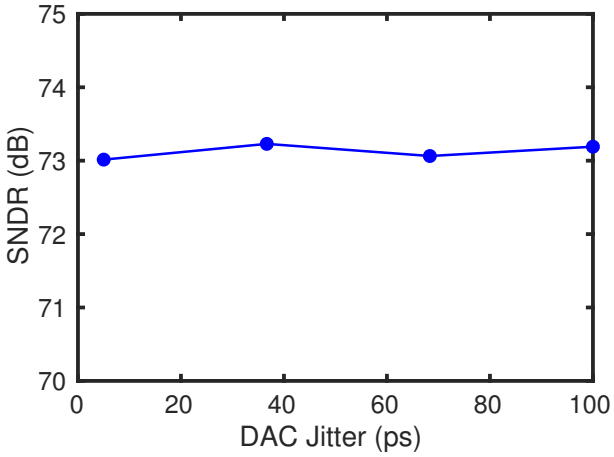

Fig. 2. DAC jitter v/s SNDR

the variation of SNDR w/r to DAC jitter in the proposed ADC, and it can be inferred from the plot that the SNDR

remains fairly constant when DAC jitter is swept from 5ps - 100ps. Another source of timing mismatch in time-interleaved ADC, is timing mismatch in the clock distribution path to each ADC, due to unequal gate delay in the clock path and RC delay present in the wires. Variations in sampling clock edges cause mismatches leading to improper sampling and re-combination of the outputs from the interleaved ADCs. Mismatches in interleaving cause improper cancellation of the higher order aliases of the input which show up as images in the signal band degrading the SNDR. Fig. 3 depicts the effect of timing mismatch on the performance of the proposed ADC. By sweeping the timing mismatch from 1ps - 5ps, it can be observed the SNDR reduces sharply, hence, careful design considerations must be made while doing the layout of the ADC to prevent timing mismatches in the clock path.

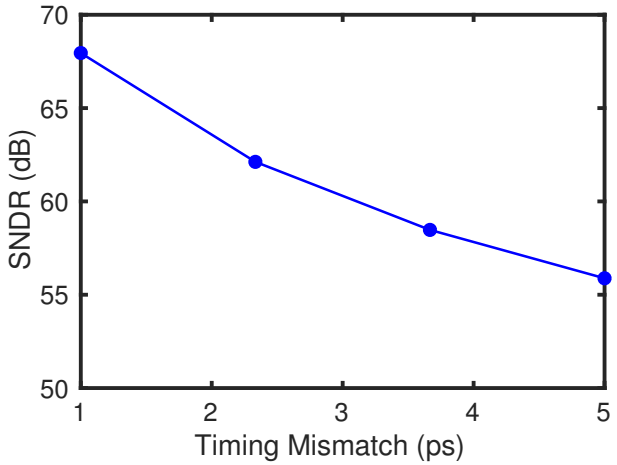

Fig. 3. Timing mismatch v/s SNDR

Once the proposed architecture was validated and optimized using Matlab, a transistor level design was implemented in Cadence, using 65nm technology and simulations were performed to further characterize the ADC. The time-interleaved ADC consumes 0.44mW from a 0.85V supply while operating at a sampling frequency of 409.6MHz, with a bandwidth of 3.4MHz. The ADC was tested at two input frequencies of 350KHz and 102.05MHz. Fig. 4 depicts the output spectrum of the ADC at the frequency of 102.05MHz. The second-order bandstop noise shaping can be clearly observed. Quantization noise, $1/f$ noise and thermal noise were the sources of noise considered during simulations. Fig. 5 shows the noise transfer function of the proposed time-interleaved ADC. Fig. 6 shows the input amplitude v/s ADC SNDR. The ADC dynamic range was calculated to be 61dB. To suppress timing mismatch, we use an analog background calibration technique using variable delay lines (VDL). The timing calibration unit consists of a fine and coarse delay tuning line, consisting of capacitors controlled by digital words. The VDL is used to control the timing of the rising edges of the clocks which are critical to the performance of the ADC. Gain calibration is performed by a foreground optimization algorithm which minimizes the in-band distortions that degrade the SNDR of the ADC. Fig. 7 depicts the output of the time-interleaved ADC with

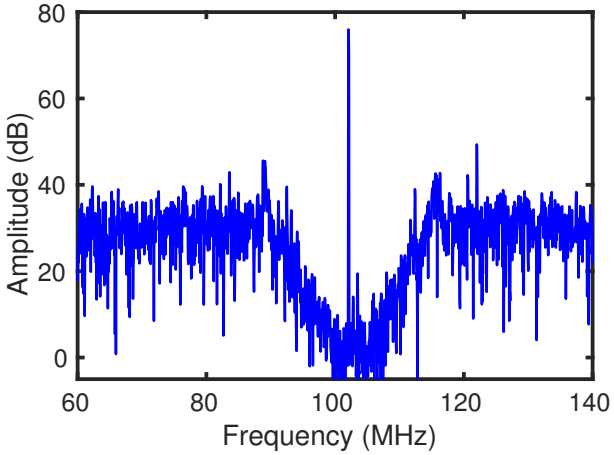

Fig. 4. ADC output spectrum at f_{in}=102.05MHz

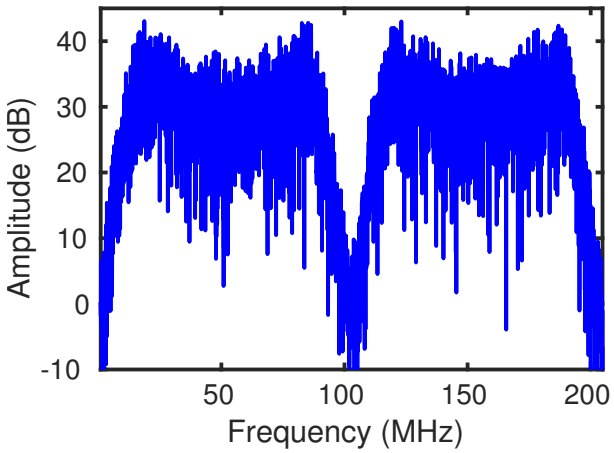

Fig. 5. NTF of proposed time-interleaved ADC

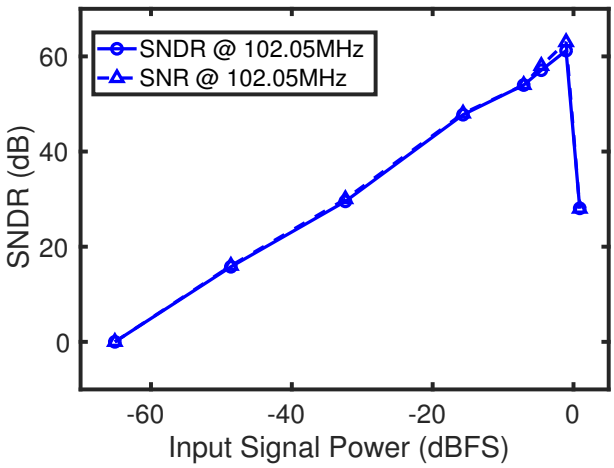

Fig. 6. SNDR/SNR v/s input amplitude sweep

a 18mV$_{pk-pk}$ input and gain mismatch with σ=5%. It can be observed that after calibration there is a significant attenuation in the harmonics caused due to gain mismatches across the four interleaved ADCs. Further simulations were performed to test the robustness of the proposed gain calibration algorithm in correcting gain mismatches in the proposed time-interleaved ADC. Fig. 8 shows the variation in SNDR with gain mismatch

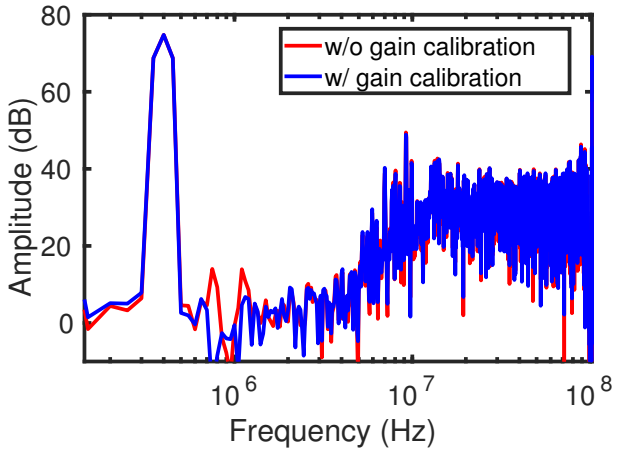

Fig. 7. ADC output spectrum with 18mV$_{pk-pk}$ input

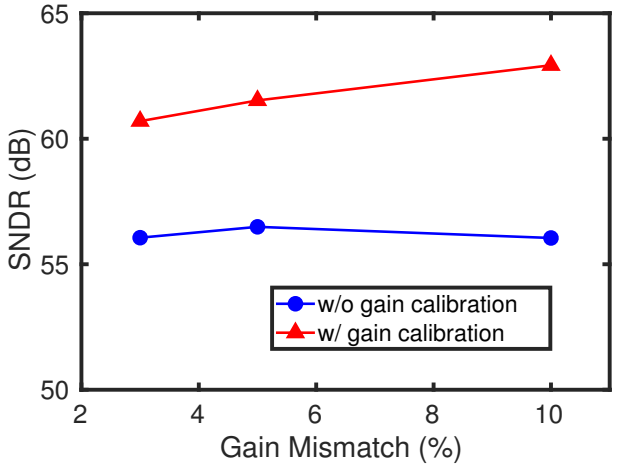

Fig. 8. ADC SNDR v/s gain mismatch

standard deviation swept from 3% - 10%. Simulation results indicate an improvement of 4-5dB in SNDR owing to our proposed gain mismatch calibration algorithm.

Table I presents a performance summary of the proposed time-interleaved ADC and comparison with prior art.

TABLE I
PERFORMANCE SUMMARY & COMPARISON TO PRIOR ART

	JSSC '07 [6]	VLSI '09 [9]	TCAS-I '15 [4]	**This Work**
Process	0.25μm	65nm	180nm	65nm
Type	4th-order G_m-LC $\Delta\Sigma$	Time-based	SC $\Delta\Sigma$	DPLL-based
f_{center}	2.4GHz	1.5GHz	50MHz	102.4MHz
f_s	3.8GHz	4GHz	200MHz	400MHz
SNR	59dB @ 1MHz	63.3dB @ 1MHz	61.3dB @ 2MHz	65dB @ 350KHz
SNDR	62dB @ 200KHz	41.5dB @ 1MHz	50.2dB @ 2MHz	61dB @ 350KHz
Power	75mW	19.6mW	2mW	0.44mW
FoM$_w$(pJ)/step	182	6.7	0.64	0.06

IV. Conclusion

This paper has presented a VCO-based time-interleaved second-order $\Delta\Sigma$ ADC with bandstop noise shaping characteristic. The proposed architecture derives its highly digital nature from the DPLL architecture, does not employ op-amps or bulky passive components, thus consuming low-power and area. The proposed ADC can be used for multi-configurable radio purposes which require quantization of signals at DC and hundreds of MHz. The proposed TI ADC lends itself to technology scaling owing to its highly digital architecture and it is also expected to have better performance at lower technology nodes due to better time-resolution.

V. Acknowledgment

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