# 2nd-Order VCO-based CT $\Delta\Sigma$ ADC Architecture

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***Abstract*—This paper proposes a novel architecture for purely voltage controlled oscillator (VCO) based continuous-time (CT) second-order $\Delta\Sigma$ analog-to-digital converter (ADC) without using bulky, passive components. The proposed technique does not require any VCO nonlinearity calibration and is robust against excess loop delay and static and dynamic errors in the multi-element digital-to-analog converter (DAC). Behavioral simulations have been performed to validate the proposed architecture.**

## I. Introduction

As internet-of-things (IoT) is set to expand rapidly over the next few years, there is a growing need to have high resolution analog-to-digital converters (ADCs) with low power and area consumption. A solution is to have highly digital continuous-time (CT) $\Delta\Sigma$ ADCs that can fully leverage CMOS technology scaling. However, conventional voltage-domain (VD) $\Delta\Sigma$ ADCs use opamps as integrators which are challenging to design in scaled CMOS technologies where both transistor intrinsic gain and voltage headroom are reduced. To address this issue, time-domain (TD) signal processing can be used in which excursions in VD are transformed to TD before quantization. A TD integrator can be implemented using a ring inverter based voltage controlled oscillator (VCO) which is highly digital and can work with low supply voltages. Not surprisingly, VCO-based ADCs have seen a lot of interest from the research community over the years [1]–[9]. However, VCO-based ADC is nonlinear and has a gain (Kvco) which is highly sensitive to process, voltage and temperature (PVT) variations. A classic technique to address VCO nonlinearity and PVT sensitivity is to embed the VCO inside a loop with high linear gain [2], [4]. Active opamp based integrators are typically used to achieve high loop gain which makes this approach less appealing for scaled CMOS technologies. [1], [3] uses digital background calibration to solve VCO nonlinearity but relies on replica matching which is difficult to guarantee in advanced technology nodes. Another technique is to use a two-stage architecture in which the first stage does a coarse quantization of the input [4]–[7] and a VCO-stage performs fine quantization on the residue from first stage. The VCO sees only the reduced swing residue of the first stage and does not require nonlinearity calibration. To address interstage gain variation with PVT, either the entire ADC is embedded in a high gain loop requiring opamps [4], or digital calibration is used [7].

Inspite of the tremendous progress made in TD $\Delta\Sigma$ ADC research, most TD $\Delta\Sigma$ ADCs only shape quantization noise to the first order. Higher-order noise shaping results in higher signal-to-quantization noise ratio (SQNR) and is key to achieving high ADC resolution. Typically higher-order noise shaping is achieved by cascading a VCO with opamp based integrators. There have been attempts to have higher-order, VCO-based $\Delta\Sigma$ ADCs without using opamps [8]–[11]. Passive integrator is used to achieve second-order noise shaping in [8], [10] which prevents higher order noise shaping at low frequencies and increases ADC area. While the MASH structure in [9] achieves third-order noise shaping, it requires complicated circuits with stringent timing considerations that are not trivial to satisfy. The work in [11] achieves second-order noise shaping with two VCO-based integrators at the cost of additional hardware and lower VCO linearity.

A second-order CT $\Delta\Sigma$ VCO based ADC architecture is presented in this paper. The proposed ADC is based on a digital phase-locked loop (DPLL) architecture and does not require any opamp. The proposed architecture does not require bulky passive components. The PLL loop obviates the need for VCO nonlinearity calibration. In addition, the proposed CT ADC is very robust against excess loop delay (ELD), and static and dynamic mismatches in the multi-bit digital-to-analog converter (DAC). A preliminary concept of the proposed architecture was presented in [12]. In this paper we have included a more detailed analysis of the proposed architecture as well as adding new discussion on techniques to counter ELD and errors in the DAC. The rest of the paper is organized as follows: the proposed ADC design is presented in Section II, the simulation results are presented in Section III and the conclusion is brought up in Section IV.

## II. Proposed Architecture

Fig. 1 shows the architecture of the proposed ADC. The motivation behind the proposed architecture can be appreciated by taking a look at PLL behavior. Under locked condition, if a phase/frequency shift is introduced in the VCO, the PLL will change the VCO control voltage to correct for the shift. Extending this idea, if a sinusoidal voltage is injected into the VCO of a locked PLL, the control voltage will be another sinusoidal voltage shifted in phase by $180°$, provided the injected signal does not cause the PLL to lose lock. If the control voltage is digitized, the PLL can act as an ADC with the injected signal as the input and the digitized control voltage as the output of the ADC. This idea forms the basis of the architecture presented in this paper. As shown in Fig. 1, two differential inputs are injected into the VCOs. A phase/frequency detector (PFD) digitizes the phase difference between the two VCOs. A switched-ring oscillator (SRO)

integrates the PFD output by switching between two current sources depending on the polarity of the PFD output. The output of the SRO is quantized, digitally differentiated, added with the input signal through a multi-bit DAC and fed back to the VCO. Second-order noise shaping is achieved as the loop contains two integrators in the form of VCO and SRO. As the VCO is embedded in a loop, the VCO sees a reduced input swing which significantly reduces its nonlinearity. The proposed architecture is also quite robust against mismatches between the input VCOs and any mismatch between the input VCOs is suppressed by the loop gain.

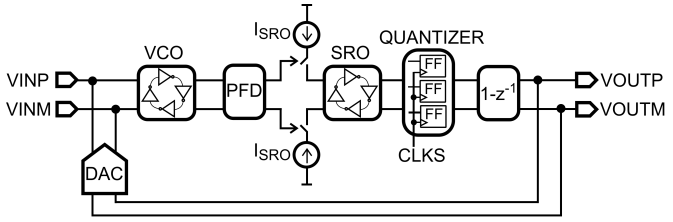



Fig. 1. Proposed second-order VCO-based ADC based on modified DPLL

### A. Frequency Domain Analysis

Figure 2 shows the frequency-domain model of the proposed second-order architecture. A single-ended model is shown for the sake of simplicity. The SRO and VCO gains are denoted by $k_{vco}$ and $k_{sro}$ respectively. The PFD is modeled by a linear subtractor in phase domain with a gain of $T_s/2\pi$. The sampling operation after the SRO is modeled by a gain of $1/T_s$. The multi-bit quantizer is assumed to have a gain of $M$ and the DAC gain is modeled by $G$. Using impulse-invariance transform [13], the ADC output can be written as

$$D_{out} = \frac{-H\left(z^{-1}+z^{-2}\right)V_{in} + 2\epsilon\left(1-z^{-1}\right)^2}{2+(GH-2)z^{-1}+(GH)z^{-2}} \quad (1)$$

where $H = 2\pi k_{vco}k_{sro}I_{sro}MT_s^2$

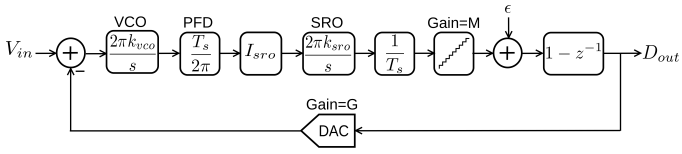



Fig. 2. Frequency domain model of second-order VCO based ADC

It can be seen from (1) that the low frequency quantization noise from the TDC is second-order shaped. This is different from the technique of [8], [10] which has first-order noise shaping at low frequencies. Thus, the proposed technique has lower in-band quantization noise than the technique of [8], [10]. Compared to [11], fewer DACs are required for the proposed technique which results in lower hardware complexity. In addition, feedback to the second VCO stage in [11], while improving stability, reduces the linearity of the ADC.

### B. DAC Design

DAC design is a critical challenge in a CT modulator design and requires a careful balance between clock jitter, static mismatch and dynamic error also known as inter-symbol interference (ISI) error. A multi-bit non-return-to-zero (NRZ) DAC is the best choice from clock jitter perspective. Also, a multi-bit DAC reduces the input swing seen by the VCO and relaxes its linearity requirement. However, multi-bit DAC suffers from static element mismatch which raises in-band noise floor and introduces harmonic distortion. ISI error, which is present in both single and multi-bit DACs, primarily arises from asymmetric rise and fall times of the digital signals driving the DAC. ISI error is proportional to the number of transitions in the DAC and nonlinearity due to ISI can be attributed to only the up-transition density given by $\Gamma[n] = D_{out}[n](1 - D_{out}[n-1])$ [14].

Digital differentiation at the SRO output applies the well known data-weighted averaging (DWA) on the DAC elements and first-order shapes static mismatch. Unfortunately, DWA also maximizes the number of transitions in the DAC, thus, exacerbating ISI error. A way to reduce ISI error is to reduce $\Gamma[n]$. We propose a dynamic element matching (DEM) technique in which $D_{out}[n]$ is converted into thermometer code but the start position of the thermometer code is advanced by 1 every cycle. Thus, the proposed DEM ensures that all DAC elements are used uniformly while maintaining a very low $\Gamma[n]$. The DAC element selection pattern for DWA and the proposed DEM are shown in Fig. 4. During any sample period, the selected DAC elements are shaded in blue. DWA cycles through the elements quickly by maximizing $\Gamma[n]$. The proposed DEM cycles through the DAC elements at a slower rate than DWA but has a much lower $\Gamma[n]$.

### C. Excess Loop Delay

Yet another source of non-ideality in CT modulators is excess loop delay arising out of quantizer delay as well as delay in latches. The effect of ELD, $\tau$, is analyzed using the technique in [13]. In presence of ELD, the ADC output can be written as

$$D_{out} = \frac{\left[\left(\alpha z^{-1}+\beta z^{-2}+\gamma z^{-3}\right)HV_{in} + \left(1-z^{-1}\right)^2\epsilon\right]}{1-(1+GH\alpha)z^1 - GH\beta z^{-2} - GH\gamma z^{-3}} \quad (2)$$

where $\alpha = -0.5 + \tau - 0.5\tau^2$, $\beta = \tau^2 - \tau - 0.5$, $\gamma = -0.5\tau^2$ ELD increases the modulator order from second to third which can potentially make the modulator unstable. Loop stability can be analyzed by looking at the poles of the noise transfer function (NTF) as a function of $\tau$ . As can be seen from (2), the NTF has 2 poles when $\tau$ = 0. As $\tau$ is increased, a third pole is introduced in the NTF and the NTF poles moves closer to the unit circle and eventually moves outside the unit circle. For a fixed $\tau$, increasing $k_{vco}$ and $k_{sro}$ also leads to the NTF poles moving outside the unit circle. Thus, $k_{vco}$ and $k_{sro}$ can be selected to ensure that the ADC does not become unstable for excess delay upto a full sampling clock cycle.

### D. Proposed ADC Circuit

Fig. 3 shows the circuit schematic for the proposed ADC. Two differential VCOs are injected with the differential inputs $V_{in}^+$ and $V_{in}^-$. The phase difference between the two VCOs is detected by the tri-state PFD which generates UP and DN signals such that the difference in pulse-width of UP and DN gives the phase difference between the two VCOs. The two

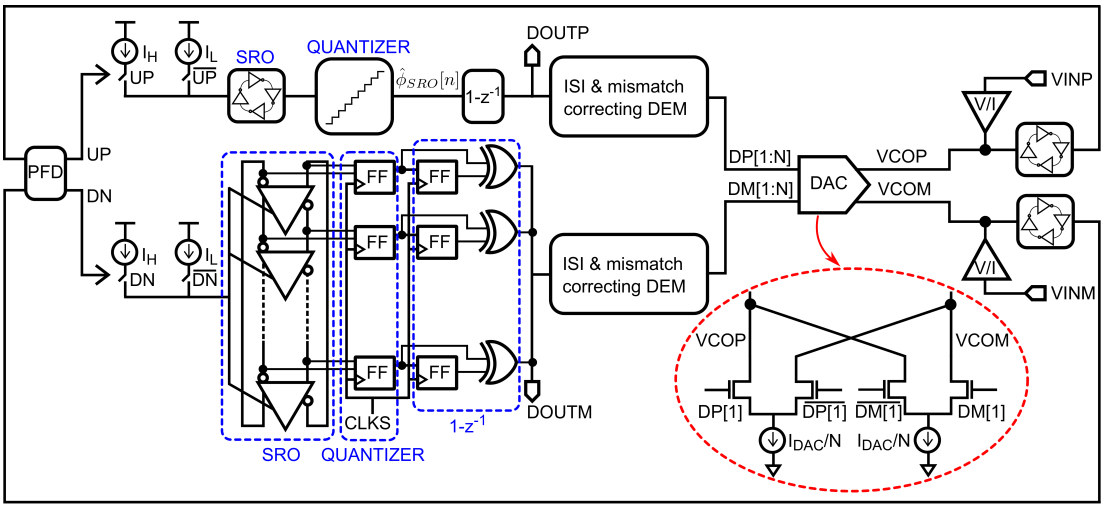



Fig. 3. Proposed second-order VCO-based $\Delta\Sigma$ circuit

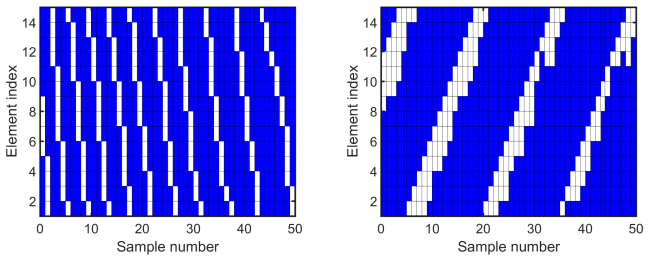



Fig. 4. Element selection pattern for (a)DWA, and(b)proposed DEM

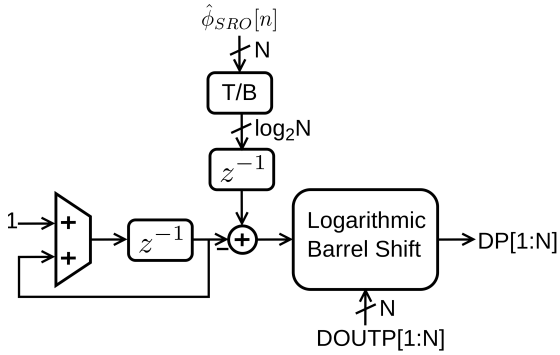



Fig. 5. Proposed ISI and mismatch correcting DEM

SROs are driven by the UP and DN signals respectively. Each SRO consists of an $N$-stage ring current controlled oscillator (CCO). The tail current to the SRO switches between two levels $I_H$ and $I_L$ depending on the input to the SRO. By operating the CCOs at only two frequencies, a high linearity from the SROs is ensured. To maintain the high linearity of the SRO, $k_{sro}$ has to be chosen to ensure that phase overflow does not occur between two consecutive sampling instants. The $N$-stage SRO quantizes the SRO phase $\phi_{SRO}$ into $2N$ levels. The quantized phase output of the SRO, $\hat{\phi}_{SRO}[n]$, is digitally differentiated using XOR gates, and is then fed back to the VCO inputs through differential DACs. The ISI and mismatch correcting DEM is shown in Fig. 5. T/B denotes thermometer-to-binary conversion. Digital differentiation of $\hat{\phi}_{SRO}[n]$ results in a barrel shifting pattern. A logarithmic barrel shifter is used to reverse the barrel shifting pattern. The amount of shifting required is generated by subtracting the output of a digital counter from the binary equivalent of $\hat{\phi}_{SRO}[n-1]$. The counter ensures that every cycle the start position of the thermometer coded DAC input is shifted by '1'. The logarithmic barrel shifter lies in the signal path and can be designed to work at high speed as it essentially consists of $\log_2 N$ transmission gates. The circuit used to generate the digital control word for the logarithmic shifter is outside the signal path and can use the full sampling period.

## III. Simulation Results

Behavioral simulations were performed on the second-order ADC to validate the proposed architecture. A 15-element SRO was used for the simulations. The VCO and TDC gains were chosen to be $k_{vco} = k_{sro}/g_m$ = 450MHz/V where $g_m$ is the transconductance of SRO tail current source. The VCO center frequency was set to 1GHz. An input signal with amplitude of $0.8V_{p-p}$ at a frequency of 0.23MHz was used. A power supply of 1V was used for the simulation. The ADC was sampled at 500MHz. Quantization noise was the only noise source considered for the simulation. $2^{16}$ point FFT of the ADC output is shown in Fig. 6. The second-order quantization noise shaping can be clearly seen. At an OSR of 32, the SQNR is 87 dB. To estimate the effect of ELD on stability, simulation was performed by varying both the ELD, $\tau$, and $k_v = k_{vco} = k_{sro}/g_m$. Fig. 7 shows the variation of SNDR with $\tau$ for different $k_v$ values. At higher values of $k_v$, the effect of excess loop delay is more pronounced and the modulator becomes unstable more quickly. For a $k_v$ of 450MHz/V, the $\Delta\Sigma$ modulator can tolerate a full cycle of excess loop delay. To prevent distortion due to input-dependent delay in the quantizer, the quantized output is resampled after half-cycle delay. Simulations were performed for different values of static mismatch and ISI errors to evaluate their effect on the multi-

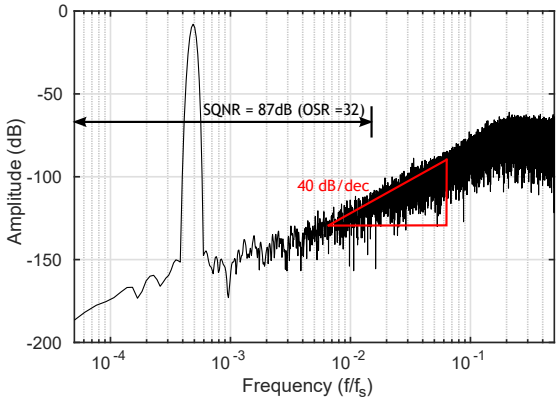
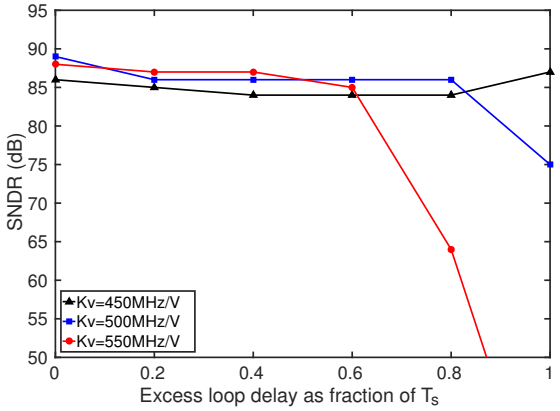



Fig. 6. $2^{16}$ point FFT of the proposed ADC




(a)

Fig. 7. SNDR variation with excess loop delay for different VCO gains

bit DAC. For all simulations, static mismatch was assumed to have a zero mean and its standard deviation, $\sigma_m$, was varied. The standard deviation of ISI error, $\sigma_{isi}$, was set to 10% and its mean ,$\mu_{isi}$, was varied. SNDR sweep vs input amplitude for varying static mismatch and ISI error is shown in Fig. 8. In the absence of any static mismatch and ISI error, the ADC has a peak SNDR of 87dB. With $\sigma_m = 2\%$ and $\mu_{isi} = 5\%$, the proposed DEM has an SNDR of 85dB which is 8dB better than DWA which has SNDR of 77dB. With $\sigma_m = 5\%$ and $\mu_{isi} = 2\%$, DWA has an improved SNDR of 80dB but the proposed DEM still achieves 2dB better SNDR than DWA. Thus, the proposed DEM achieves good suppression of both static mismatch and ISI error and outperforms DWA. While some of the more recent techniques [14] can achieve better suppression of both ISI and static mismatch, they have a much higher hardware cost than the proposed DEM. A prototype ADC designed in 65nm consumes 1mW of power and has a figure-of-merit of 50fJ/step.

## IV. Conclusion

This paper has presented a novel, purely VCO-based second-order continuous-time $\Delta\Sigma$ ADC. The proposed architecture is based on a DPLL architecture and is highly digital in nature. It is expected that the power consumption and performance of the proposed ADC will improve with technology scaling due to its highly digital nature. The proposed architecture can also be extended to develop higher-order ($> 2$) VCO-based $\Delta\Sigma$ ADCs.

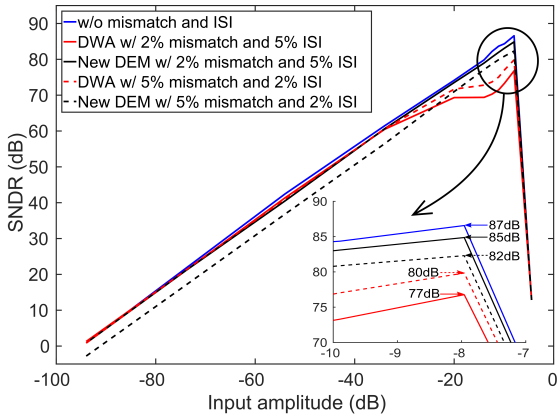



Fig. 8. DR for varying static mismatch and ISI error

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