Statistical estimator for simultaneous noise and mismatch suppression in SAR ADC

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A statistical estimator based on maximum-likelihood estimation theory is developed to simultaneously reduce capacitor mismatch and noise in a SAR ADC. After the SAR ADC has finished quantization, the residue voltage is available at the comparator input and is estimated accurately by using the statistical estimator. The ADC resolution is improved by subtracting the estimated residue from the digital output. The same technique of residue extraction is used to estimate mismatches in the capacitive DAC. This work shows a 7dB improvement in SNDR by using the statistical estimator for an 11-bit SAR over a wide range of capacitance mismatch and ADC noise.

Introduction: Successive approximation register (SAR) analog-to-digital converter (ADC) is widely used for medium resolution applications due to its very high energy efficiency and highly digital nature. While medium resolution SAR ADCs can have energy consumption as low as a few fJ for each conversion-step, energy efficiency of SAR ADCs reduces with increase in resolution. This is because at high resolutions, comparator thermal noise becomes the dominant noise source and requires 4X increase in power consumption for 1-bit increase in SAR resolution. A technique to address this issue is to add a second-stage after the SAR ADC [1]. The second-stage ADC quantizes the residue of the SAR stage, v_{res}, and subtracts it from the first stage output to digitize the analog input with better accuracy than the SAR stage alone. Since the second-stage quantizer cancels the quantization and comparator thermal noise of the SAR, a high resolution can be achieved with good energy-efficiency [1]. In principle, a separate quantizer is not required to digitize v_{res}. Once the SAR has finished quantization, v_{res} is available at the comparator input nodes. Hence, the SAR comparator itself can be used to digitize v_{res}. However, a single comparison is not going to yield a very accurate estimate of v_{res}. The presence of random noise at the comparator input ensures that if multiple comparisons are performed on v_{res}, a better estimate of v_{res} can be obtained by simple averaging or majority voting [2]. More recently, statistical estimation theory has been applied to digitize v_{res}. The technique in [3] uses maximum likelihood estimator (MLE) to digitize v_{res}. However, [3] uses 16 comparators for v_{res} estimation and it is not trivial to match offsets of all 16 comparators. The technique in [4] presents a Bayes estimator (BE) which performs better than the MLE technique proposed in [3], but requires prior knowledge of noise distribution at the comparator input. While adoption of low power switching techniques [5] and statistical estimation has improved SAR energy-efficiency significantly, further increase in energy efficiency can be achieved if size of the capacitive digital-to-analog converter (DAC) is reduced. Reducing DAC size comes with the penalty of increased capacitance mismatch. [6] presents a widely used technique to calibrate capacitance mismatches, but requires an additional sub-DAC. Other mismatch reduction techniques use perturbation-based digital background calibration [7] or inject pseudo-random sequences during comparator metastability periods to measure the distance between code-boundaries [8]. However, most previously reported techniques cannot address both noise and mismatch simultaneously. In this letter, we will present a statistical estimator which uses maximum likelihood estimation (MLE) to simultaneously suppress both noise and capacitor mismatch in SAR ADCs without any prior knowledge of noise distribution. The proposed estimator provides asymptotically unbiased and consistent estimation of v_{res}.

Proposed Architecture: Fig. 1 shows the architecture and mathematical model of the proposed technique. A single-ended circuit architecture is shown in Fig. 1(a) for simplicity. In Fig. 1(b), thermal noise from the comparator and kT/C sampling noise is represented by n_{th} at the ADC input, quantization noise is modeled by an additive error q_1 and δ denotes capacitor mismatch in the DAC. Using Fig. 1(b), d_{sar} and v_{res} can be calculated as

$$d_{sar} = V_{in} + n_{th} + q_1; \;\; v_{res} = d_{sar} + \delta - V_{in} \tag{1}$$

A maximum likelihood estimator is used to digitize v_{res} and capacitor mismatch δ and subtract them at the output. The final digital output is given as

$$d_{out} = d_{sar} - \hat{v}_{res} + \hat{\delta} = V_{in} + \epsilon \tag{2}$$

where ϵ is the estimation error of MLE. Thus, resolution of the ADC is determined solely by how accurately v_{res} and δ can be estimated.

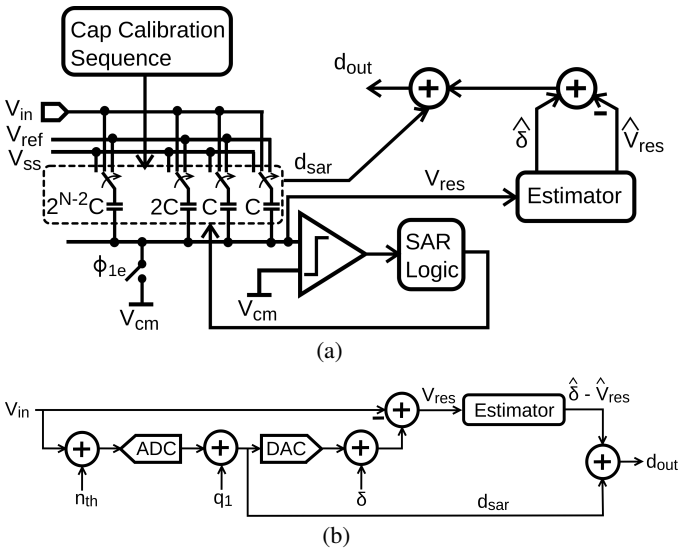

Fig. 1. (a) Circuit diagram, (b) mathematical model of proposed technique

Estimation of capacitor mismatch and noise: After the SAR ADC has finished quantization, v_{res} is available at the comparator's inputs. The comparator is fired M times and the comparator outputs $d_i (i \in [1, M])$, are passed to the estimator. The estimator's task is now to extract $\hat{v}_{res}$ from the distribution of d_i such that $\chi = (v_{res} - \hat{v}_{res})^2$ is minimized. The main challenge for applying MLE is how to define a likelihood function for the comparator. For each quantization, we modeled the likelihood function as the joint density of v_{res} and the comparator outputs $d_i (i \in [1, M])$:

$$L(v_{res}|d_1, d_2, ...d_M) = \frac{1}{\sqrt{2\pi\sigma_c^2}} \prod_{i=1}^{M} e^{\frac{(d_i - v_{res})^2}{2\sigma_c^2}} \tag{3}$$

where σ_c is the standard deviation of comparator noise. To minimize the error χ, the estimator maximizes the likelihood by following MLE theory and estimates $\hat{v}_{res}$ as:

$$\hat{v}_{res} = \arg\max L(v_{res}|d_1, d_2, ...d_M) \tag{4}$$

The effect of kT/C sampling noise is ignored in the calculation as for medium to high resolution SAR ADCs, comparator noise usually dominates kT/C noise.

In presence of mismatches in the DAC, each capacitor in the DAC array can be written as $C_i^{'} = C_i + \Delta C_i, \; i \in [1, N]$. The voltage error contributed by ΔC_i is given by

$$V_{\epsilon,i} = \frac{\Delta C_i}{\sum_{i=1}^{N} C_i^{'}} \cdot V_{ref} \tag{5}$$

The error due to capacitor mismatches can be written as $\delta = \sum_{i=1}^{N} V_{\epsilon,i} d_{sar,i}$. In order to estimate δ, a technique similar to [6] is used but without using any auxiliary sub-DAC. As an example, to estimate mismatch in the MSB capacitor, during the sampling phase of the ADC, V_{ref} is sampled on the MSB capacitor and '0' on all the other capacitors. During the quantization phase, the MSB capacitor's top-plate is tied to '0' and top-plate of all the other capacitors are tied to V_{ref}. Voltage error due to MSB capacitor mismatch, $V_{\epsilon,N}$, can be calculated from the residue voltage, $v_{res,N}$ at the comparator input and is estimated using MLE. The same technique is used for the other capacitors in the DAC and error

voltage due to mismatch in the i-th capacitor can be written as

$$V_{\epsilon,N} = \frac{v_{res,N}}{2};\ V_{\epsilon,i} = \frac{1}{2}\left(v_{res,i} - \sum_{j=i+1}^{N} V_{\epsilon,j}\right),\ i \in [1, N-1] \quad (6)$$

Thus, MLE can be used to extract capacitor mismatch in the DAC by providing estimates of $v_{res,i}$, ($i \in [1, N]$). Since, capacitor mismatch does not vary much with PVT, mismatch calibration can be performed once and the extracted mismatch values can be used for subsequent quantization operations.

Simulation Results: The capacitance mismatch and residue extraction algorithm was tested with an 11-bit SAR. A 1% capacitor mismatch was assumed. The comparator noise standard deviation, σ_c, was set to 0.65 LSB. After the SAR had finished quantization, the comparator was fired 20 times for estimation of v_{res} using MLE. 2^{13} point FFT of the ADC with and without MLE is shown in Fig. 2. Use of MLE improved the SNDR of the ADC from 57dB to 64dB and improved the SFDR by 10dB. The lowering of noise floor due to MLE can be clearly seen. Compared to [4], use of MLE to reduce both noise and capacitance mismatch results in a 2dB better SNDR.

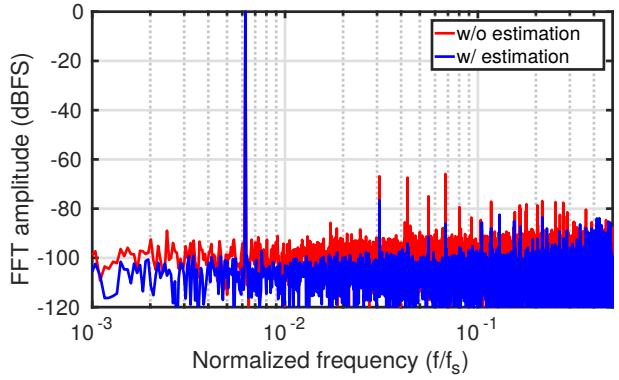

Fig. 2. Spectra of 11-b SAR ADC with and without estimation

Fig. 3 shows the SNDR variation with capacitance mismatch with and without using MLE. It can be clearly seen that use of MLE results in a consistent improvement in SNDR of around 7dB over a wide range of capacitance mismatch.

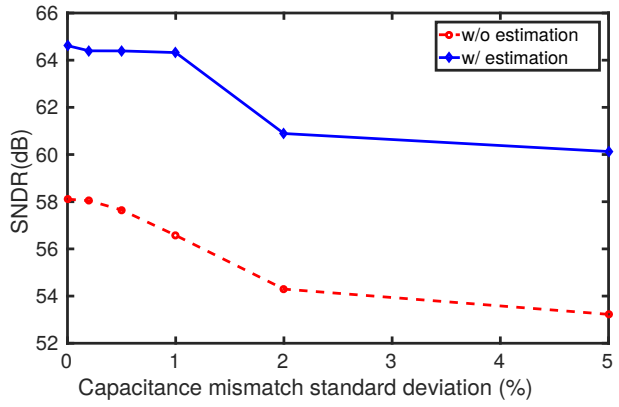

Fig. 3. SNDR versus capacitance mismatch

Use of MLE allows significant reduction in comparator and DAC switching power. To achieve the same SNDR without using MLE requires 7dB reduction in comparator noise power which necessitates a σ_c of 0.13 LSB. To reduce the comparator noise from 0.65 LSB to 0.13 LSB requires 25 times increase in comparator power. For an 11-bit SAR, the unit capacitor requires a matching accuracy of at least 0.5%. However, as can be seen from Fig. 3, use of MLE relaxes the capacitor matching accuracy to 1% which allows 4 times reduction in unit capacitor size, thus reducing the DAC switching power by 4. Thus, the overall ADC power can be greatly reduced through simultaneous reduction in capacitor mismatch and ADC noise using MLE. As an example, an 11-bit SAR ADC, with SNDR of 64dB, designed in 40nm CMOS process consumes 292μW power of which the comparator consumed 256μW and the DAC consumed 28μW. The DAC had a matching accuracy of 0.3%. Use of MLE reduces the comparator power to 10.2μW and the DAC switching power to 2.5μW, thus reducing the overall ADC power by a factor of 14. Firing the comparator for an additional 20 times will reduce the sampling speed by roughly a factor of 2.5, but that is not a major issue for most low speed bio-medical applications which can trade-off speed for lower power and higher resolution.

A pertinent question that arises here is since the estimation accuracy depends on the comparator noise standard deviation, (see (3)), how accurate will the estimation be as σ_c varies with PVT. Fig. 4 shows the improvement in SNDR by using MLE as σ_c is varied from 0.3 LSB to 1 LSB. As is expected, if σ_c is very small, multiple comparisons will not yield much information about the residue and the estimation accuracy will be low. Once σ_c is over 0.5 LSB, MLE results in a consistent 7dB better SNDR than without estimation.

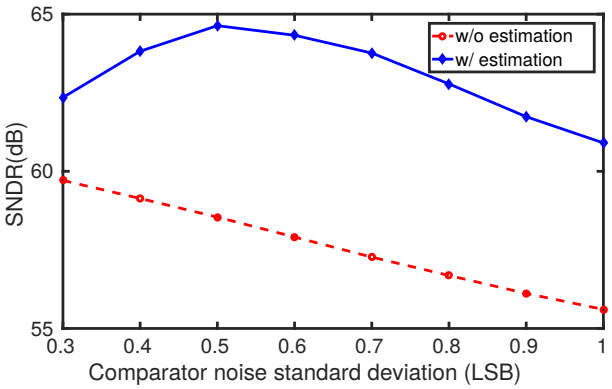

Fig. 4. SNDR versus comparator noise

Conclusion: This work has presented a statistical estimation technique based on MLE for reducing both noise and capacitance mismatch in a SAR ADC. The use of MLE results in 7dB improvement in SNDR for an 11-bit SAR ADC, or equivalently, for the same resolution MLE results in lowering of the 11-bit SAR ADC power by 14 times.

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References

1 Sanyal, A. and Sun, N.: 'A 18.5-fJ/step VCO-Based 0-1 MASH $\Delta\Sigma$ ADC with Digital Background Calibration', *IEEE Sym. VLSIC.*, 2016, pp. 26–27.

2 Harpe, P., Cantatore, E. and van Roermund, A.: 'A 10b/12b 40kS/s SAR ADC with data-driven noise reduction achieving upto 10.1b ENOB at 2.2fJ/conversion-step', *IEEE JSSC.*, 2013, **48**, pp. 3011–3018.

3 Verbruggen, B., Tsouhlarakis, J., Yamamoto, T., Iriguchi, M., Martens, E. and Craninckx, J.: 'A 60dB SNDR 35MS/s SAR ADC with comparator-noise-based stochastic residue estimation', *IEEE JSSC.*, 2015, **50**, pp. 2002–2011.

4 Chen, L., Tang, X., Sanyal, A., Yoon, Y., Cong, J. and Sun, N.: 'A 10.5-b ENOB 645nW 100kS/s SAR ADC with statistical estimation based noise reduction', *IEEE CICC.*, 2015, pp. 1–4.

5 Sanyal, A. and Sun, N.: 'An energy-efficient, low frequency-dependence switching technique for SAR ADCs', *IEEE TCAS–II.*, 2014, **61**, pp. 294–298.

6 Lee, H.-S., Hodges, D. A. and Gray, P. R.: 'A self-calibrating 15 bit CMOS A/D converter', *IEEE JSSC.*, 1984, **19**, pp. 813–819.

7 Liu, W., Huang, P., and Chiu, Y.: 'A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration', *IEEE JSSC.*, 2011, **46**, pp. 2661–2672.

8 Chen, L., Ma, J., and Sun, N.: 'Capacitor mismatch calibration for SAR ADCs based on comparator metastability detection', *IEEE ISCAS*, 2014, pp. 2357–2360.