

A 18.5-fJ/step VCO-Based 0-1 MASH $\Delta\Sigma$ ADC with Digital Background Calibration

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Abstract

A scaling-friendly and energy-efficient 0-1 MASH $\Delta\Sigma$ ADC is proposed in this work. An 8b SAR is used as the 1st stage for coarse quantization. A ring VCO is used as the 2nd stage for fine quantization. The proposed ADC uses digital background calibration to track VCO gain variation across PVT. A 40nm CMOS prototype achieves a Walden FoM of 18.5 fJ/conv-step while operating from 1.1V supply.

Introduction

With technology scaling, traditional voltage-domain ADCs face severe challenges due to reduction in transistor intrinsic gain and supply voltage. This has brought to the fore time-domain (TD) quantizers which can leverage technology scaling to build high performance ADCs. Ring VCO is widely used as a TD ADC due to its highly digital nature and simplicity of design [1]-[6]. It also provides an intrinsic 1st-order noise shaping. However, the VCO's frequency tuning gain is nonlinear and highly sensitive to PVT variations, which significantly undermines the ADC accuracy and robustness. In addition, FoMs of existing VCO-based ADCs are around 100-fJ/step [1]-[6], which presents a scope for improvement.

This work presents a scaling-friendly and energy-efficient 0-1 MASH $\Delta\Sigma$ ADC. It combines a coarse SAR with a fine VCO. The VCO is effective at quantizing small voltages in TD. Since the VCO only sees a small SAR residue, the VCO nonlinearity is greatly suppressed and does not need any correction. The PVT variation of the VCO tuning gain can still cause SAR quantization noise leakage, degrading SNDR. To address this issue, a simple, low-power, and fast-convergence digital background calibration technique is developed. It enables the precise tracking of the VCO gain and high ADC linearity. A prototype in 40nm CMOS achieves 74.3 dB SNDR with a BW of 2MHz while consuming only 350 μ W.

Proposed SAR-VCO 0-1 MASH $\Delta\Sigma$ ADC

Fig. 1 shows the architecture of the proposed ADC. During Φ_1 , the input is sampled across the bottom-plates of the DAC array. During Φ_2 , the sampled input is quantized by the SAR. The residue is fed to a pseudo-differential dual-VCO at Φ_3 . The VCO performs phase domain integration, and the output is differentiated digitally before being combined with the SAR output to generate the ADC output. To reduce power consumption of the SAR, the bi-directional single-sided switching scheme of [7] has been adopted. The SAR DAC has no redundancy as the VCO can absorb SAR decision errors as long as they are not too large to result in VCO phase overflow. This relaxes the precision requirement of the SAR comparator and saves power. The SAR in turn reduces the VCO swing and obviates the need for any VCO nonlinearity calibration.

Fig. 2 shows the circuit diagram of the 2nd stage VCO. Each VCO consists of a 7-stage pseudo-differential ring inverter chain. Although the VCOs quantize the SAR residue V_{res} only during Φ_3 , they are not stopped when Φ_3 goes low. This is to prevent charge leakage which can corrupt the phase information held by the VCOs. Instead, the VCOs are biased with I_{cm} and run at a fixed frequency during Φ_3 , which is kept low to save power and reduce phase noise. The digital logic for

the 2nd stage runs at the ADC sampling frequency. There is no phase-overflow counter running at high VCO frequency, which significantly lowers the power consumption of the 2nd stage compared to [6].

Fig. 3 shows the ADC model, where G represents the SAR residue voltage attenuation due to parasitic capacitors, K_{VCO} is the VCO tuning gain, G_d is the digital gain, and Rn is a dither. The ADC output can be derived as:

$$d_{out} = V_{in} + (q_1 - Rn) \left(1 - \frac{GK_{VCO}}{G_d} \right) + \frac{q_2(1 - z^{-1})}{G_d}$$

Both Rn and SAR conversion error q_1 can be cancelled if G_d matches the analog inter-stage gain GK_{VCO} . The cancellation of SAR error allows the use of a low power comparator. The final quantization noise at the ADC output d_{out} comes solely from the VCO (q_2) and is first-order shaped.

The VCO gain K_{VCO} is sensitive to PVT variations and can cause mismatch between G_d and GK_{VCO} , leading to noise leakage. To solve this issue, an efficient and fast background calibration technique is developed to precisely track the inter-stage gain GK_{VCO} . An *on-chip* pseudo-random number generator (PRNG) injects a dither Rn into the SAR DAC. GK_{VCO} is extracted from the difference between the d_2 averages for $Rn=1$ and $Rn=0$ [8]. The hardware cost of this background calibration scheme is low. It requires only an extra LSB capacitor in the DAC, two digital averagers, a MUX, and a subtractor (see Fig. 1). Its convergence speed is very fast. This is because the unknown ADC input V_{in} , which is the primary source of perturbation in the background calibration loop, is substantially attenuated by the 1st-stage 8-b SAR [9]. The part in d_2 that is uncorrelated with Rn is very small.

Measurement Results

The proposed ADC is implemented in 40nm CMOS. Fig. 4 shows the measured spectrum with a 2.2V differential input at 500kHz and the sampling frequency of 36MHz. Calibration improves the SNDR from 64.5 dB to 74.3 dB at the OSR of 9. The ADC consumes 350 μ W. Fig. 5 shows the SNDR and SNR sweep versus input amplitude. The ADC has a dynamic range of 75.7 dB. The measured histogram of d_2 is shown in Fig. 6. The shift in d_2 distributions from $Rn=1$ to $Rn=0$ can be clearly seen, and the difference of the two averages gives the inter-stage gain GK_{VCO} of 1.3. Fig. 7 shows that the proposed background calibration has a very fast convergence speed and requires only 10^3 samples (or 25 μ s) to converge. Fig. 8 shows the die photo. Table I compares the proposed hybrid SAR-VCO ADC with state-of-the-art VCO-based ADCs. It can be seen that this work has a FoM of 18.5 fJ/conv-step which represents a significant improvement over the prior art.

References

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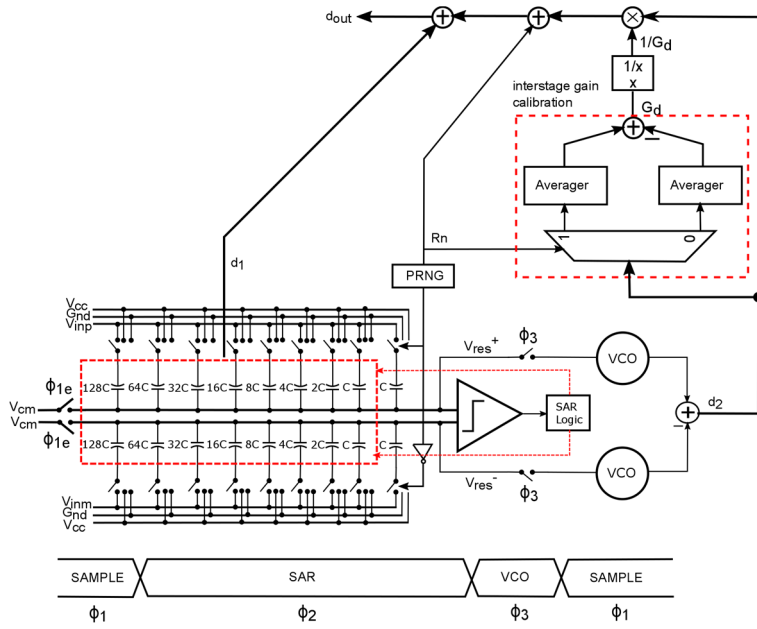


Fig. 1. Circuit diagram of the proposed ADC.

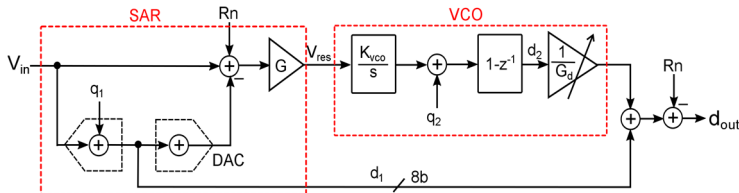


Fig. 3. Block diagram of the proposed ADC.

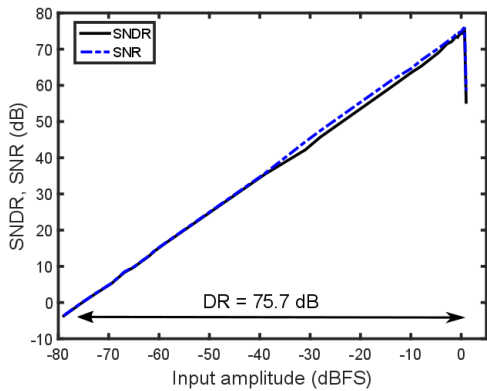


Fig. 5. Measured SNDR and SNR vs input amplitude.

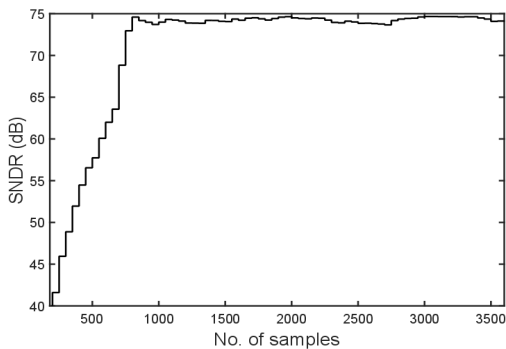


Fig. 7. Measured SNDR convergence curve.

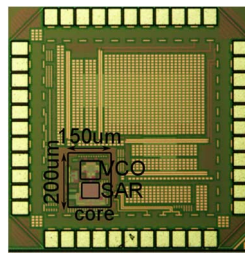


Fig. 8. Die photo

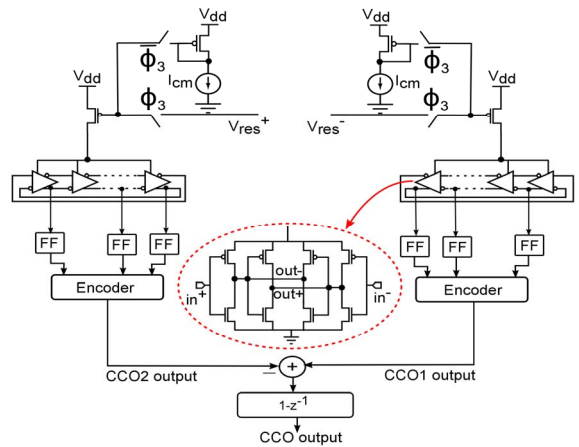


Fig. 2. Circuit diagram showing the 2nd stage VCO.

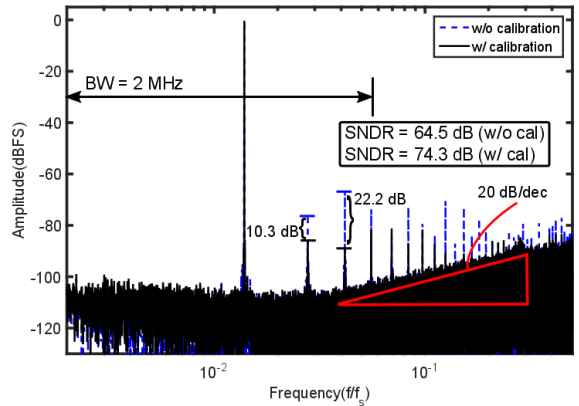


Fig. 4. Measured ADC spectrum with and without calibration.

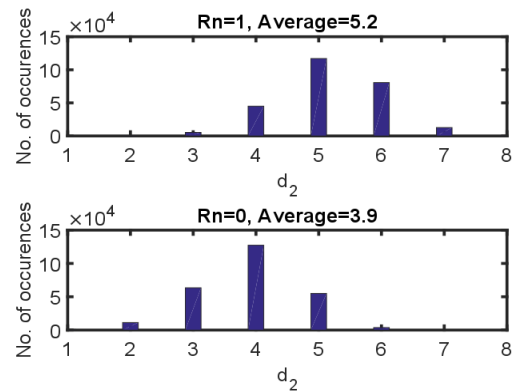


Fig. 6. Measured d_2 histogram for $R_n=1$ and $R_n=0$.

Table I. Performance summary and comparison.

	[2]	[3]	[4]	This work	
Process (nm)	65	90	90	40	
Power (mW)	11.5	16	4.1	0.35	
Area (mm ²)	0.07	0.36	0.16	0.03	
f_s (MHz)	1300	600	640	36	
BW (MHz)	5.1	10	5	3	2
SNDR (dB)	75	78.3	74.7	71.4	74.3
FoMs (dB) ¹	161	163	165	171	172
FoM _w (fJ/step) ²	246	120	92	18.5	21.3

¹FoM_S = SNDR + 10log₁₀(BW/Power)

²FoM_w = Power/(2*BW)/2^{ENOB}