# Dynamic Element Matching With Signal-Independent Element Transition Rates for Multibit $\Delta\Sigma$ Modulators

Arindam Sanyal, *Student Member, IEEE*, Long Chen, *Student Member, IEEE*, and Nan Sun, *Member, IEEE*

***Abstract*—This paper presents a novel dynamic element matching (DEM) technique for multi-bit $\Delta\Sigma$ digital-to-analog converters (DACs). The proposed technique can address errors due to both static element mismatch and dynamic inter-symbol-interference (ISI). The proposed technique ensures no ISI-induced distortion even at large signal amplitudes by de-correlating the instantaneous number of DAC transitions from the signal. It can shape the total number of transitions and whiten the individual transition sequence, thereby significantly reducing the in-band ISI errors. The proposed technique can be easily extended to higher-order shaping for both static mismatch and ISI errors. An efficient hardware implementation based on the vector-quantizer mismatch shaping framework is also presented. Simulation results show that the proposed technique can significantly improve DAC linearity in presence of both static mismatch and dynamic ISI errors.**

***Index Terms*—Analog-to-digital converter (ADC), device mismatch, digital-to-analog converter (DAC), dynamic element matching, dynamic error, inter-symbol interference (ISI), mismatch shaping, thermometer coding, $\Delta\Sigma$ modulator.**

## I. Introduction

MULTIBIT $\Delta\Sigma$ ADCs and DACs are more favorable than their binary counterparts for: 1) they have higher stability; 2) they allow the use of more aggressive noise transfer function, and thus, can achieve a higher SQNR; and 3) they have lower out-of-band noise, and hence, reduce jitter sensitivity and relax the linearity and slew rate requirement for the first-stage integrator (for ADC) or the reconstruction filter (for DAC). However, their drawback is that they cannot guarantee linearity in the presence of device mismatch. The mismatch errors, unshaped by the $\Delta\Sigma$ loop, can cause significant distortion and SNR loss. There are two common ways to handle the mismatch. One is to perform either analog or digital calibration [1]–[3]. The other is to use dynamic element matching (DEM). By randomly selecting the DAC elements, the DEM technique of [4] can turn distortion into white noise. The data weighted averaging (DWA) technique of [5]–[7] can achieve first-order high-pass shaping of the mismatch error by barrel shifting the selection pattern. More advanced DEM techniques have also been developed that can shape mismatch errors to higher orders [8]–[10]. The merit of DEM is that it does not need any information about device mismatch, and thus, it is generally applicable and easy to use. By contrast, any calibration technique requires highly accurate measurement of the mismatch error, which increases the design complexity. Another advantage for DEM is that it is a purely digital technique, whose cost in terms of chip area and power naturally decreases with technology scaling.

Another major source of nonlinearity in high-performance continuous-time (CT) multibit ADCs and DACs is inter-symbol-interference (ISI). ISI is a dynamic error that shows up during the transition of DAC elements. It can be caused by asymmetric on-and-off switching, clock skew, and parasitic memory effects. Note that ISI error can cause nonlinearity even in a single-bit CT $\Delta\Sigma$ ADC and DAC, which is different from mismatch induced nonlinearity that shows up only in multibit modulators. Also, unlike static mismatch whose error contribution is independent from clock frequency, the impact of ISI error increases with clock frequency. As a result, ISI error is especially problematic for high-speed CT $\Delta\Sigma$ ADCs and DACs.

A widely used analog approach to mitigate ISI error is to use the return-to-zero (RZ) pulse shape. However, this reduces the output signal amplitude assuming the same total DAC power. It also produces large discontinuities in the output waveform, which increases the requirement on filter linearity and slew rate. In addition, it is much more sensitive to clock jitter compared to a non-return-to-zero (NRZ) DAC.

It is highly desirable to develop digital DEM-like techniques to mitigate ISI error. The ideal situation is that by controlling the DAC selection pattern, we can simultaneously handle both mismatch and ISI errors. Since existing DEM techniques can randomize the DAC element selection, it might seem that they could somehow mitigate the ISI problem. Unfortunately most of the existing DEM techniques exacerbate the ISI problem. The reason is that the magnitude of the ISI error is proportional to the DAC switching rate. Most DEM techniques increase the transition activity in order to quickly scramble the DAC element selection pattern [5]–[10]. In particular, the widely used DWA technique has the highest element transition activity, as it always turns on new elements. This leads to the largest ISI error.

If we only consider the total amount of ISI error, the best element selection scheme is thermometer coding, as it has the lowest element transition rate. In addition, because its element transition is mainly caused by random quantization noise, thermometer coding also has low ISI induced distortion. Nevertheless, it cannot handle device mismatch. To solve this issue, researchers have developed modified thermometer coding schemes that make use of the intrinsic quantization

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The authors are with The Department of Electrical and Computer Engineering, University of Texas at Austin, TX 78712 USA (e-mail: arindam3110@utexas.edu; jackiechan.cl@utexas.edu; nansun@mail.utexas.edu).

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noise to randomize the element selection pattern. For example, the techniques of [11], [12] can whiten the mismatch error, and our recent work of [13] can high-pass shape the mismatch error but without any increase in the DAC element transition rate. However, the limitation of [11]–[13] is that their mismatch shaping results are not as effective as other DEM techniques due to the low element transition rate especially with a less aggressive noise transfer function (NTF).

Instead of minimizing the element transition activity, another way to reduce ISI induced distortion is to make the number of DAC element transitions to be less dependent on the signal. This important observation was first used in the modified mismatch shaping (MMS) technique [14] to keep a relatively constant total number of up $(0 \rightarrow 1)$ and down $(1 \rightarrow 0)$ transitions of all DAC elements during every clock cycle. This turns a large portion of the ISI error into an offset. Despite its clear advancement from prior works, the MMS technique has its own limitations. Its ISI error model assumes that both up and down transitions produce the same ISI error, which is rarely true in reality [15]. In addition, although it is mentioned in [14] that the ISI error can be shaped, no details have been given on how it can be realized.

The recent development of ISI shaping technique [15] represents a major step forward. It [15] developed a general ISI model and proved that the ISI induced nonlinearity can be associated with only one type of transition (e.g., the up transition). Thus, by regulating the up transition rate via a feedback loop, it not only ensures that the long-term average of the up transition rate is constant, but also high-pass shapes the ISI error. Later, building upon [15], a recent work further reduces the in-band ISI error by monitoring both up and down transitions [16]. Although the existing ISI shaping techniques [15], [16] greatly improve the linearity and SNR, they suffer from one limitation: when the signal amplitude is large, they still produce large distortions due to ISI errors. The reason is that the ISI shaping loop is coupled with the mismatch shaping loop. As a result, although the average up transition rate is constant, the instantaneous number of up transitions is still signal dependent, which causes large distortions when the coupling is tight at large signal amplitudes.

This paper proposes a novel DEM algorithm that can address both the static mismatch error and the dynamic ISI error for an NRZ DAC. Compared to [14]–[16], the key advantage of the proposed technique is that it guarantees no ISI-induced distortion even at large signal amplitudes. This is achieved by decoupling mismatch shaping and ISI shaping at every clock period. It builds upon the technique of [14] but significantly extends it in the following ways:

1) It brings in the general ISI error model of [15] and proves that having a constant number of total transitions is equivalent to linearizing the up transition sequence and the ISI error;
2) It allows the instantaneous number of transitions, $K[n]$, to vary among three adjacent integers, $L-1$, $L$, and $L+1$, and guarantees that $K[n]$ and signal $d[n]$ are completely uncorrelated;
3) It uses a $\Delta\Sigma$ loop to generate $K[n]$, and thus, can shape $K[n]$ to the first-order and also higher orders.

The proposed technique monitors only the total number of transitions $K[n]$, which is different from [15] that monitors the transition of each individual DAC element. The benefit is reduced hardware complexity, but the limitation is that it can only shape $K[n]$ but not the individual DAC element transition sequence. Nevertheless, this limitation is mild. The reason is that the proposed technique can shape the majority common-mode part of the ISI errors from all DAC elements. Although it cannot shape the mismatches among ISI errors from different DAC elements, it can whiten their spectra. As a result, it still ensures no distortion and can significantly reduce in-band ISI errors, even in the presence of ISI mismatches. In addition, the mismatches among ISI errors can be kept small in practice [14], [15].

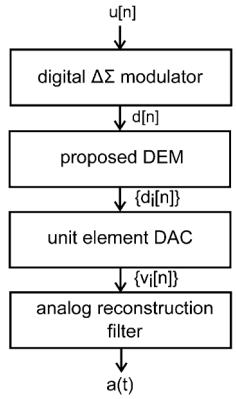


Fig. 1. Architecture of a $\Delta\Sigma$ DAC with the proposed DEM scheme.

The proposed technique can be implemented using the vector-quantizer (VQ) based mismatch shaping architecture [8]. Since it requires two vector quantizers, its hardware cost is expected to be twice that of a standard VQ based DEM scheme. Nevertheless, because it is purely digital, the increased hardware cost can be compensated by going to an advanced technology node. If hardware complexity reduction is necessary when the number of elements is large, this paper also presents a way to minimize the number of digital gates by adopting a tree-structured topology similar to the mismatch shaping architecture of [9]. The proposed technique is validated through behavioral level simulations in Matlab. The simulation results show that the proposed technique can increase SFDR by more than 40 dB compared to the ISI shaping technique of [15].

The paper is organized as follows. Section II reviews the mismatch and ISI error model. Section III presents the proposed DEM technique. Section IV extends the proposed technique to higher-order mismatch and ISI shaping. Section V shows the simulation results. Finally, Section VI draws the conclusion.

## II. Mismatch and ISI Error Model

The architecture of a $\Delta\Sigma$ DAC with the proposed DEM technique is shown in Fig. 1. Let us use $d_i[n]$ to represent the single-bit digital input for the $i$-th unit element DAC in a multibit DAC. We can derive a discrete-time representation of the unit element DAC output $v_i[n]$ in the presence of mismatch and ISI errors.

$$v_i[n] = (1+\Delta_i)d_i[n] + \mathrm{ISI}_i[n] \tag{1}$$

where $\Delta_i$ is the static mismatch and $\mathrm{ISI}_i[n]$ represents the dynamic ISI error during the transition from $d_i[n-1]$ to $d_i[n]$. As analyzed in [15], $\mathrm{ISI}_i[n]$ can be modeled as

$$\mathrm{ISI}_i[n] = \alpha_i + \beta_i d_i[n] + \gamma_i d_i[n-1] + \epsilon_i \Gamma_i[n] \tag{2}$$

where $\alpha_i$, $\beta_i$, $\gamma_i$, and $\epsilon_i$ are normalized ISI error coefficients in percentage. They are independent from $d[n]$ and are fixed for a given DAC element. Their values increase as the clock frequency increases, because the time duration of each DAC symbol decreases while the absolute amount of ISI error remains unchanged. $\Gamma_i[n]$ is the up transition sequence, given by $\Gamma_i[n] = (1 - d_i[n-1])d_i[n]$. The first three terms of (2) are linear with $d_i[n]$, while the last term produces nonlinearity. Plugging (2) into (1), we have:

$$v_i[n] = d_i[n] + \alpha_i + (\Delta_i + \beta_i)d_i[n] + \gamma_i d_i[n-1] + \epsilon_i \Gamma_i[n] \quad (3)$$

Assuming the law of superposition holds when combining outputs from all unit element DACs, we derive the overall DAC output $v[n]$ as

$$\begin{aligned} v[n] &= \sum_{i=1}^{M} v_i[n] \\ &= d[n] + \sum_{i=1}^{M} \alpha_i + \sum_{i=1}^{M} (\Delta_i + \beta_i) d_i[n] \\ &\quad + \sum_{i=1}^{M} \gamma_i d_i[n-1] + \sum_{i=1}^{M} \epsilon_i \Gamma_i[n] \end{aligned} \quad (4)$$

where $M$ is the total number of unit DAC elements and $d[n]$ is the multi-bit quantizer output. (4) shows that the mismatch and ISI errors are intertwined. In order for $v[n]$ to be clean, we must guarantee that there is no distortion in any $d_i[n]$ or $\Gamma_i[n]$, because $\epsilon_i$, $\alpha_i$, $\beta_i$, and $\Delta_i$ are all unknown random variables. Conventional DEM techniques can shape $d_i[n]$ by scrambling the element selection, but cannot handle $\Gamma_i[n]$ [15]. As mentioned earlier, most of the DEM techniques actually increase the element transition activity, leading to larger ISI induced distortion. To improve linearity, we can minimize the element transition rate as in [11]–[13], or keep a relatively constant number of transitions as in [14]–[16]. We can rewrite the last term of (4) as:

$$\begin{aligned} \sum_{i=1}^{M} \epsilon_i \Gamma_i[n] &= \sum_{i=1}^{M} \epsilon(1 + \epsilon_{ri}) \Gamma_i[n] \\ &= \epsilon \left( \sum_{i=1}^{M} \Gamma_i[n] + \sum_{i=1}^{M} \epsilon_{ri} \Gamma_i[n] \right) \\ &= \epsilon \left( \Gamma[n] + \sum_{i=1}^{M} \epsilon_{ri} \Gamma_i[n] \right) \approx \epsilon \Gamma[n] \end{aligned} \quad (5)$$

where $\epsilon_{ri}$ represents the relative mismatch in $\epsilon_i$ among different unit DAC elements and $\Gamma[n] \equiv \sum_{i=1}^{M} \Gamma_i[n]$. In deriving (5), we have assumed a reasonable matching among ISI error coefficients $\{\epsilon_i\}$, so that $\epsilon_{ri} \ll 1$. (5) shows that if we can make sure that the total number of up transition, $\Gamma[n]$, is a linear function of $d[n]$, we can remove ISI induced distortion. Furthermore, if we can make $\Gamma[n]$ to have a high-pass spectrum, we can also shape the ISI error. These are the goals of this work. Note that even if the ISI errors have significant mismatches and $\epsilon_i$ is not much smaller than 1, the proposed algorithm still does not produce ISI induced distortion, as it randomizes $\{\Gamma_i[n]\}$ and whitens its spectrum. More details will be presented later.

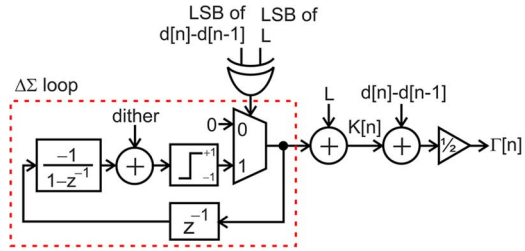


Fig. 2. Circuit block diagram that generates first-order high-pass shaped $K[n]$ and $\Gamma[n]$.

## III. Proposed DEM Technique With Signal Independent Transition Rate

### A. Proposed DEM Technique

Let us use $K[n]$ to denote the total number of up and down transitions. Because the total number of up transitions minus the total number of down transitions is equal to $(d[n] - d[n-1])$, we can derive that:

$$\Gamma[n] = \frac{K[n] + d[n] - d[n-1]}{2} \quad (6)$$

Thus, if we design $K[n]$ to be uncorrelated with $d[n]$ and have a high-pass spectrum, we ensure no ISI induced distortion and can shape the ISI error. Note that $K[n]$ cannot be a constant, because $(K[n] + d[n] - d[n-1])$ must be even, which means $K[n]$ and $d[n]$ cannot be completely independent. However, we can define $K[n]$ in such a way that it is uncorrelated with $d[n]$. The method is as follows. Let us assume that we want the long term average of $K[n]$ to be $L$, which is a constant integer. If $(L + d[n] - d[n-1])$ is even, we choose $K[n] = L$. If it is odd, we randomly choose $K[n]$ to be either $L-1$ or $L+1$. As a result, the average of $K[n]$ remains to be $L$, and $K[n]$ is uncorrelated with $d[n]$ due to random selection. This method can only whiten the spectrum of $K[n]$. To high-pass shape it, we can use a $\Delta\Sigma$ modulator to make the selection of $L-1$ or $L+1$. Fig. 2 shows the hardware implementation for such a scheme. An XOR gate examines the parity of $(L + d[n] - d[n-1])$. If it is even, the first-order $\Delta\Sigma$ modulator produces 0, leading to $K[n] = L$. If it is odd, the output of the modulator is either $+1$ or $-1$ depending on the integrator output, which results in $K[n] = L \pm 1$. A small and efficient dither is added to remove spurs [17]. This way, we guarantee that $K[n]$ is first-order high-pass shaped.

As shown in Fig. 2, once $K[n]$ is generated, we obtain $\Gamma[n]$ from (6) and use it to decide the element selection in the following manner: at every clock cycle,

1) We turn on $\Gamma[n]$ unselected elements that have been least frequently used.
2) We keep on $(d[n] - \Gamma[n])$ selected elements that have been least frequently used.

There are requirements on $d[n]$ and $\Gamma[n]$ in order for this algorithm to work. First, $(d[n-1] + \Gamma[n]) \leq M$. If this inequality is violated, step 1) of the algorithm is unrealizable, as the total number of unselected elements is smaller than $\Gamma[n]$. By plugging in (6), this inequality is essentially

$$K[n] \leq (2M - d[n] - d[n-1]) \quad (7)$$

The second requirement is $0 \leq (d[n] - \Gamma[n]) \leq d[n-1]$. If violated, step 2) of the algorithm is invalid because there is

insufficient number of elements to keep on. Again plugging in (6), we have

$$(d[n]-d[n-1]) \le K[n] \le (d[n]+d[n-1]) \qquad (8)$$

These requirements impose constraints on $K[n]$ and the range of $d[n]$. The lower limit for $K[n]$ is $(d[n]-d[n-1])$. In a low-pass $\Delta\Sigma$ modulator with high OSR, the range of $(d[n]-d[n-1])$ is typically set not by the signal but by the noise transfer function (NTF). Thus, this limit essentially states that $K[n]$ or $L$ must be equal or greater than the maximum NTF gain. For example, if $\max\{|NTF(\omega)|\}=2$, we have $L \ge 2$. Note that for a $\Delta\Sigma$ modulator with low OSR, the maximum value of $(d[n]-d[n-1])$ may be larger than $\max\{|NTF(\omega)|$. In such a case, $L$ needs to be set even larger. Similarly, we can derive the constraints on the range of $d[n]$ from $K[n] \le (d[n]+d[n-1])$ and $K[n] \le (2M-d[n]-d[n-1])$. They are equivalent to $K[n] \le (d[n]+d[n-1]) \le (2M-K[n])$. Thus, the maximum range for $d[n]$ is smaller than $[0, M]$. For example, if $M=32$ and $L=2$, we have $1 \le d[n] \le 31$. This constraint is mild as it is only about 1 dB loss in the signal swing. However, if $\max\{|NTF|\}$ is large and $M$ is small, the constraint will become tighter. Hence, the proposed technique is most suitable for $\Delta\Sigma$ modulators with a large $M$ and a small $\max\{|NTF(\omega)|\}$. In case $d[n]$ goes beyond the aforementioned range, we can stop controlling the number of transitions and go back to the conventional DEM scheme. This way, we can still support a full signal range, but just lose the ISI shaping capability when $d[n]$ is close to full scale. Note that such constraint on $d[n]$ also exists for other ISI shaping techniques (e.g., [15], [16]). More discussions on the trade-offs between input signal swing, $M$, and $\max\{|NTF(\omega)|\}$ are presented in the Appendix.

As mentioned earlier, the proposed algorithm always turns on or keeps on those DAC elements that are least frequently used. This is necessary to achieve mismatch shaping. It ensures the long-term usage frequencies for all DAC elements are equal, and thus, every $\{d_i[n]\}$ is high-pass shaped, leading to small in-band mismatch error. To implement it in hardware, we need to keep track of the number of usages for every unit element DAC, which can be realized using an integrator $1/(1-z^{-1})$.

Fig. 3 shows one hardware implementation of the proposed DEM technique. It is based on the vector-quantizer (VQ) framework [8]. The key modification is the insertion of two direct feedback paths. Similar to [13], by choosing a large enough gain $G$, we can ensure that $V_{q1}$ always gives a higher priority to elements that are not previously selected and $V_{q2}$ always gives a higher priority to elements that are previously selected. Finally, an array of OR gates combines the selected elements and yield $\{d_i[n]\}$. This way, it ensures that the total number of up transitions is equal to $\Gamma[n]$ and the total number of selected elements is equal to $d[n]$.

For efficient hardware implementation, the two summers adding and subtracting $G \cdot d_i[n-1]$ from the $V_{q1}$ path and $V_{q2}$ path respectively can be removed and replaced by an indicator bit which acts as the sign bit for the inputs to $V_{q1}$ and $V_{q2}$. For the elements of $d_i[n]$ that have been selected in the previous cycle, the indicator bit will be set to "1" for the corresponding inputs to $V_{q2}$ and the indicator bit will be set to "0" for the remaining inputs to $V_{q2}$. The indicator bits for the inputs to $V_{q1}$ are complements of the indicator bits for the inputs to $V_{q2}$. This ensures that correct priorities are given in both $V_{q1}$ and $V_{q2}$.

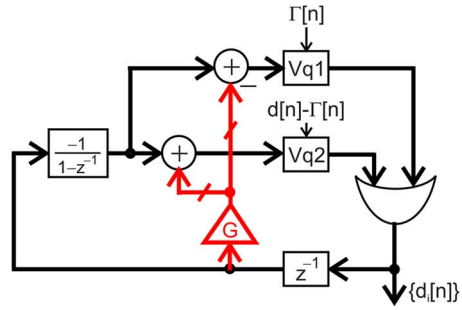


Fig. 3. Implementation of the proposed DEM technique.

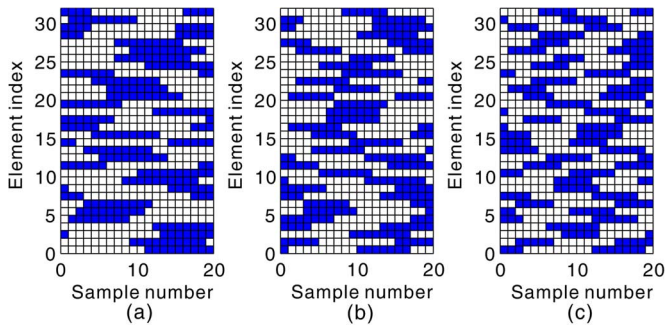


Fig. 4. Element selection pattern for the proposed technique for (a) $L=3$; (b) $L=4$; (c) $L=5$.

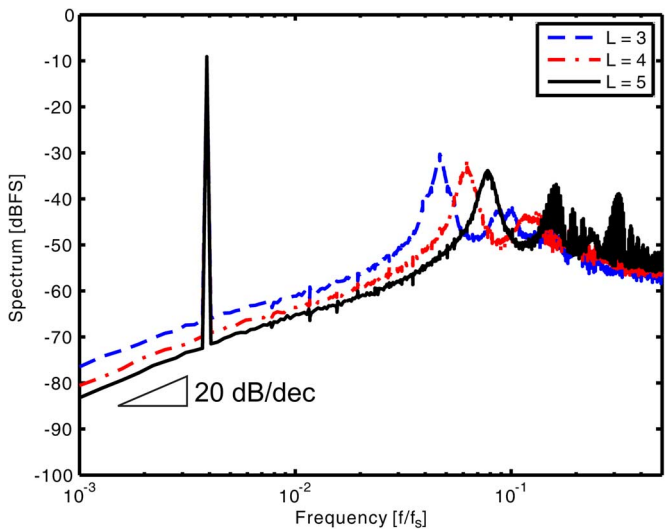


Fig. 5. Spectra of $d_i[n]$ for different $L$ values.

The proposed algorithm is implemented in Matlab. Fig. 4 shows the simulated selection pattern for $M=32$ and $L=3$, 4 and 5. The solid blue box indicates that its corresponding unit element DAC is selected. The $\Delta\Sigma$ modulator is a fifth order modulator with maximum NTF gain of 2. The input is a sine wave with amplitude of $-3$ dBFS and frequency of $f_s/257$. Fig. 5 shows the spectra of $d_i[n]$. As expected, it is first order shaped. With increase in $L$, the noise floor goes down. The reason is that as the number of transitions increases, the element selection can be scrambled more quickly. However, enlarging $L$ does impose more constraints on the maximum allowed signal swing as explained earlier. Thus, in real application, we need to balance this trade-off.

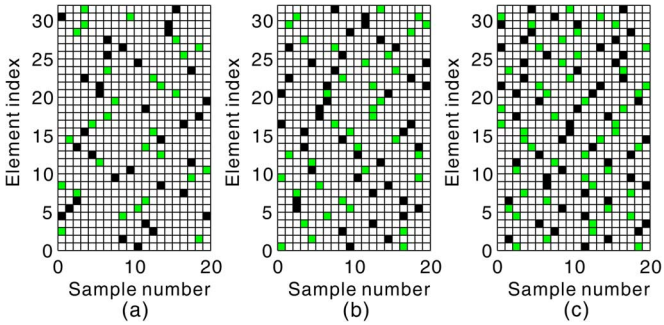


Fig. 6. Element transition pattern for (a) $L = 3$; (b) $L = 4$; (c) $L = 5$.

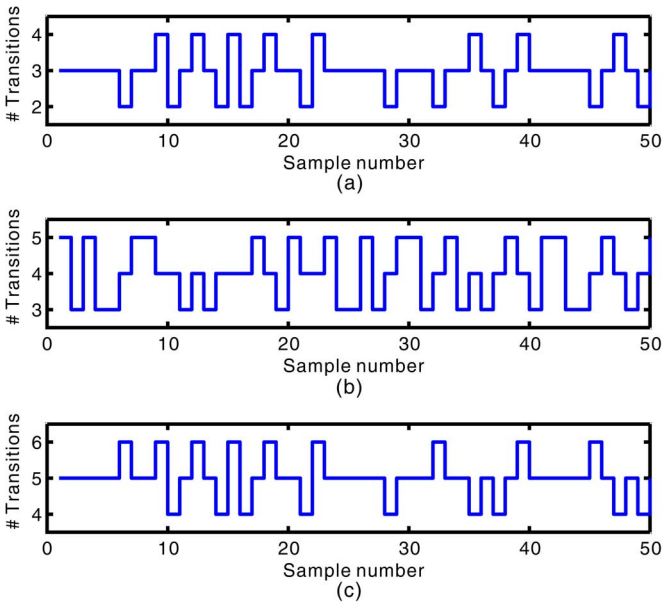


Fig. 7. $K[n]$ as a function of time for (a) $L = 3$; (b) $L = 4$; (c) $L = 5$.

Note that the spectra of $d_i[n]$ show peaks at frequencies of $k \cdot f_s \cdot L/(2M)$, where $k$ is an integer. The reason is that on an average $L/2$ new DAC elements are turned on every clock cycle. Since there are in total $M$ elements, each $d_i[n]$ takes on average $2M/L$ clock cycles to repeat its pattern, leading to spectra peaks at $k \cdot f_s \cdot L/(2M)$. The presence of noise peaks in the spectra of $d_i[n]$ requires a reasonably high OSR to maintain a good static mismatch shaping performance. Thus there is trade-off with respect to choice of $L$. A larger value of $L$ will push the noise peaks away from in-band at the cost of reducing the redundancy available for ISI shaping and lowering the signal swing. This is similar to the trade-off in DWA which has the highest element switching rate and thus the best first-order static mismatch shaping, but also the worst ISI error.

Fig. 6 plots the corresponding element transition pattern. The dark black box indicates an up $(0 \rightarrow 1)$ transition, and the light green box indicates a down $(1 \rightarrow 0)$ transition. It is clear that with increase in $L$ there are more transitions. The total number of transitions $K[n]$ as a function of time is plotted in Fig. 7. As discussed before, for each $L$, $K[n]$ varies among $L-1$, $L$, and $L+1$. It always has the same parity as $(d[n] - d[n-1])$. The spectra of $K[n]$ are shown in Fig. 8, which demonstrates clear first-order shaping. Note that there are no spurious tones because $K[n]$ and $d[n]$ are made uncorrelated.

Fig. 9 plots the spectra of $\Gamma[n]$. The spectrum of $\Gamma[n]$ is very similar to Fig. 8 except that there is a large fundamental tone

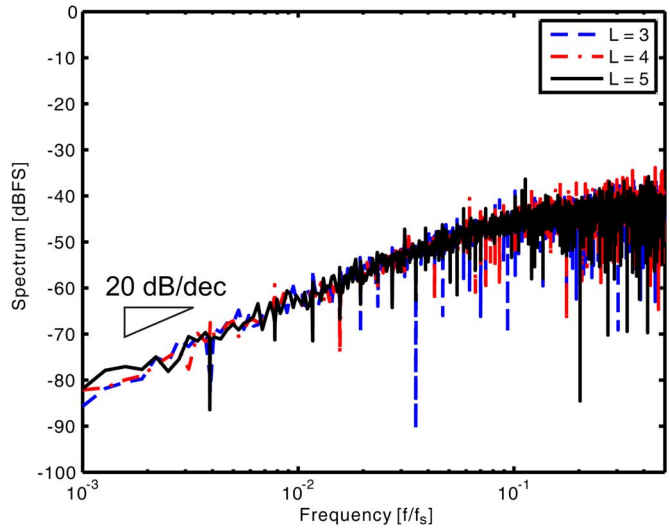


Fig. 8. Spectra of $K[n]$ for different $L$ values.

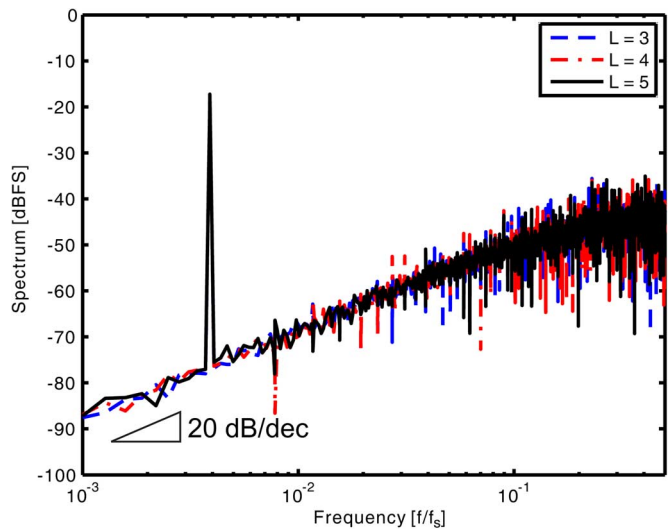


Fig. 9. Spectra of $\Gamma[n]$ for different $L$ values.

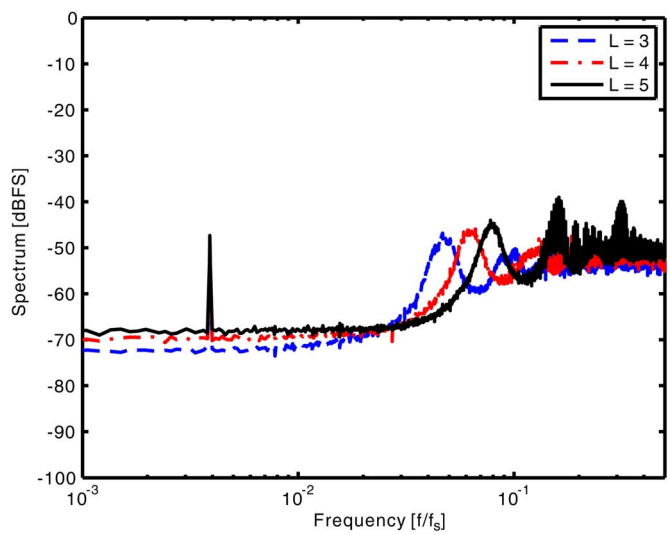


Fig. 10. Spectra of $\Gamma_i[n]$ for different $L$ values.

because $\Gamma[n]$ is proportional to $(d[n]-d[n-1])$, as shown in (6). These simulation results solidly prove that the proposed DEM technique can shape both mismatch and ISI errors.

Fig. 10 plots the spectra of $\Gamma_i[n]$. Note that the spectrum of each individual $\Gamma_i[n]$ is whitened but not high-pass shaped. The

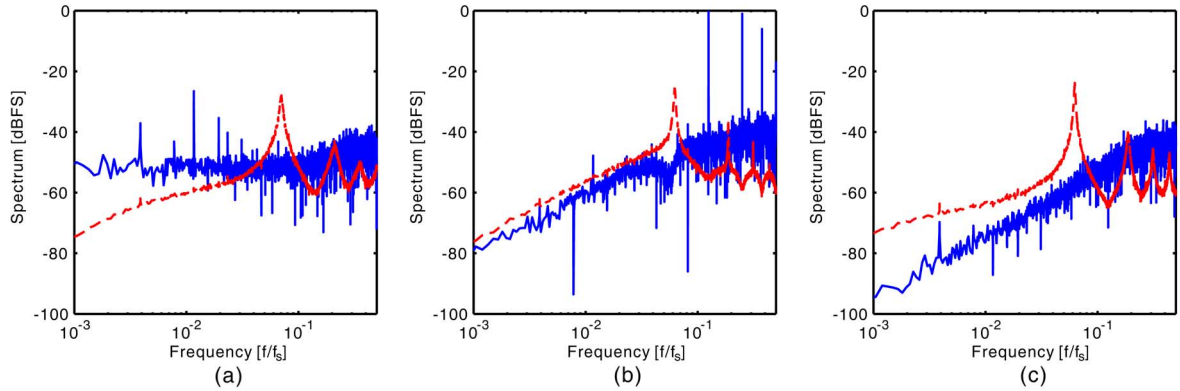


Fig. 11. Spectra of $\Gamma[n]$ (in solid line) and $d_i[n]$ (in dashed line) for (a) MMS technique; (b) ISI shaping technique of [15]; and (c) proposed technique for $-60$ dBFS input.

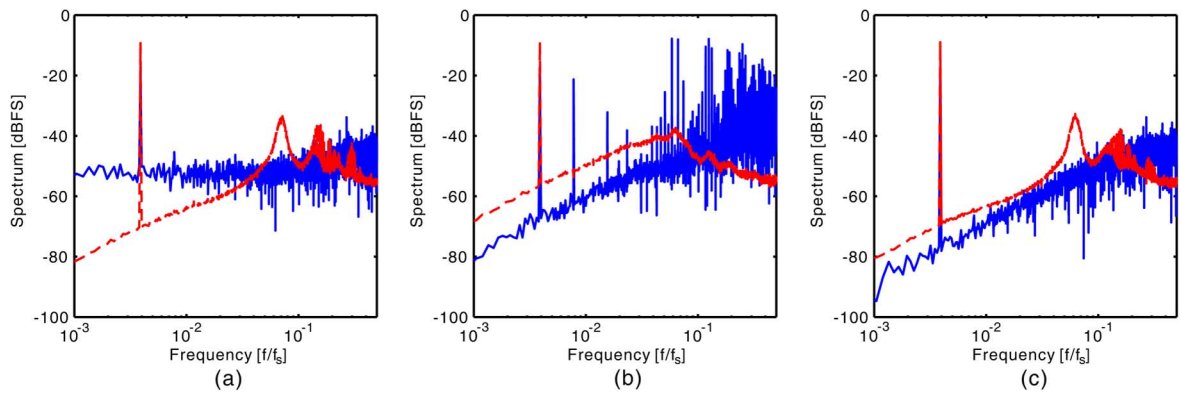


Fig. 12. Spectra of $\Gamma[n]$ (in solid line) and $d_i[n]$ (in dashed lined) for (a) MMS technique; (b) ISI shaping technique of [15]; and (c) proposed technique for $-3$ dBFS input.

reason is that the proposed technique monitors only the total number of transitions $K[n]$, but not the transition of each individual DAC element. The merit is reduced hardware cost, but it loses the ability to shape $\Gamma_i[n]$. Nevertheless, because it can high-pass shape $\Gamma[n]$, the majority common-mode part of the ISI errors is removed from in-band. Also, as it whitens the spectra of $\Gamma_i[n]$, the in-band contribution of the ISI mismatches $(\epsilon_{ri})$ is greatly reduced too.

### B. Comparison to MMS and ISI Shaping Techniques

Since the proposed technique is closely related to the MMS technique [14] and ISI shaping technique [15], it is meaningful to compare against their performance. For the original MMS technique, $K[n]$ is allowed to vary between two adjacent integers, $L$ and $L+1$. Because the value of $K[n]$ is directly set by the parity of $(d[n]-d[n-1])$, $K[n]$ and $d[n]$ are correlated. Consequently, there are still spurious tones in $\Gamma[n]$ and the spectrum of $K[n]$ is not shaped. Both the ISI shaping technique and the proposed technique achieve high-pass shaping of $\Gamma[n]$ by controlling $\Gamma[n]$ via a feedback loop. The difference is that the technique of [15] can only ensure the long-term average number of transitions to be a constant. However, its instantaneous number of transitions still depends on $d[n]$ due to the coupling between the ISI and mismatch shaping loops. As a result, it produces large distortions when the coupling is strong at large input amplitude. By contrast, the proposed technique makes sure that the number of transitions is uncorrelated with $d[n]$ at any clock cycle. Consequently, no ISI induced distortion is produced.

The above analyses are confirmed by simulation results. Fig. 11 shows the spectra of $d_i[n]$ and $\Gamma[n]$ for a small $-60$ dBFS input for MMS [14], ISI shaping [15], and the proposed technique. For a fair comparison, the average numbers of element transitions are chosen to be close for all three techniques. As a result, their first-order mismatch shaping results are similar (see dashed curves in Fig. 11). As expected, the spectrum of $\Gamma[n]$ for the MMS technique is unshaped. It also has spurious tones due to the correlation between $K[n]$ and $d[n]$. Both the ISI shaping technique and the proposed technique achieve first-order high-pass shaping of $\Gamma[n]$. Since the proposed technique has tighter control over $\Gamma[n]$, its noise floor is lower than that of ISI shaping technique by 10 dB.

Compared to the ISI shaping technique of [15], the advantage of the proposed technique is more pronounced at large inputs. Fig. 12 shows the simulation results for a large $-3$ dBFS input. The spectrum of $\Gamma[n]$ for the technique of [15] shows large second-order and third-order distortions. By contrast, the proposed technique produces a distortion-free $\Gamma[n]$. Note that the mismatch shaping performance for the ISI shaping technique of [15] is also worsened by 10 dB when the input is large, which is also due to the interference between its coupled mismatch and ISI shaping loops.

### C. Hardware Complexity Reduction

As shown in Fig. 3, the proposed technique uses two vector quantizers (VQs). Each VQ performs a hardware sorting of $M$ digital inputs, which can be hardware intensive when $M$ is large. If we directly implement a VQ, the total number of digital gates

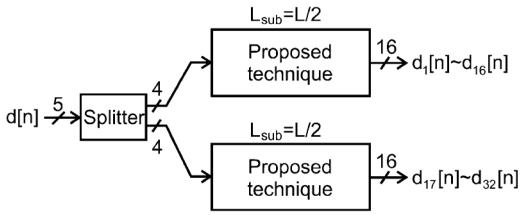


Fig. 13. Implementation of the proposed technique with reduced hardware complexity.

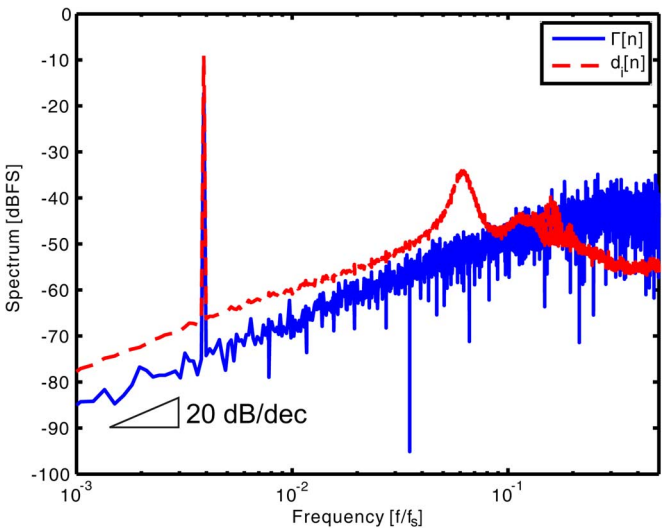


Fig. 14. Spectra of $\Gamma[n]$ (in solid line) and $d_i[n]$ (in dashed line) with reduced hardware complexity.

increases with $M$ in a super-linear fashion. To reduce the digital complexity, we can adopt the tree-structure of [9]. Fig. 13 shows an example for $M = 32$. We first use a splitter to separate the 5-bit $d[n]$ into two 4-bit integers. This way, we only need to implement two 4-bit version of the proposed technique, leading to reduced hardware complexity. To maintain the same total number of transitions, we also split $L$ and ensure that the average transition number is $L/2$ for each path.

Fig. 14 shows the simulation results using this hardware complexity reduction method with $L = 4$. It achieves first-order shaping of both $\Gamma[n]$ and $d_i[n]$. Compared to the results shown in Fig. 5 and Fig. 9 under the same condition but using 5-bit VQs, the noise floor of Fig. 14 is about 3 dB higher. This represents the trade-off for using a splitter and 4-bit VQs.

## IV. High-Order Mismatch and ISI Shaping

The proposed technique can be extended to achieve high-order mismatch and ISI error shaping. Fig. 15 shows the circuit block diagram that produces a second-order high-pass shaped $K[n]$. The modification is the addition of one more integrator and a feed-forward path to stabilize the modulator. Similarly, to achieve second-order mismatch shaping, the overall architecture can be implemented as shown in Fig. 16.

Fig. 17 shows the Matlab simulation results. The clear 40-dB/decade slope shows that both $\Gamma[n]$ and $d_i[n]$ are second-order high-pass shaped. For even higher order shaping, we can adopt the technique of [10] to achieve up to fourth-order shaping.

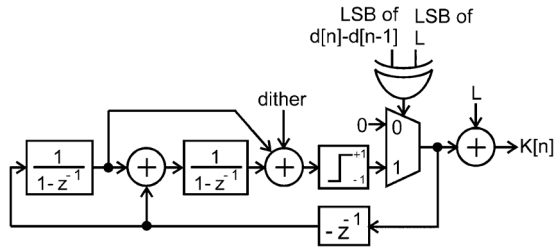


Fig. 15. Second-order shaped $K[n]$ generation technique.

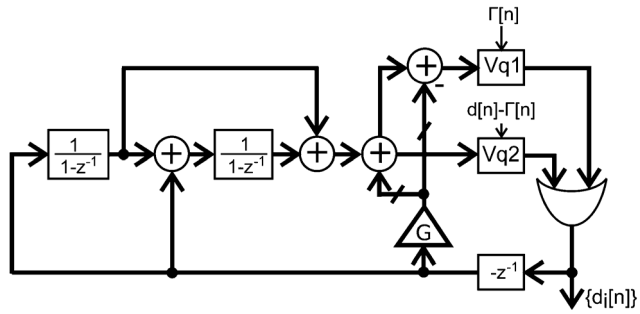


Fig. 16. Implementation of the proposed technique for second-order mismatch and ISI shaping.

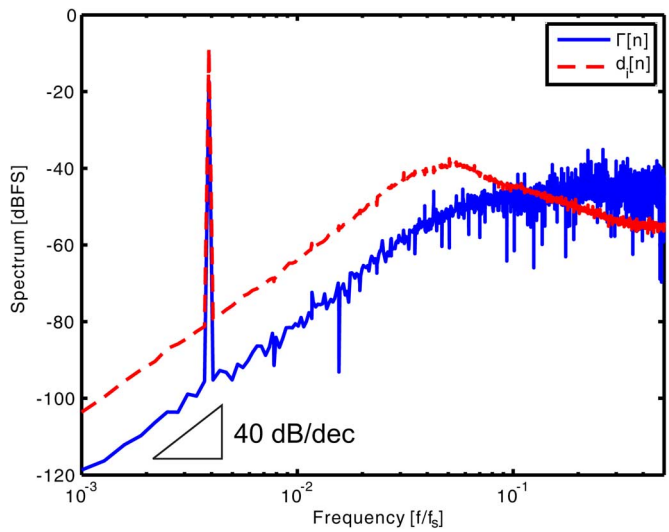


Fig. 17. Spectra of $\Gamma[n]$ and $d_i[n]$ for second-order mismatch and ISI shaping.

## V. Simulation Results for a Multibit $\Delta\Sigma$ DAC

To further study the performance of the proposed technique, we have applied it to a 32-element $\Delta\Sigma$ DAC and performed a discrete time simulation with $2^{16}$ points. The $\Delta\Sigma$ modulator is fifth order and its NTF has a maximum out-of-band gain of 2. It is designed and optimized by using the Matlab $\Delta\Sigma$ modulator toolbox [8]. The oversampling ratio (OSR) is 64. The input signal frequency is set to be $f_s/1332$, so that distortion terms up to tenth order are in-band. The input amplitude is $-1.5$ dBFS. The static mismatch between unit DAC elements is assumed to have a zero mean but a standard deviation of 1%. The ISI error ($\epsilon$) is assumed to be 2%, while the relative mismatch between ISI errors of different elements ($\epsilon_{ri}$) is assumed to be 1%. Thermal noise is also added so that the thermal noise limited SNR at OSR of 64 is 103.7 dB.

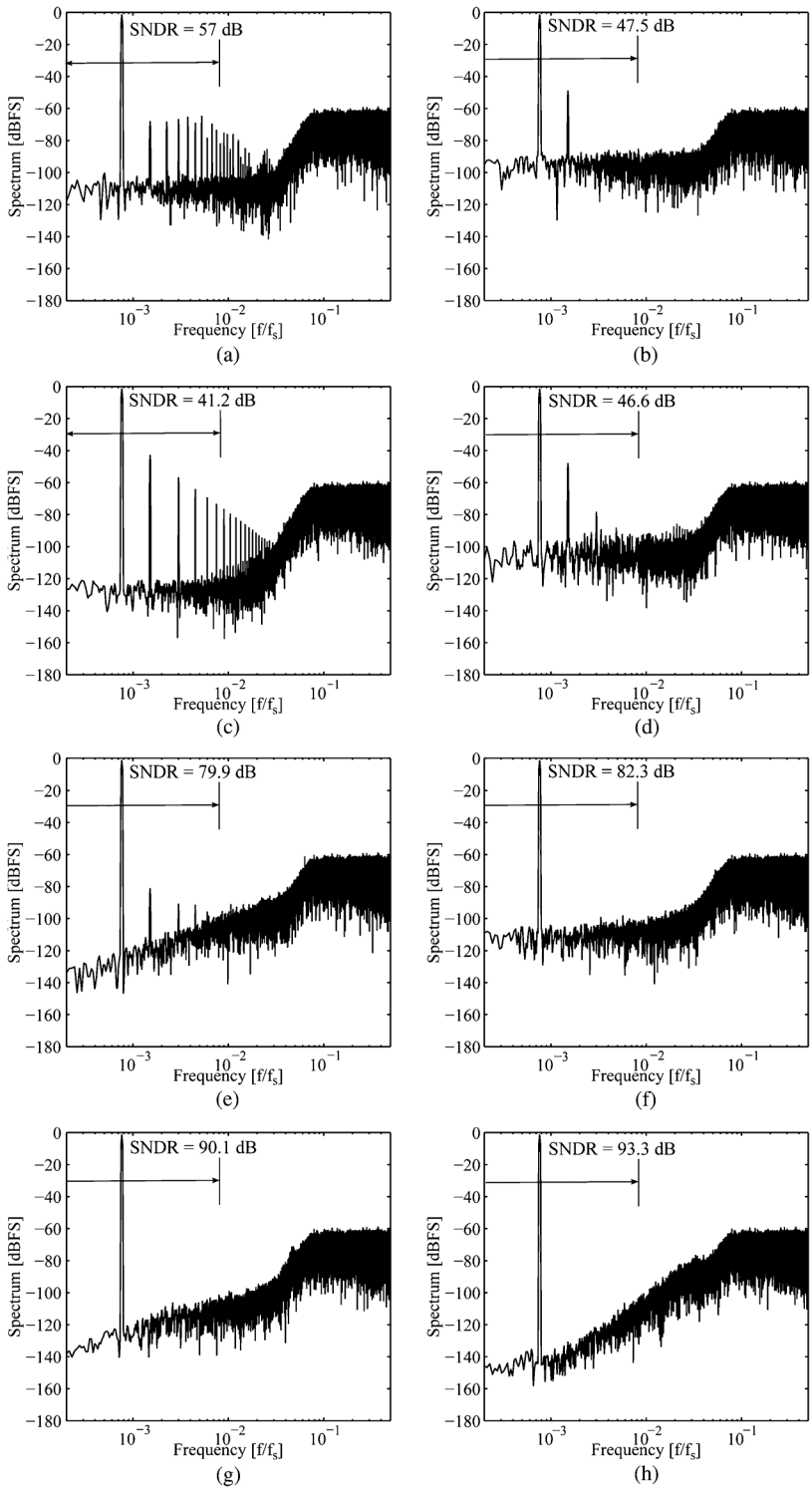


Fig. 18. DAC output spectrum for (a) thermometer coding; (b) random selection; (c) DWA; (d) 2nd-order DEM; (e) ISI shaping [15]; (f) MMS [14]; (g) proposed technique with first-order shaping; (h) proposed technique with second-order shaping.

Fig. 18 shows the simulation results for various types of DEM techniques. The basic thermometer coding is prone to device mismatches, and thus, produces many harmonics and a high noise floor, leading to an SFDR of 58.9 dB and an SNDR of 57 dB [see Fig. 18(a)]. Random selection of DAC elements whitens the mismatch errors; however, it cannot handle ISI errors, and because of its increased element transition rates, the overall SFDR is reduced to 47.7 dB [see Fig. 18(b)]. DWA can shape the mismatch error and lower the noise floor, but it produces the largest ISI induced distortions and its SFDR is worsened to 41.5 dB [see Fig. 18(c)]. A second-order DEM has lower distortion than DWA but the SFDR is still limited to 46.8 dB [see Fig. 18(d)]. The ISI shaping technique of [15] can shape both mismatch and ISI errors, leading to a higher SNDR of 78 dB, but it produces a large second-order distortion, resulting in a SFDR of 79.9 dB [see Fig. 18(e)]. The MMS technique significantly re-

TABLE I
COMPARISON OF DIFFERENT DEM TECHNIQUES FOR MULTIBIT $\Delta\Sigma$ DAC

| | OSR=64 | | OSR=16 | |
|---|---|---|---|---|
| | SNDR(dB) | SFDR(dB) | SNDR(dB) | SFDR(dB) |
| Ideal | 103.7 | $> 130$ | 81.7 | $> 130$ |
| Thermometer | 57 | 58.9 | 57 | 58.9 |
| Random selection | 47.5 | 47.7 | 47.5 | 47.7 |
| DWA | 41.2 | 41.5 | 41.2 | 41.4 |
| 2nd-order DEM | 46.6 | 46.8 | 46.6 | 46.8 |
| MMS [14] | 82.3 | 102.8 | 73.6 | 104.5 |
| ISI shaping [15] | 78 | 79.9 | 64.1 | 79.9 |
| This work | 90.1 | $> 110$ | 75.5 | $> 110$ |

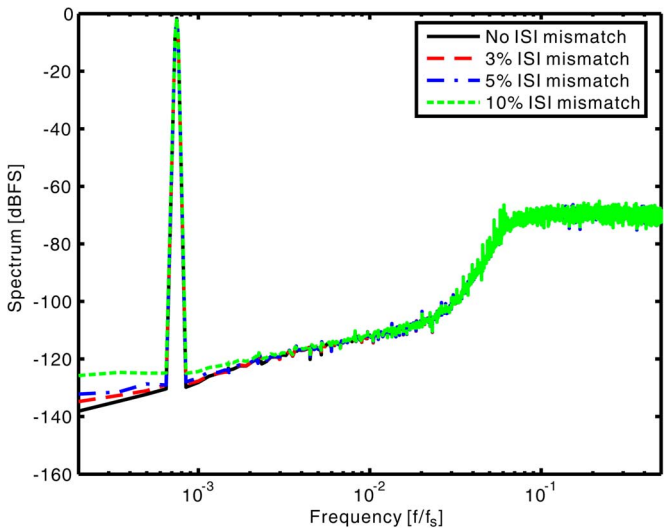


Fig. 19. Output spectrum for varying mismatch between ISI errors of the DAC elements.

duces ISI induced distortions and improves the SFDR to 102.8 dB. However, because it cannot shape the ISI error, the in-band noise floor is flat, leading to a limited SNDR of 82.3 dB [see Fig. 18(f)]. The proposed technique achieves mismatch and ISI error shaping but without any linearity degradation. As shown in Fig. 18(g), for first-order shaping, the SFDR is above 110 dB, and the SNDR is also improved to 90.1 dB for its better ISI shaping result. If second-order shaping is used [see Fig. 18(h)], SNDR can further increase to 93.3 dB. The simulation results are summarized in Table I. They clearly demonstrate the effectiveness of the proposed technique.

As discussed earlier, the proposed technique can achieve good performance in the presence of ISI mismatches. To prove it, simulations with different ISI mismatch values ($\epsilon_r$) have been performed, while other parameters are kept the same as before. Fig. 19 shows DAC output spectra. As can be seen, the proposed technique always guarantees no ISI induced distortion. The effect of ISI mismatch is only a slightly increased noise floor. The SNDR at OSR of 64 are 90.1 dB, 90 dB, 89.9 dB, and 89.5 dB for 0%, 3%, 5%, and 10% ISI mismatches, respectively. The performance degradation is within 1 dB even for a relatively large ISI mismatch of 10%.

## VI. CONCLUSION

This paper has presented a novel mismatch and ISI shaping technique for continuous-time low-pass $\Delta\Sigma$ DACs. Compared to existing mismatch shaping and ISI shaping techniques, it can significantly reduce the distortions due to both static mismatches and dynamic ISI errors. It is especially useful for applications that demand high linearity, such as high-quality audio applications. As a purely digital technique, it is scaling friendly and is expected to consume negligible area and power in deep-submicrometer CMOS processes.

## APPENDIX

The proposed technique imposes a constraint on the maximum input swing as has been discussed in Section III. This is a fundamental trade-off in that redundancies are required to achieve de-correlation of the number of transitions from the signal $d[n]$. MMS algorithm [14] also has a similar restriction on the input swing. The technique of [15] allows for a larger signal swing but at the expense of significantly increased ISI induced tones in the spectrum.

Table II shows a comparison of the different ISI error reduction techniques for $M = 16$ and different $\max\{NTF(\omega)\}$. Table III shows the same comparison for $M = 32$. The simulation conditions are the same as those used to obtain Fig. 18. An OSR of 64 is used for all SNDR calculations.

It can be seen from Table II, III that the proposed technique maintains higher SNDR than the other techniques over different $\max\{NTF(\omega)\}$. It can also be seen from Table II that the proposed technique does not suffer seriously from input swing reduction for $M$ as small as 16 and $\max\{NTF(\omega)\}$ as high as 4. Even for a high-speed CT $\Delta\Sigma$ modulator with a small $M$, the proposed technique still outperforms a single-bit modulator with NRZ DAC as the proposed DEM can support a higher out-of-band NTF gain.

It should be noted here that signal swing reduction with the proposed technique is a constraint only when both $M$ is small and $\max\{NTF(\omega)\}$ is large simultaneously. For multi-bit CT $\Delta\Sigma$ modulators, a moderate value of $\max\{NTF(\omega)\}$ (e.g., 2 or 3) is sometimes preferred over a large $\max\{NTF(\omega)\}$. For a $\Delta\Sigma$ ADC, a moderate out-of-band NTF gain results in smaller input swing for the first-stage integrator, thereby improving its linearity and relaxing the slew rate requirement. For a $\Delta\Sigma$ DAC, it relaxes the performance requirement of the analog reconstruction filter. Moreover, a moderate out-of-band gain together with a large $M$ can reduce the amount of out-of-band noise, and thus, reduce the clock jitter sensitivity. In addition to high-speed CT $\Delta\Sigma$ modulators, ISI reduction is also of great importance in high-resolution but low-speed ADCs/DACs, such as those used in high quality audio applications. A large value of $M$ is common in high-quality audio DACs. As an example, the modulator in [15] has a segmented DAC with both the primary and secondary DACs having 32 elements each. In this scenario, the signal swing loss for the proposed technique is small. In summary, the proposed technique is suitable for a wide range of multi-bit $\Delta\Sigma$ modulators despite its signal swing constraint.

## ACKNOWLEDGMENT

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TABLE II
COMPARISON OF DIFFERENT TECHNIQUES FOR DIFFERENT $\max\{NTF(\omega)\}$ AND $M = 16$

| | $\max\{NTF(\omega)\}$=2 | | | $\max\{NTF(\omega)\}$=3 | | | $\max\{NTF(\omega)\}$=4 | | |
|---|---|---|---|---|---|---|---|---|---|
| | Ampl.(dBFS) | SNDR(dB) | SFDR(dB) | Ampl.(dBFS) | SNDR(dB) | SFDR(dB) | Ampl.(dBFS) | SNDR(dB) | SFDR(dB) |
| Ideal | -3 | 96.1 | $> 120$ | -4.4 | 94.7 | $> 120$ | -6.3 | 92.8 | $> 120$ |
| MMS [14] | -3 | 74.9 | 91.8 | -4.4 | 74.3 | 96.5 | -6.3 | 72.4 | 96.7 |
| ISI shaping [15] | -3 | 77.5 | 79.9 | -4.4 | 77.6 | 84.6 | -6.3 | 72.3 | 86.6 |
| This work | -3 | 88.6 | $> 110$ | -4.4 | 88.4 | $> 110$ | -6.3 | 87.4 | $> 110$ |

TABLE III
COMPARISON OF DIFFERENT TECHNIQUES FOR DIFFERENT $\max\{NTF(\omega)\}$ AND $M = 32$

| | $\max\{NTF(\omega)\}$=2 | | | $\max\{NTF(\omega)\}$=3 | | | $\max\{NTF(\omega)\}$=4 | | |
|---|---|---|---|---|---|---|---|---|---|
| | Ampl.(dBFS) | SNDR(dB) | SFDR(dB) | Ampl.(dBFS) | SNDR(dB) | SFDR(dB) | Ampl.(dBFS) | SNDR(dB) | SFDR(dB) |
| Ideal | -1.5 | 103.7 | $> 130$ | -2.8 | 102.4 | $> 130$ | -4.4 | 100.8 | $> 130$ |
| MMS [14] | -1.5 | 82.3 | 105 | -2.8 | 81.7 | 105 | -4.4 | 80.4 | 105 |
| ISI shaping [15] | -1.5 | 78 | 79.9 | -2.8 | 79.9 | 83 | -4.4 | 80.5 | 85 |
| This work | -1.5 | 90.1 | $> 110$ | -2.8 | 89.6 | $> 110$ | -4.4 | 89.8 | $> 110$ |

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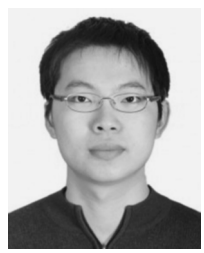
**Arindam Sanyal** received his B.E. degree from Jadavpur University, India, in 2007 and his M.S. degree from the Indian Institute of Technology, Kharagpur, India, in 2009. He is a Ph.D. student in the integrated circuits and systems track at the University of Texas, Austin, TX, USA. He has worked as a Graduate Research intern at Intel Austin and at Silicon Laboratories, Austin. His current research interests are VCO-based ADC design and error correction in multi-bit $\Delta\Sigma$ DACs.



**Long Chen** received the B.Eng. degree from the Institute of Microelectronics, Tsinghua University, Beijing, China, in 2011. He is currently working towards the Ph.D. degree in the electrical and computer engineering at University of Texas, Austin, TX, USA. His current research is focused on low power mixed-signal circuit design and CMOS RF biosensors design. He received the Second Prize in the 25th Intercollegiate Physics Competition in 2009, the Tsinghua First Class Academic Excellence Scholarship in 2009 and 2010, and the Microelectronics and Computer Development (MCD) Fellowship from UT-Austin in 2011.

**Nan Sun** received the B.S. degree from Tsinghua University, China, in 2006, where he ranked top in EE Department and graduated with the highest honor. He received the Ph.D. degree from Harvard University, Cambridge, MA, USA, in 2010. He is an Assistant Professor at the University of Texas, Austin, TX, USA. Dr. Sun received the 1st-class Outstanding Student Award from Tsinghua University each year from 2003 to 2006. He won the Top Prize in the Intercollegiate Physics Competition in 2003. He is the recipient of Samsung Fellowship, Hewlett Packard Fellowship, and Analog Devices Outstanding Student Designer Award in 2003, 2006, and 2007, respectively. He also won Harvard Teaching Award in three consecutive years: 2008, 2009, and 2010. He received NSF Early Career Award in 2013. He currently serves in the TPC of ASSCC and as the guest editor for IEEE *Internet of Things Journal*. His research interests include: 1) analog, mixed-signal, and RF integrated circuits; 2) miniature spin resonance systems; 3) low-cost medical imaging systems; and 4) sensors and actuators.