An Energy-Efficient Low Frequency-Dependence Switching Technique for SAR ADCs

Arindam Sanyal, *Student Member, IEEE*, and Nan Sun, *Member, IEEE*

***Abstract*—This brief presents a highly energy-efficient switching scheme for successive approximation register (SAR) analog-to-digital converters that achieves a 95% reduction in switching energy over the conventional SAR. The switching energy has been calculated by taking into account both the power drawn from reference and the power consumed by the switches themselves. The frequency dependence of the switching energy has been studied and the proposed technique presents ways to maintain high energy efficiency over the entire frequency range of operation. The results have been verified through behavioral and SPICE simulations.**

***Index Terms*—Analog-to-digital converter (ADC), digital-to-analog converter (DAC), successive approximation register (SAR), switching energy.**

I. Introduction

A successive approximation register (SAR) analog-to-digital converter (ADC) is a very attractive solution for low-power analog-to-digital conversion. The highly digital nature of a SAR ADC makes it very amenable to technology scaling. Combined with low power consumption, the digital nature of a SAR ADC can exploit the benefits of the ever-shrinking technology nodes. For these reasons, the SAR ADC has recently captured the attention of the research community [1]–[4] and is increasingly being used in different applications. On one hand, medium-resolution SAR ADCs are increasingly finding use in very high sampling rate (200–500 MS/s) applications [2]. On the other hand, low-frequency ultralow-power SAR ADCs are being used in biomedical applications and low energy radios [5]–[9]. In many cases, the digital-to-analog converter (DAC) can contribute a significant part toward the total power consumption of the SAR ADC. This has brought to fore the challenge of further reducing the power consumption of the DAC. Unfortunately, the conventional DAC is not very power efficient, and more so if its initial guess of the input is wrong. Many studies have been conducted on reducing the switching power of the DAC. The split-capacitor technique of [10] achieves 37% savings in switching energy over the conventional switching technique. The technique in [11] combines the split-capacitor technique with an energy-saving method to achieve 56% savings in switching energy. The monotonic switching scheme reported in [12] has an 81% reduction in switching energy. The $V_{\rm cm}$-based switching techniques of [13] and [14] can reduce the switching energy by 88% compared with a conventional SAR (for a single-ended implementation the energy savings in [14] is 93% but reduces to 88% for a differential configuration). An energy saving of 98% has been reported in [15], but the technique requires accurate $V_{\rm cm}$.

All the switching energy reduction techniques reported in [10]–[14] only account for the power drawn from the reference but largely ignore the power dissipated in driving the switches. As will be shown in this brief, the energy spent in driving the switches can form a significant part of the overall switching energy, particularly for the highly energy-efficiency techniques. To clearly differentiate the two components of the switching energy, henceforth the switching energy drawn from the reference will be denoted by $E_{\rm ref}$ and the switching energy spent on driving the switches will be denoted by $E_{\rm sw}$. $E_{\rm ref}$ is independent of sampling frequency, but $E_{\rm sw}$ increases with frequency. For the ultralow-power SAR ADCs, $E_{\rm ref}$ is the major contributor to the total switching energy of the DAC. For the high-frequency SAR ADCs, $E_{\rm sw}$ contributes more toward the total switching energy and, hence, it is important to find ways of reducing both $E_{\rm ref}$ and $E_{\rm sw}$.

A new energy-efficient switching technique, with an energy savings of 95%, is presented in this brief. A way to reduce $E_{\rm ref}$ is to reduce the number of capacitors in the DAC. The proposed technique achieves $4\times$ reduction in the total capacitance compared with a conventional SAR with the same resolution. The proposed technique further reduces $E_{\rm ref}$ by ensuring that no energy is drawn from the reference during the first 2 cycles. The proposed technique ensures that $E_{\rm sw}$ is reduced by adopting a scheme that has only one switching event per cycle. This is a significant improvement over the conventional scheme, which has at least two transitions each cycle and can have four transitions if its initial guess is wrong. The $V_{\rm cm}$-based switching scheme has two switching events every cycle. The monotonic switching of [12] has one switching every cycle, but it will be shown in Section II that the proposed technique offers higher energy efficiency by using a different switching sequence. In addition, the proposed technique uses fewer capacitors and, hence, fewer switches. This also reduces $E_{\rm sw}$, in addition to reducing $E_{\rm ref}$. In this brief, the focus is primarily on medium-resolution low-power SAR ADCs. Hence, the proposed technique is presented for a top-plate sampling SAR. However, the proposed technique can be easily extended to bottom-plate sampling SAR ADC. The proposed switching technique is discussed in detail in Section II and compared with the existing art. The conclusion is in Section III.

Manuscript received October 29, 2013; accepted January 18, 2014. Date of publication February 27, 2014; date of current version May 14, 2014. This brief was recommended by Associate Editor X. Jiang.

The authors are with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78712 USA (e-mail: arindam3110@utexas.edu; nansun@mail.utexas.edu).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2014.2304890

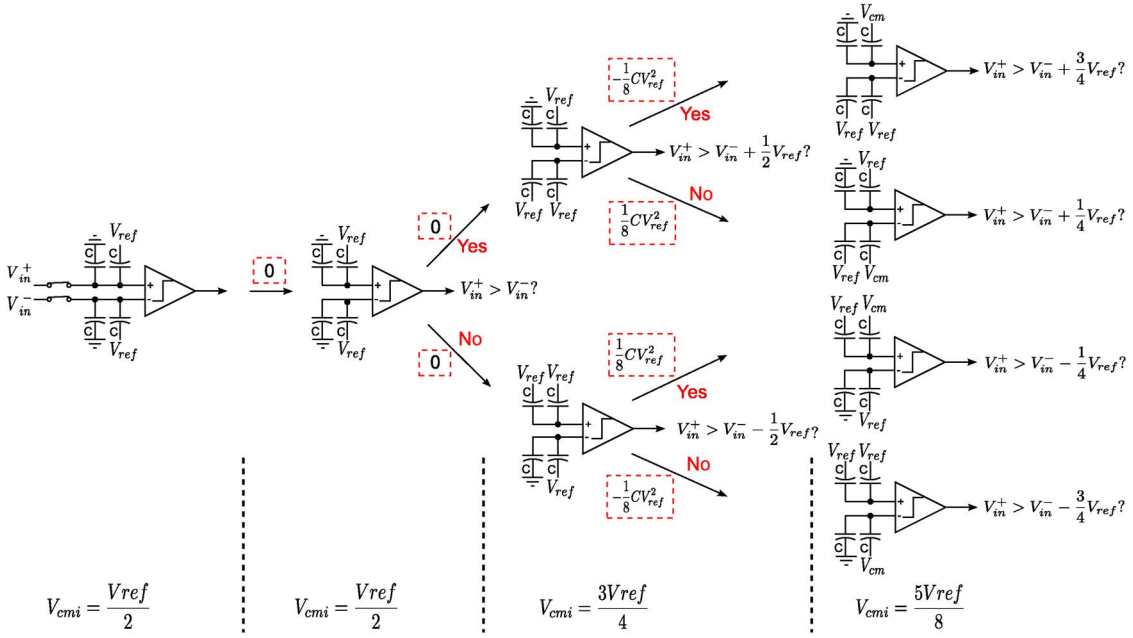

Fig. 1. Proposed switching technique illustrated for a 3-bit SAR ADC.

II. Proposed Switching Technique

A. Switching Energy Drawn From References

1) Four Times Reduction in Capacitance: An example 3-bit SAR ADC, which makes use of the proposed switching technique, is shown in Fig. 1. The analog supply $V_{\rm cc}$ is used as $V_{\rm ref}$ in the proposed design. The proposed technique can be easily generalized to a SAR ADC with any resolution. It can be seen that the proposed technique requires a total capacitance of 4 C for a 3-bit ADC compared with a 16-C total capacitance required in the conventional method. Thus, the proposed technique achieves a 4× reduction in capacitance of the DAC. A capacitance reduction by 2× has been already widely reported in literature [4], [12]–[14]. The proposed scheme achieves a reduction of 4× by switching the last unit capacitor between $(V_{\rm ref}, V_{\rm cm})$ instead of $(V_{\rm ref}, 0)$. This allows an additional comparison and the outputs of the comparator can be directly combined with the DAC outputs to generate the final digital code. The $V_{\rm cm}$ value does not have to be accurate nor does its use dissipate more power. This is due to two reasons. The reference level, i.e., $V_{\rm cm}$, is used only for the last unit capacitor, and an error in its value does not degrade the resolution seriously. For a 10-bit SAR with a full-swing input of $(-1\ {\rm V}, 1\ {\rm V})$, a 50-mV deviation in $V_{\rm cm}$ value degrades the signal-to-quantization-noise ratio from 61.96 dB (10 bits) to 61.84 dB (9.9 bits). In addition, no energy is drawn from $V_{\rm cm}$ during the comparison cycles.

2) Zero Switching Energy in the First 2 Cycles: The use of top-plate sampling ensures that $E_{\rm ref} = 0$ in the first cycle [12]–[14]. The concept of reducing the switching energy in the second cycle is introduced in Fig. 2. Fig. 2(a) indicates the simplified initial switching sequence proposed in this brief, as shown in Fig. 1, whereas Fig. 2(b) shows the initial sequence from [12]. Applying charge conservation on Fig. 2(a), $V_y = V_x + V_{\rm ref}/2$. The switching energy E_1 can be calculated as $E_1 = \{2(V_x - V_y) + V_{\rm ref}\}CV_{\rm ref} = 0$. Thus, no energy is drawn from $V_{\rm ref}$. However, if the sequence is reversed as is done in [12] [see Fig. 2(b)], applying charge conservation gives

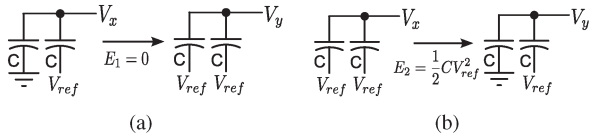

Fig. 2. Illustration of the idea behind energy saving.

$V_y = V_x - V_{\rm ref}/2$. Hence, the switching energy E_2 is given by $E_2 = (V_x - V_y)CV_{\rm ref} = CV_{\rm ref}^2/2 \neq 0$. Applying this concept also ensures that $E_{\rm ref} = 0$ during the second cycle, as shown in Fig. 1. Grounding the MSB capacitor initially also provides another important advantage over the monotonic switching technique of [12] in terms of the common-mode voltage variation at the comparator's inputs. The common-mode variation at the comparator's inputs is given by $\Delta V_{\rm cm} = V_{\rm cmi} - V_{\rm ref}/2$, where $V_{\rm cmi}$ is the common-mode voltage at the comparator's inputs. A $\Delta V_{\rm cm}$ can cause an input-dependent offset resulting in harmonic distortion at the output. The common-mode voltage variations for the conventional method, the monotonic switching scheme of [12], and the proposed technique are shown in Fig. 3. The $\Delta V_{\rm cm}$ with the proposed technique is half of that of the monotonic switching technique. In addition, $V_{\rm cmi}$ for the proposed technique gradually converges toward $V_{\rm ref}/2$, unlike the monotonic switching technique in which $V_{\rm cmi}$ drifts away from $V_{\rm ref}/2$ every cycle and finally settles at "0". As shown in Fig. 3, for the proposed scheme, $\Delta V_{\rm cm}$ is very small for the last several comparison cycles. In addition, note that the comparator input voltages are always bounded by $(0, V_{\rm ref})$. The proposed technique does not reduce the achievable signal swing.

3) Comparison With Other Techniques: The proposed switching scheme ensures that only one capacitor is switched in every comparison cycle, which also helps in reducing the total switching energy. As shown in Fig. 1, the proposed technique ensures that, for SAR ADCs with resolution less than or equal to 3 bits, the average $E_{\rm ref}$ is zero for all the cycles. The negative switching energy in the last cycle is not nonphysical; rather, it implies that the DAC gives back energy

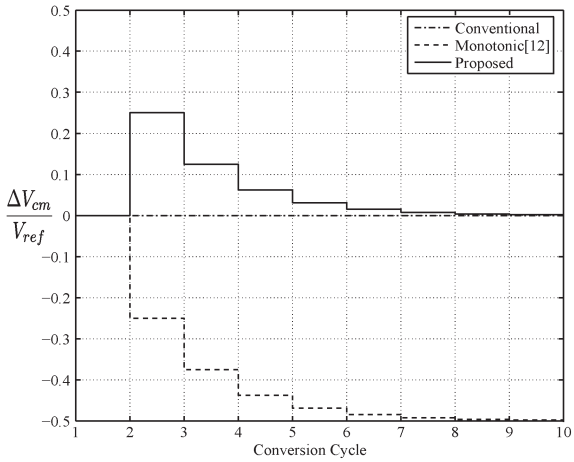

Fig. 3. Deviation of $V_{\rm cmi}$ from $V_{\rm ref}/2$ for a 10-bit SAR ADC.

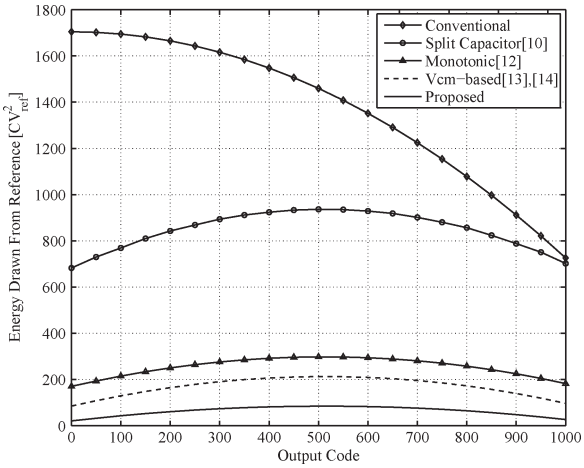

Fig. 4. Comparison of E_{ref} for different switching techniques for a 10-bit SAR ADC.

to the reference voltage sources. However, for an n-bit SAR ADC, with $n > 3$, the average $E_{\rm ref}$ is nonzero and is given by $E_{\rm ref} = (\sum_{i=2}^{n-2} 2^{n-3-i}) C V_{\rm ref}^2$. Fig. 4 shows the comparison of $E_{\rm ref}$ for the different techniques for a 10-bit SAR. As can be seen, the proposed scheme has a significantly lower $E_{\rm ref}$ than the other techniques.

B. Energy Spent on Driving Switches

A considerable amount of energy, i.e., $E_{\rm sw}$, is dissipated on driving the switches connecting the capacitors in the DAC to the reference voltages. Unfortunately, $E_{\rm sw}$ cannot be set to zero unlike $E_{\rm ref}$. Here, the focus will be on showing how the total switching energy is affected by $E_{\rm sw}$. For this purpose, behavioral simulations using MATLAB will be used to compare the different switching techniques and illustrate how each of them performs once $E_{\rm sw}$ is taken into account.

Let the unit capacitor in the DAC be denoted by C_0, the resistance of the unit nMOS switch be R_0, and its gate capacitance be C_{R0}. It will be assumed that the unit pMOS switch is sized to give the same resistance as R_0. Let the ith capacitor in the DAC have a capacitance of C_i and the resistance of the ith nMOS switch connecting it to the reference be R_i. We will assume that, for an n-bit conventional DAC, the switches are sized such that the RC time constant of all switches are the same, i.e., $R_i C_i = R_j C_j \; \forall i, j \in [0, n], i \neq j$. A first-order estimate of R_i can be obtained from

$$R_i = \min\{0.8T_s/(\beta \cdot C_i), 0.8T_{\rm DAC}/(\beta \cdot C_i)\} \qquad (1)$$

where T_s is the time during which the input is sampled, β is the number of time constants required for the virtual node to settle to n-bit accuracy, and $T_{\rm DAC}$ is the DAC settling time given by $[(T_{\rm clk} - T_s)/n - T_{\rm comp} - T_{\rm logic}]$. $1/T_{\rm clk}$ is the sampling frequency, $T_{\rm comp}$ is the time required by the comparator to resolve its input, and $T_{\rm logic}$ is the propagation delay of the control logic. The limits placed on R_i come from two different time constant requirements: 1) the sampling time constant T_s/β and 2) the DAC settling time constant $T_{\rm DAC}/\beta$. The factor of 0.8 in (1) is used to account for the effect of parasitic gate capacitance of the switches. To keep the discussion simple, the bottom-plate parasitic capacitance to substrate has not been taken into account. Strictly speaking, $(T_{\rm comp} + T_{\rm logic})$ is not a fixed number but depends on the signal swing at the comparator's inputs and the specific comparison cycle. For our first-order model, having a fixed value for $(T_{\rm comp} + T_{\rm logic})$ will not take away too much from the accuracy of the results while still providing a good understanding of how the switching power might vary in an actual scenario. As can be seen from (1), an upper limit is placed on the maximum sampling rate of the SAR ADC by T_s $(T_{\rm comp} + T_{\rm logic})$ and the resolution of the ADC. Once R_i is known, the capacitance C_{Ri} can be extracted from SPICE simulation. Thus, the gate capacitance of the smallest switch used in the DAC, i.e., C_{R0}, is given by $\max\{\alpha/R_i, C_{\rm min}\}$, where α is a function of the process parameters, and $C_{\rm min}$ is the gate capacitance of the minimum-sized switch available in that process. $E_{\rm sw}$ is proportional to $\sum_i C_{Ri} V_{\rm cc}^2$. Due to the lower limit imposed by $C_{\rm min}$, $E_{\rm sw}$ slowly increases with frequency at low sampling frequencies. At high sampling frequencies (low $T_{\rm clk}$), $E_{\rm sw}$ is proportional to $\alpha V_{\rm cc}^2/T_{\rm DAC}$. Since $T_{\rm DAC}$ starts approaching zero at low $T_{\rm clk}$, $E_{\rm sw}$ shows a sharp increase.

Fig. 5 shows the variation of the total switching energy, i.e., $E_{\rm tot} = E_{\rm ref} + E_{\rm sw}$, for two different processes, i.e., 180 and 65 nm, and two different unit capacitor values, i.e., 20 and 2 fF. The supply voltage for the 180-nm process was 1.8 V, and the supply voltage for the 65-nm process was 1 V. To model the interconnect, wiring, and comparator's gate capacitances, 10% of the total capacitance in the DAC was added to the comparator's inputs.

The frequency dependence of the switching energy can be clearly seen. The conventional method and the split-capacitor scheme of [10] show a lesser increase in $E_{\rm tot}$ with frequency than the other schemes. This is because both these schemes have a large $E_{\rm ref}$. The $V_{\rm cm}$-based technique of [13] and [14] shows the largest increase in $E_{\rm tot}$ with frequency. This is because the nMOS switches connected to $V_{\rm cm}$ have to be wider than the nMOS switches connected to ground, due to the reduced gate-to-source voltage. In addition, the $V_{\rm cm}$-based technique needs to drive the wider nMOS switches twice every cycle. This leads to a larger $E_{\rm sw}$, which results in a rapidly increasing $E_{\rm tot}$ with frequency. The proposed technique has the lowest $E_{\rm sw}$ among the existing techniques. The proposed technique offers an energy savings of 95% at 10 MHz and 91% at 70 MHz when compared with the conventional scheme for the 180-nm process and $C_0 = 20$ fF. In contrast, the $V_{\rm cm}$-based technique [13], [14] offers an energy savings of 86% at 10 MHz

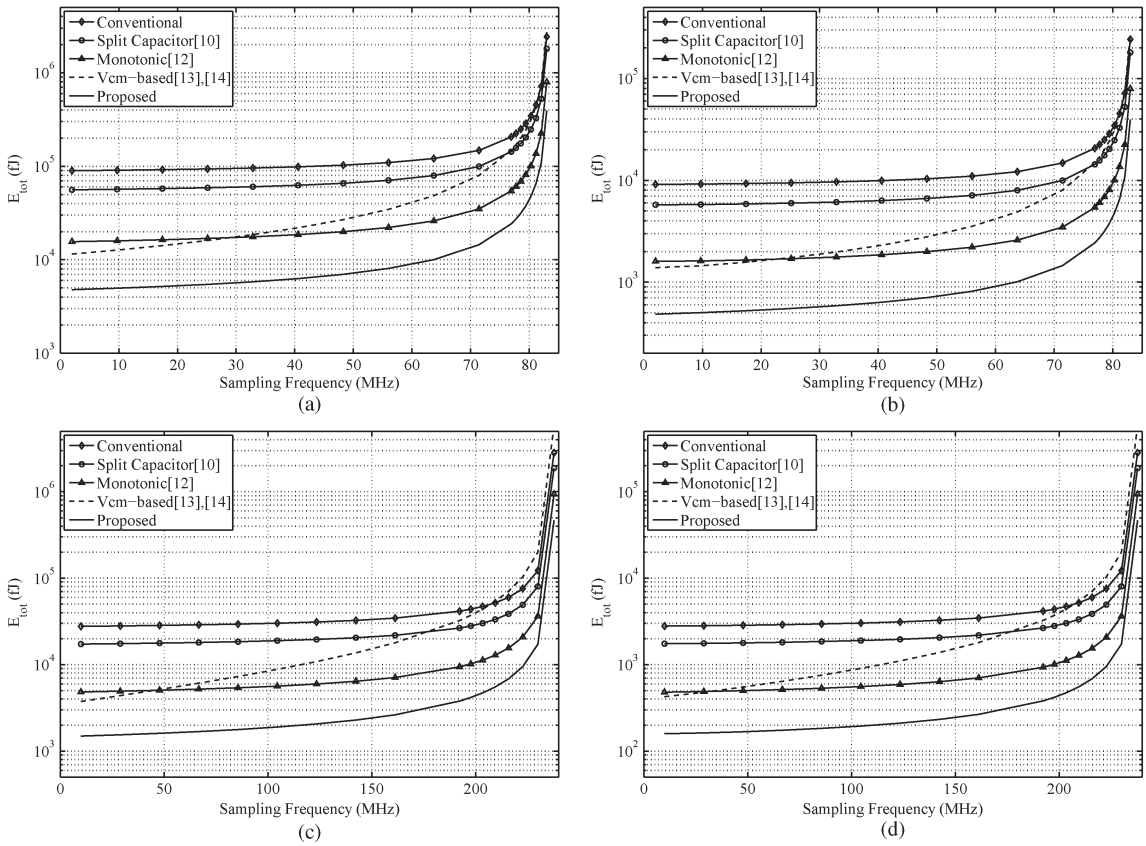

Fig. 5. $E_{\rm tot}$ versus sampling frequency for 180 nm. (a) $C_0 = 20$ fF, (b) $C_0 = 2$ fF and 65 nm, (c) $C_0 = 20$ fF, and (d) $C_0 = 2$ fF for a 10-bit SAR ADC.

TABLE I
COMPARISON OF SWITCHING TECHNIQUES FOR $C_0 = 20$ fF AT 180 nm FOR A 10-BIT SAR ADC

			Low Freq.(10 MHz)		Medium Freq.(40 MHz)		High Freq.(70 MHz)	
switching method	C_{tot}(pF)	E_{ref}(pJ)	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM
conventional	20.48	89.36	1.34	88.58	9.25	96.29	58.42	144.32
split-capacitor [10]	20.48	56.17	1.01	55.85	6.92	61.62	43.73	97.56
monotonic [12]	10.24	14.56	0.46	14.67	3.08	17.23	19.47	33.24
V_{cm}-based [13], [14]	10.24	11.08	1.60	12.38	10.89	21.45	68.79	77.99
this work	5.12	4.27	0.21	4.38	1.54	5.67	9.74	13.68

TABLE II
COMPARISON OF SWITCHING TECHNIQUES FOR $C_0 = 2$ fF AT 65 nm FOR A 10-BIT SAR ADC

			Low Freq.(10 MHz)		Medium Freq.(120 MHz)		High Freq.(200 MHz)	
switching method	C_{tot}(pF)	E_{ref}(pJ)	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM
conventional	2.05	2.76	0.03	2.73	0.36	3.05	1.39	4.06
split-capacitor [10]	2.05	1.72	0.02	1.70	0.24	1.93	0.93	2.60
monotonic [12]	1.02	0.44	0.01	0.44	0.12	0.55	0.46	0.88
V_{cm}-based [13], [14]	1.02	0.34	0.08	0.42	0.76	1.08	2.90	3.17
this work	0.51	0.13	0.01	0.14	0.06	0.19	0.23	0.36

that drops to 46% at 70 MHz. The monotonic switching technique [12] has an energy savings of 83% at 10 MHz and 77% at 70 MHz. Both $E_{\rm ref}$ and $E_{\rm sw}$ scale very well with C_0, as shown in Fig. 5(a) and (b), except for at low frequencies, where $E_{\rm sw}$ does not scale with C_0 as the switch capacitances start hitting the lower limit $C_{\rm min}$. $E_{\rm tot}$ also scales very well with the technology node, as shown in Fig. 5(c) and (d).

To provide a better comparison of the different switching techniques across the process nodes and C_0 values, a figure-of-merit (FoM), which is similar to the Walden FoM, has been used. For an n-bit SAR, the FoM used is defined by $FoM \equiv (E_{\rm ref} + E_{\rm sw})/(2^n)$. The results of the comparisons, for a 10-bit SAR ADC, are summarized in Tables I and II. It can be seen that, compared with the other methods, the proposed technique has a superior FoM over the entire frequency range of operation. The proposed technique can be seen to benefit from technology scaling and offers impressive FoM, which presents exciting opportunities for low-power SAR designs. As an example, the conventional DAC in the ultralow-power SAR in [6] consumes 33 nW out of a total power of 53 nW. If the proposed switching technique was used instead, the total power of the ADC could be reduced to 21.65 nW, which is a reduction of roughly 2.5 times. For the 7 μW SAR in [7], the DAC contributes 92% of the total power, whereas the DAC of the 6 nW SAR in [8] contributes 58% of the total power. The DAC used in the low-power radio in [9] consumes 25% of the total power. These low-power SAR architectures present opportunities for greatly reducing the power consumption further by adopting

TABLE III
COMPARISON OF SWITCHING TECHNIQUES FOR $C_{tot} = 512$ fF AT 65 nm FOR A 10-BIT SAR ADC

			Low Freq.(10 MHz)		Medium Freq.(120 MHz)		High Freq.(200 MHz)	
switching method	C_0(fF)	E_{ref}(pJ)	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM
conventional	0.5	0.69	0.03	0.69	0.10	0.77	0.35	1.02
split-capacitor [10]	0.5	0.43	0.02	0.44	0.07	0.49	0.24	0.65
monotonic [12]	1.0	0.22	0.01	0.23	0.06	0.28	0.23	0.45
V_{cm}-based [13], [14]	1.0	0.17	0.08	0.24	0.39	0.55	1.46	1.59
this work	2.0	0.13	0.01	0.14	0.06	0.19	0.23	0.36

the proposed switching technique. The proposed technique also paves the way for a highly energy-efficient medium-resolution SAR at high sampling rates. As shown in Table II, even at a high sampling rate of 200 MHz, the FoM for the proposed technique is only 0.36 fJ/conversion step. Assuming that a low-power comparator can be designed, it is not too difficult to envision that future SAR ADCs incorporating the proposed technique will consume only a fraction of the power of a pipelined ADCs while operating at speeds ranging from 1 to 200 MS/s.

C. Discussion on Noise and Matching

The discussion so far has focused on the comparison of switching energy of the different techniques for the same unit capacitance. However, it is also useful to compare the different switching techniques for the same $C_{\rm tot}$. The proposed technique reduces $C_{\rm tot}$ by $4\times$ compared with the conventional SAR ADC, which might raise concerns about the increase in the kT/C noise. A comparison of the different switching techniques is presented in Table III for the same $C_{\rm tot}$. It can be seen from Table III that the proposed technique has the lowest switching energy compared with the other techniques for the same $C_{\rm tot}$ and still achieves 80% energy savings when compared with the conventional technique. The monotonic technique of [12] achieves a 67% energy savings and the $V_{\rm cm}$-based technique achieves a 65% energy savings over the conventional technique for the same $C_{\rm tot}$. With a 1-V supply, the quantization noise for a 10-bit ADC is 564 μV rms. To make the kT/C noise the same as the quantization noise, C_u needs to be as small as 0.1 fF. A very small unit capacitance implementation is not a major problem as has been shown in [17], which uses a C_u as small as 50 aF.

The use of the proposed switching technique allows the unit capacitance to be increased by $4\times$ compared with the conventional technique when designed for the same kT/C noise. This eases the implementation issues involving fabrication of very small capacitors in silicon.

III. CONCLUSION

A highly energy-efficient switching technique for SAR ADCs has been presented in this brief and compared with different switching techniques reported in literature. The energy consumed by the switches has been taken into account and has been shown to degrade the overall energy savings. It has been also shown that the proposed technique can offer a high energy efficiency over a wide band of frequency. The proposed scheme benefits from technology scaling and its FoM for switching energy can be as low as 0.14 fJ/conversion step in the 65-nm process. Hence, with a well-designed low-power comparator, the proposed technique can be envisioned to offer an overall conversion efficiency of sub-fJ/step in an advanced technology node.

REFERENCES

[1] J. H. Cheong, K. L. Chan, P. B. Khannur, K. T. Tiew, and M. Je, "A 400-nW 19.5 fJ/conversion step 8-ENOB 80-KS/s SAR ADC in 0.18-μm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 7, pp. 407–411, Jul. 2011.

[2] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, Apr. 2007.

[3] V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. Van der Plas, and J. Craninckx, "An 820 μW 9 b 40 MS/s noise-tolerant dynamic-SAR ADC in 90 nm digital CMOS," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 238–239.

[4] A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "A 0.5V 1.1 MS/sec 6.3fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1022–1030, Apr. 2012.

[5] N. Verma and A. P. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1196–1295, Jun. 2007.

[6] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-KS/s SAR ADC in 0.13-μm CMOS for medical implant devices," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.

[7] T. G. R. Kuntz, C. R. Rodrigues, and S. Nooshabadi, "An energy-efficient 1MSps 7 μW 11.9 fJ/conversion step 7 pJ/sample 10-bit SAR ADC in 90 nm," in *Proc. IEEE ISCAS*, May 2011, pp. 261–264.

[8] R. Sekimoto, A. Shikata, and H. Ishikuro, "A power scalable SAR-ADC in 0.18 μm-CMOS with 0.5V nano-watt operation," in *Proc. IEEE ISCAS*, 2011, pp. 89–94.

[9] P. J. A. Harpe, C. Zhou, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[10] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 184–187.

[11] Y. Chang, C.-S. Wang, and C.-K. Wang, "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," in *Proc. IEEE ASSCC Dig. Tech. Papers*, Nov. 2007, pp. 228–231.

[12] C. C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[13] Y. Zhu, C.-H. Chan, U. F. Chio, S.-W. Sin, U. Seng-Pan, R. P. Martins, and F. Maloberti, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[14] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electron. Lett.*, vol. 46, no. 9, pp. 620–621, Apr. 2010.

[15] A. Sanyal and N. Sun, "SAR ADC architecture with 98% reduction in switching energy over conventional scheme," *Electron. Lett.*, vol. 49, pp. 248–249, 2013.

[16] W. Liu, P. Huang, and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2661–2672, Nov. 2011.

[17] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Nov. 2013.