# A 0.95-mW 6-b 700-MS/s Single-Channel Loop-Unrolled SAR ADC in 40-nm CMOS

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***Abstract*—This brief presents a low-power and high-speed single-channel successive approximation register (SAR) analog-to-digital converter (ADC). It uses a loop-unrolled architecture with multiple comparators. Each comparator is used not only to make a comparison but also to store its output and generate an asynchronous clock to trigger the next comparator. The SAR logic is significantly simplified to increase speed and reduce power. The comparator offset and decision time are optimized with a bidirectional single-side switching technique by controlling the input common-mode voltage $V_{\rm cm}$. To remove the nonlinearity due to the comparators' offset mismatch, a simple and effective $V_{\rm cm}$-adaptive offset calibration technique is proposed. The prototype ADC in 40-nm CMOS achieves a 35-dB signal to noise-plus-distortion ratio and a 48-dB spurious-free dynamic range at a 700-MS/s sampling rate. It consumes 0.95 mW, leading to a Walden figure-of-merit (FOM) of 30 fJ/conversion-step and a Schreier FOM of 153.4 dB.**

***Index Terms*—Analog-to-digital converter (ADC), high speed, offset calibration, successive approximation register (SAR).**

## I. Introduction

HIGH-SPEED low-resolution analog-to-digital converters (ADCs) are required by many demanding applications, such as high-speed serial link transceivers and communication systems. Compared with pipelined and $\Delta\Sigma$ ADCs, SAR ADCs are more scaling friendly due to their mostly digital architecture and power efficiency, particularly at low sampling rates [1]–[3]. In order to increase the speed of SAR ADCs, several techniques have been developed [4]–[12]. The first asynchronous SAR ADC was proposed in [4] to shorten the time duration of each comparison cycle. The SAR ADC speed can also be improved by using multibit-per-cycle architectures to reduce the number of comparisons, however at the cost of increased hardware complexity [6], [7]. Other effective high-speed techniques include using alternate comparators to save the comparator reset time [8] or pipelining two-stage SAR ADCs [9]. Recently, several works arrange multiple comparators to further increase the speed [10]–[12]. A binary-search ADC was proposed in [10], which describes a transitional structure between flash and SAR ADCs. However, the hardware cost is high in [10] as this technique requires additional switching networks and $2N-1$ comparators for an $N$-bit design. The loop-unrolled architecture of [11] and [12] employs a dedicated comparator for each comparison cycle. The comparison result is stored directly at the comparator output. As a result, the SAR logic is greatly simplified, leading to reduced power and delay. Although more comparators are used compared to the conventional SAR architecture, the total comparator power does not increase since each of them is fired only once during the whole conversion. Nevertheless, the comparator common-mode voltage $V_{\rm cm}$ varies significantly and eventually goes to $V_{\rm DD}$ in [11] and [12], resulting in large comparator offsets and reduced linearity. Both works [11] and [12] require complicated calibrations for comparators' offset mismatches, which increase the power consumption and design complexity.

This brief proposes a novel loop-unrolled SAR ADC with two new key techniques to improve the linearity and the power efficiency. First, in order to address the large $V_{\rm cm}$ variation issue, a bidirectional single-side (BSS) switching technique is employed. It reduces the comparator offset by appropriately controlling $V_{\rm cm}$. The comparator decision time is also optimized. In addition, it allows a reduced number of digital-to-analog converter (DAC) unit capacitors, which reduces the DAC area and the routing parasitics. Second, to further improve the linearity, a novel $V_{\rm cm}$-adaptive offset calibration technique is proposed to calibrate the comparators' offset mismatch. The proposed calibration technique has very low hardware complexity. It can calibrate the comparator offset at its operating $V_{\rm cm}$ following the proposed switching procedure. A prototype ADC is implemented in 40-nm CMOS. It achieves a 34.8-dB signal to noise-plus-distortion ratio (SNDR) and a 47.8-dB SFDR at a sampling rate of 700 MS/s while consuming only 0.95-mW power from a 1.2-V supply.

This brief is organized as follows. Section II describes the proposed SAR ADC architecture. Section III presents the circuit implementation. Section IV shows the measured results. The conclusion is drawn in Section V.

## II. Proposed SAR ADC Architecture

The proposed 6-b SAR ADC architecture is shown in Fig. 1(a). It consists of a clock generator, a sampling network, two capacitive DACs, six comparators, and a calibration unit. The clock generator generates the required timing phases. The sampling switches $S1$ and $S2$ are bootstrapped to ensure high sampling linearity at high input frequencies. The DACs are implemented using binary weighted capacitors. Small dynamic comparators with offset calibration are used to minimize power consumption. Dynamic OR gates with reset and controlled delay are used to generate the asynchronous clocks. The comparator offset mismatch is foreground calibrated by the calibration unit. The LSB comparator outputs are combined by a NOR gate

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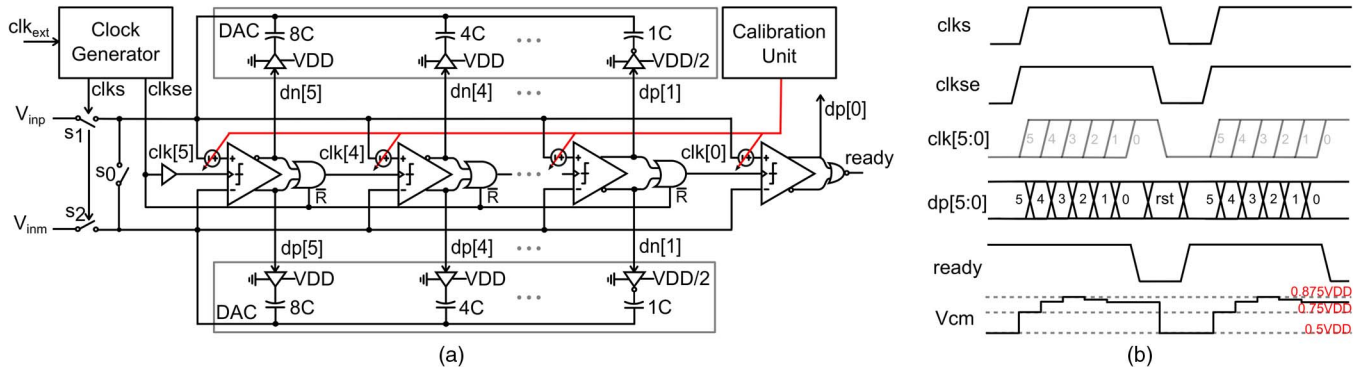


Fig. 1. (a) Architecture and (b) timing diagram of the proposed SAR ADC.

to generate a ready signal, which indicates the end of the whole ADC conversion.

The timing diagram is shown in Fig. 1(b). When clks is low, the input voltages are top plate sampled on the DACs through $S_1$ and $S_2$. All comparators' outputs are reset to low through dynamic OR gates controlled by clkse. The ready signal is reset to high. When the sampling phase ends, both clkse and clks go to high. The MSB comparator is triggered by clk [5] which is a two-gate delay of clkse. Depending on the sampled input voltages, the MSB comparator makes its decisions *dp* [5] and *dn* [5], which directly control the capacitive DACs to perform the proposed switching technique without the need for any shift register-based SAR logic. The dynamic OR gate delay is controlled to provide adequate time for DAC settling. It generates clk [4] to trigger the second MSB comparator. This procedure propagates in a "domino" fashion until the LSB comparison finishes. The ready signal goes to low. The next sampling phases start after the comparator outputs are latched by the falling edge of clkse.

Compared to the conventional SAR ADC, the SAR logic is greatly simplified in this loop-unrolled architecture. There is no need for any shift register-based sequencer or D flip-flop (DFF)-based data storage because all comparator results are directly stored at the comparator outputs. The asynchronous clock is generated easily by ORing the comparators' outputs. The reduced logic complexity reduces the circuit power, minimizes the chip area, and increases the speed. In the proposed architecture, the conversion time is reduced in three ways compared to the conventional asynchronous SAR ADC [4]. First, no DFF or latch delay is needed to store the comparator output. Second, comparators are reset simultaneously, and thus, no comparator reset time is needed for every comparison cycle. The comparator reset time can be a speed bottleneck, particularly in most advanced technology nodes where both logic delay and DAC settling time are small [8]. Third, the proposed design allows independent optimization for each comparison cycle. In other words, each OR gate delay can be adjusted based on the corresponding DAC settling time. The comparator power can also be optimized using the technique in [13]. Overall, the optimized critical path for each comparison cycle in the proposed design can be represented as

$$T = t_{\mathrm{comp,decision}} + \max\{t_{\mathrm{DAC}}, t_{\mathrm{OR}}\}. \quad (1)$$

This design optimizes $t_{\mathrm{comp,decision}}$ by optimizing the comparator input common-mode voltage with a BSS switching technique. $t_{\mathrm{DAC}}$ and $t_{\mathrm{OR}}$ are optimized by using a small unit capacitor and a specially designed dynamic OR gate, respectively, as shown in Section III. Based on SPICE simulation, $t_{\mathrm{DAC}}$ is greater than $t_{\mathrm{OR}}$ for the first 2 MSB bits where the DAC capacitors are large. $t_{\mathrm{OR}}$ dominates over $t_{\mathrm{DAC}}$ for the last 4 LSB bits.

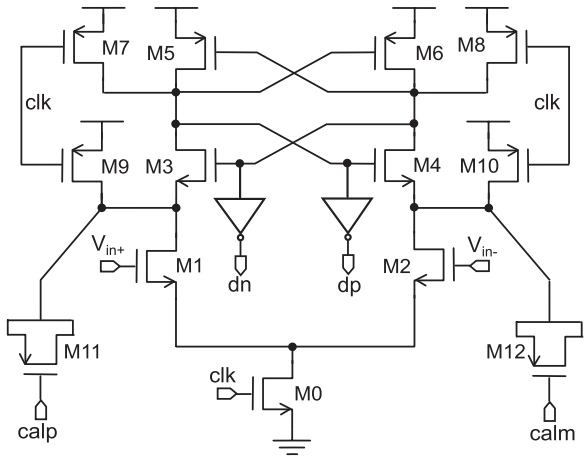


Fig. 2. Dynamic comparator with varactor loading.

## III. Circuit Implementations

### A. Comparator

Fig. 2 shows the dynamic comparator with offset calibration. Two variable MOS capacitors are added at the drain of input transistors $M1$ and $M2$ for calibration purpose. Comparator offset and decision time are two key parameters in this design. Unlike the conventional SAR ADC with one single comparator, the loop-unrolled architecture employs six comparators. All comparators have offsets, and their offset mismatches degrade the ADC linearity. Comparator decision time is in the critical timing path as shown in (1). Thus, it is desirable to design the comparator with small offset and fast decision time. One important factor that influences both offset and decision time is the comparator input common-mode voltage $V_{\mathrm{cm}}$ [14]. A small $V_{\mathrm{cm}}$ is preferred to reduce the offset. The reason is that the preamplification gain is larger at small $V_{\mathrm{cm}}$, which suppresses the offset contribution from the latch. A large $V_{\mathrm{cm}}$ helps reduce the preamplification time, but the time duration of the latch regeneration phase is longer due to the reduction in the preamplification gain [14]. There exists an optimized $V_{\mathrm{cm}}$ for decision time. The simulated $1\sigma$ offset and decision time are shown in Fig. 3. Here, the decision time is defined as the time that it takes for the comparator output differential voltage to

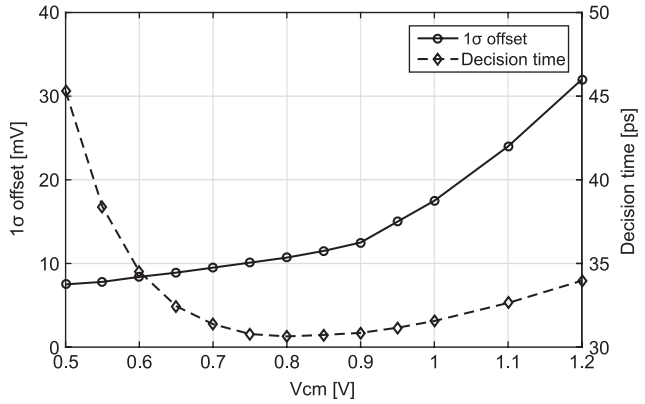


Fig. 3. Simulated comparator offset and decision time at different $V_{\rm cm}$.

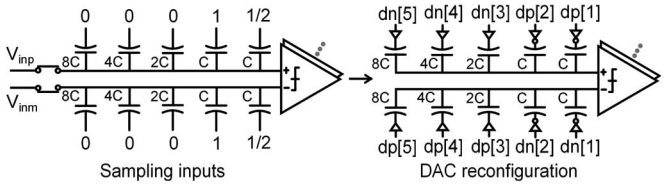


Fig. 4. BSS switching scheme.

reach 0.7 $V_{\rm DD}$ given a 1-mV differential input. It suggests that the optimal value of $V_{\rm cm}$ is around 0.8 V, where the decision time is minimized and the offset is also small.

### B. Modified BSS Switching Technique

A modified BSS switching technique based on [15] and [16] is employed in the design. The BSS technique can reduce the number of unit capacitors by four times compared to the conventional switching technique and two times compared to the monotonic switching technique [11], [12]. The binary capacitors used in the DAC are $[8C_U, 4C_U, 2C_U, C_U, C_U]$ for the 6-b implementation, with a unit capacitor $C_U$ of 1.9 fF. Owing to the small unit capacitor, the DAC settling time $t_{\rm DAC}$ is short, and it is easy to guarantee the settling error to be within 1/2 LSB. No redundancy is provided to avoid additional comparison cycles. The reduced number of unit capacitors reduces the layout complexity since fewer interconnections are needed. The measured result shows that the capacitors are matched well without calibration for a 6-b accuracy with a similar layout strategy in [15].

The proposed BSS switching scheme is shown in Fig. 4. DAC is connected to [0, 0, 0, 1, 1/2] when sampling the inputs, where 0, 1, and 1/2 indicate ground, $V_{\rm DD}$, and $V_{\rm DD}/2$, respectively. The two references $V_{\rm DD}$ and $V_{\rm DD}/2$ are provided off-chip for simplicity, although they can be generated on-chip at low power cost [18]. Instead of switching DAC capacitors from ground to $V_{\rm DD}$ monotonically, the proposed technique switches the first 3 MSB capacitors $[8C_U, 4C_U, 2C_U]$ from ground to $V_{\rm DD}$ and then switches the left-side $C_U$ capacitors from $V_{\rm DD}$ to ground. The right-side $C_U$ is switched from $V_{\rm DD}/2$ to ground similar to [17].

The simulated $V_{\rm cm}$ variation is shown in Fig. 5. In the proposed switching scheme, $V_{\rm cm}$ stays close to 0.8 V after the first comparison cycle, where the optimized decision time is achieved and the comparator offset is kept small. Compared with the monotonic switching scheme in [11] and [12], where

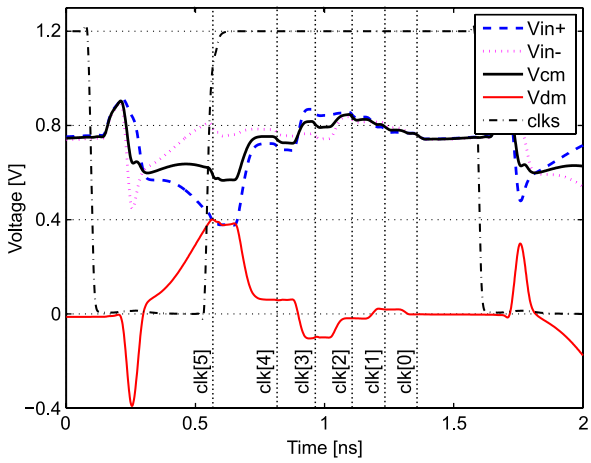


Fig. 5. Simulated time-domain waveforms for comparator inputs Vin+ /Vin−, its common-mode voltage $V_{\rm cm}$, and its differential mode voltage $V_{\rm dm}$.

$V_{\rm cm}$ can converge to $V_{\rm DD}$, the $1\sigma$ offset can be reduced from 32 to 10 mV, and the decision time can be reduced by 10% in the proposed switching technique. Note that $V_{\rm cm}$ decreases slightly when the comparators are fired due to the comparator kick-back noise. The kick-back noise is a common-mode noise to the first order, which does not degrade the linearity for this 6-b ADC.

### C. $V_{\rm cm}$-Adaptive Offset Calibration

In the prototype ADC, the full-scale differential input swing is 1.4 V, and the 1 LSB size is about 20 mV. The optimized comparator $1\sigma$ offset is 10m V, which is comparable to the LSB size. To avoid linearity degradation due to offset mismatch, a $V_{\rm cm}$-adaptive offset calibration technique is proposed. The calibration technique works as follows. When the ADC is in the calibration mode, the calibration control switch $S0$ is on, and a zero differential input voltage is sampled through $S1$ and $S2$ (see Fig. 1). A low-frequency external clock $\rm clk_{ext}$ is provided. Each OR gate's delay is set large enough such that, before each comparator is triggered, its differential inputs settle well and stay close to zero. If there is no offset, each comparator's output jumps between "1" and "0" due to thermal noise. The comparator thermal noise in the design is about 400 $\mu$V, which is much smaller than the offset. With a large offset present, the comparator's output keeps staying at either "1" or "0." The offset can be calibrated by tuning the MOSFET-based varactors shown in Fig. 2, whose values are controlled by its gate voltage calp/calm. The calibration range is designed to be 30 mV which is three times the simulated $1\sigma$ offset. By observing the comparator's output, we can tell whether the comparator offset has been calibrated or not. The calibration is finished when the comparator output is evenly distributed between "1" and "0." 1024 ADC outputs are captured by a logic analyzer during the calibration. The comparator offset is removed when the probability that its output code equals to "1" is around 50%. Note that the probability does not need to be exactly 50% since the calibration accuracy is relaxed for a 6-b design. The measured probability of the comparator outputs being "1" versus its calibration voltage calm for the MSB comparator is plotted in Fig. 6. The proposed calibration is simple as it only requires one additional switch $S0$. It does not require special DAC patterns to generate the operating $V_{\rm cm}$ as in [11] or special input voltages that cause metastability at

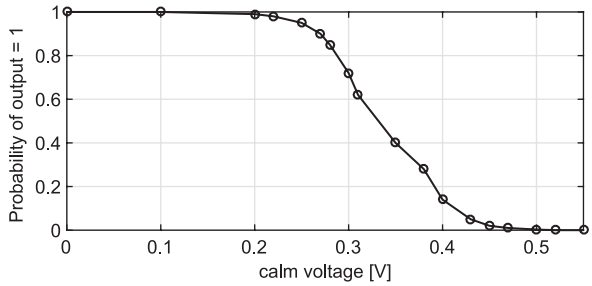


Fig. 6. Probability of MSB comparator output being "1" versus its calm with calp fixed at 1.2 V.

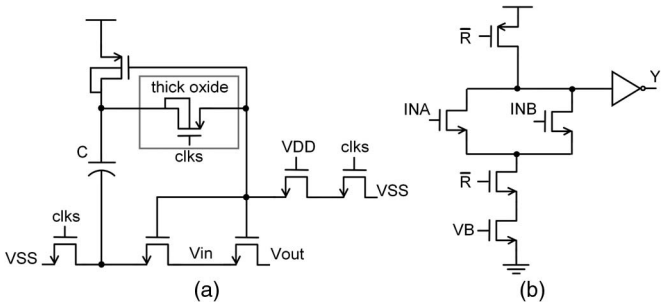


Fig. 7. Schematic of (a) bootstrapped switch and (b) dynamic OR gate.

different comparators as in [12]. Furthermore, since the same DAC switching procedure happens during calibration, each comparator offset is calibrated at the same $V_{\rm cm}$ as that of the normal ADC operation. This is necessary in BSS or monotonic switching technique since $V_{\rm cm}$ varies in each comparison cycle and the comparator offset depends strongly on $V_{\rm cm}$ [14], [15].

### D. Switches and Logic

A clock generator similar to that in [4] is used. The input sampling switches $S1$ and $S2$ are bootstrapped with the circuit shown in Fig. 7(a) [19]. A thick-oxide device provided in the process is used to tolerate a potential voltage higher than 1.2 V. The OR gate needs to have a reset function together with controlled delay with the aim to provide enough time for DAC settling. Since the unit capacitor employed in this design is quite small (1.9 fF), the DAC settling time is comparable with the CMOS logic gate delay. To minimize the number of logic gates and their delay, a dynamic OR gate shown in Fig. 7(b) is used instead of the traditional CMOS gates. VB is used to control the current flowing through the OR gate, thus tuning the gate delay.

## IV. Measurement Results

The prototype ADC is fabricated in 40-nm CMOS and occupies an active area of only 0.004 mm$^2$, as shown in Fig. 8. Unlike the floor plan in [12], where the DAC and SAR logic are placed side by side, the SAR logic is placed between two capacitive digital-to-analog converters (CDACs) in our design. By doing this, long routing wires are avoided, which saves both area and power. The outputs are decimated by 32 using five divide-by-two toggle flip-flops to facilitate ADC measurements. All measurements are performed under a 1.2-V power supply.

Fig. 9 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) before and after performing the proposed comparator offset calibration. Before calibration, large DNL and INL jumps happen due to comparator offset mismatches. After performing the $V_{\rm cm}$-adaptive offset calibration, DNL and INL are reduced significantly to $-0.4$ LSB/0.9 LSB and $-0.3$/0.6 LSB, respectively. The effectiveness of the calibration can also be observed from the measured spectrum shown in Fig. 10, where 4.3-dB SNDR and 8.5-dB SFDR improvements are achieved after calibration.

Fig. 11 shows the measured fast Fourier transform (FFT) spectrum with a 700-MS/s sampling rate and a 300-MHz input. The measured SNDR and SFDR are 34.8 dB and 47.8 dB, respectively, leading to a 5.5-b effective number of bits. When the input frequency is reduced to 10 MHz, the measured SNDR and SFDR are 35.1 dB and 49.5 dB, respectively. Fig. 12 shows the SNDR and SFDR at different sampling frequencies with a 50-MHz input, at different input frequencies with a 700-MS/s sampling rate, and at different input amplitudes with a 300-MHz input and a 700-MS/s sampling rate. The measured SNDR is above 34.7 dB across the whole Nyquist band. The maximum sampling rate of 700 MS/s is limited by insufficient

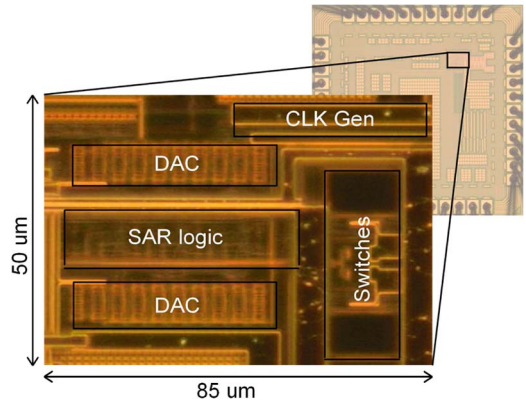


Fig. 8. Chip micrograph.

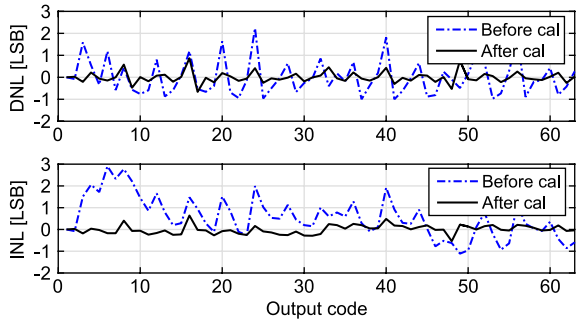


Fig. 9. Measured DNL/INL (dotted line) before calibration and (solid line) after calibration.

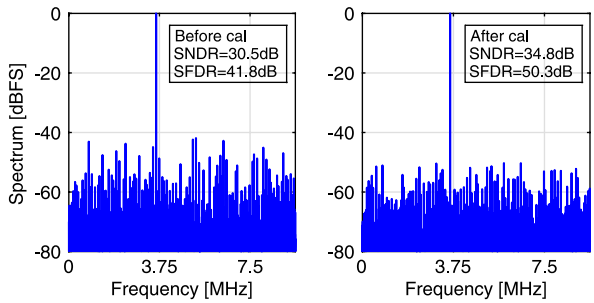


Fig. 10. Measured 1024 p FFT spectrum before calibration and after calibration with 600-MS/s sampling rate and 100-MHz input.

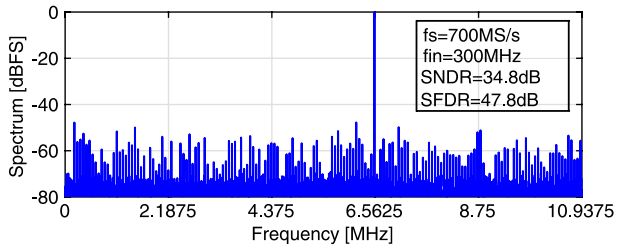


Fig. 11. Measured 1024 p FFT spectrum with 700-MS/s sampling rate and 300-MHz input.

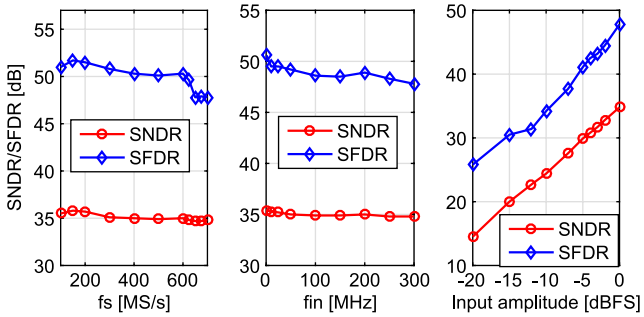


Fig. 12. Measured SNDR/SFDR (left) under different sampling rates with 50-MHz input, (middle) under different input frequencies with 700-MS/s sampling rate, and (right) under different input amplitudes with 700-MS/s sampling rate and 300-MHz input.

TABLE I
PERFORMANCE COMPARISON

| | [4] | [5] | [9] | [12] | **This work** |
|---|---|---|---|---|---|
| Resolution [Bits] | 6 | 6 | 6 | 6 | **6** |
| Process [nm] | 130 | 65 | 40 | 40 | **40** |
| Supply voltage [V] | 1.2 | 1.2 | 1.2 | 1.0 | **1.2** |
| Active area [mm$^2$] | 0.060 | 0.110 | 0.009 | 0.014 | **0.004** |
| Number of TI channels | 2 | 2 | 1 | 1 | **1** |
| Sampling rate [GS/s] | 0.6 | 1 | 1 | 1.25 | **0.7** |
| SNDR (Nyq) [dB] | 32 | 29 | 31.2 | 26.8 | **34.8** |
| ENOB [bit] | 5.0 | 4.5 | 4.9 | 4.1 | **5.5** |
| Power [mW] | 5.3 | 6.7 | 5.3 | 6.08 | **0.95** |
| Walden FoM [fJ/step] | 276 | 290 | 180 | 272 | **30** |
| Schreier FOM [dB] | 142.5 | 140.7 | 144.0 | 139.9 | **153.4** |

sampling time discovered during chip measurements. When clkse goes low, it takes longer time to reset comparators in measurements than that in simulation, which reduces the effective sampling time. The total power consumption at 700 MS/s is 0.95 mW, whose breakdown is as follows: 0.84 mW used by the SAR logic and comparator, 0.09 mW used by DAC, and 0.02 mW used by the clock generator. The measured Walden figure-of-merit (FOM) [20] at the Nyquist rate is 30 fJ/conversion-step, and the Schreier FOM [21] is 153.4 dB. As shown in Table I, this work achieves the highest SNDR and the best FOM with the smallest chip area compared to other state-of-the-art 6-b designs.

## V. CONCLUSION

This brief presented a high-speed and low-power single-channel loop-unrolled SAR ADC. It proposed a simple method to calibrate the comparator offsets. The proposed switching technique allows the designers to control the comparator input common-mode voltage for comparator offset and speed optimization. It can be easily time interleaved (TI) for even higher speed applications.

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