A Novel Hybrid Radix-3/Radix-2 SAR ADC With Fast Convergence and Low Hardware Complexity

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***Abstract*—This brief presents a fast-converging hybrid successive approximation register (SAR) analog-to-digital converter (ADC) based on the radix-3 and radix-2 search approaches. The radix-3 approach achieves 1.6 bits/cycle, and the radix-2 approach mitigates the effect of comparator offset and improves the accuracy of the ADC. Incorporating clock gating of comparators and efficient switching of capacitors, the proposed hybrid ADC demonstrates promising balance between hardware complexity and speed and can achieve equivalent signal-to-noise-and-distortion-ratio (SNDR) with less capacitors compared with radix-3 SAR ADC. Behavioral simulation-based results verify operation and merit of the proposed architecture. An 11-bit 45-MS/s prototype with 5% capacitor mismatch in 180-nm CMOS was simulated in SPICE and achieves 67 dB of SNDR after calibration.**

***Index Terms*—Analog-to-digital converter (ADC), digital-to-analog converter (DAC), successive approximation register (SAR).**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) are popular ADCs because of exploiting the benefits of the ever-shrinking technology nodes and high-switching speed of nanometer CMOS processes [1]. The fundamental factor limiting SAR ADC's speed is the linear relationship between the number of comparison cycle and the resolution. A K-bit conventional SAR ADC takes K comparison cycles for a full conversion. To overcome this issue, multibits/step SAR ADCs have been proposed at the expense of hardware complexity and with limitation of resolution because of comparator offsets [2], [3].

To reduce the hardware complexity, we proposed an efficient implementation of fast radix-3 SAR ADC in [4] and [5], which requires fewer number of capacitors and has lower hardware complexity compared with [2] and [3]. In addition, it provides $\log_2 3 = 1.6$ bits/cycle. The proposed architecture was implemented with two differential DACs and two comparators and consumed less power compared with [2] and [3]. To further reduce power, the radix-3 ADC can be implemented by two single-ended DACs. However, fully differential DACs offer wider dynamic range, better SNDR and higher common mode rejection compared with single-ended DACs. In addition, use of multiple comparators affects the linearity of the ADC if the comparators have different offsets.

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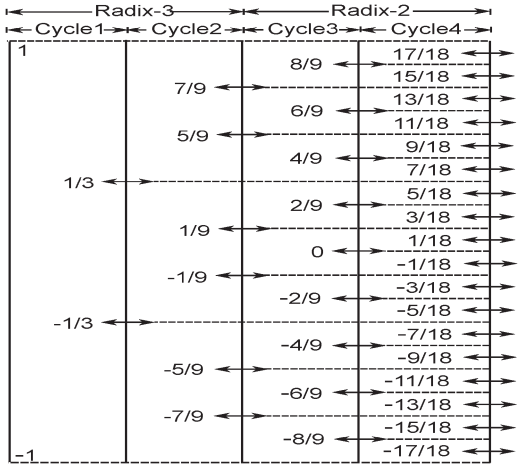

Fig. 1. Reference voltage levels of the proposed hybrid ADC architecture.

In this brief, we propose a novel hybrid SAR ADC that uses a single-ended radix-3 search for the first few bits and a differential radix-2 search for the rest of the least significant bits (LSB). Radix-3 search provides fast convergence rate and requires low-resolution and low-power comparators. Differential radix-2 search mitigates the effect of comparator offset with a comparator of higher resolution and higher power. Using an efficient switching scheme [6] during radix-2 search and clock gating among low- and high-power comparators, the proposed hybrid ADC maintains both accuracy and efficiency in power and speed. ADC linearity highly depends on capacitor matching. In this brief, to reduce capacitor mismatch, a fully digital calibration method has been proposed that does not require any extra capacitor DAC.

This brief is organized as follows. Section II explains the architecture of hybrid SAR ADC. Section III theoretically compares the speed, power, and performance of the ADC with radix-3 and radix-2 ADCs. Section IV presents the calibration of the ADC. Circuit implementation details and SPICE simulation results are presented in Section V. Conclusion is drawn in Section VI.

II. Proposed Hybrid SAR ADC

An in-depth review of comparison levels is very imperative to understand the architecture of any ADC. For that purpose, Fig. 1 presents the comparison levels of the proposed hybrid SAR ADC containing 2 ternary and 2 binary bits. Assuming input voltage $V_{in} \in [-1, 1]$, in the first cycle, it is compared

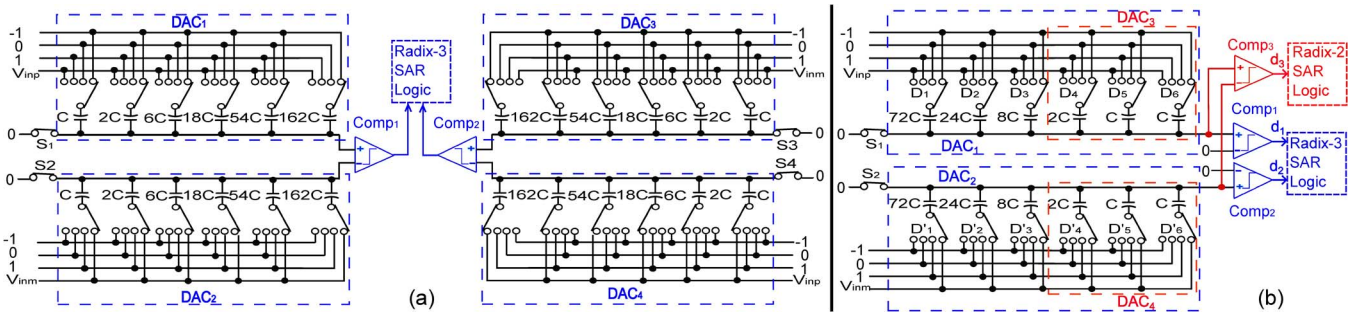

Fig. 2. (a) Conventional radix-3 SAR ADC. (b) Proposed radix-3/radix-2-based hybrid SAR ADC.

against 1/3 and $-1/3$ and one ternary bit is resolved in cycle1. In cycle2, comparison levels can be $(-7/9, -5/9)$ or $(-1/9, 1/9)$ or $(5/9, 7/9)$ and another ternary bit will be resolved. In cycle3 and cycle4, two binary bits are resolved. Hence, total $(2 \times 1.6 + 2 \times 1) = 5.2$ binary bits are achieved from 4 cycles.

A conventional 5-ternary bit radix-3 ADC circuit implementation is shown in Fig. 2(a). In this ADC, two comparators $\text{Comp}_{1,2}$ and four capacitor DACs, $\text{DAC}_{1,2,3,4}$ are used to perform the differential ternary search. Hence, a total of 5 cycles are required to produce 8 binary bits. Fig. 2(b) shows the proposed hybrid SAR ADC containing 3 ternary bits and 3 binary bits with $\sim$78% less capacitance of radix-3 SAR ADC. In the proposed ADC, two comparators $\text{Comp}_{1,2}$ and two capacitor DACs, $\text{DAC}_{1,2}$, are used to perform the single-ended ternary search, and $\text{DAC}_{3,4}$ act as a single LSB capacitor for $\text{DAC}_{1,2}$ and produce 4.8 binary bits in 3 comparison cycles. In addition, $\text{DAC}_{3,4}$ and Comp_3 are used to perform differential radix-2 search. Hence, a total of 6 cycles are required to achieve 7.8 binary bits. To illustrate the circuit level operation, it is assumed that an input voltage "55/108" is sampled across the DACs. In the first comparison cycle, i.e., ϕ_1, capacitor 72C of $\text{DAC}_{1,2}$ are connected to 0 and the rest of the capacitors are connected to 1, which generate two reference levels "1/3" and "$-$(1/3)." Comparators' outputs (d_1, d_2) become $(-1, -1)$ and a simple logic circuit converts that to single control inputs D_1 and D'_1 for MSB capacitors of DAC_1 and DAC_2, respectively. Thus, the first 1.6 bits are obtained in cycle ϕ_1. Similarly, with radix-3 search, 3.2 binary bits are obtained in $\phi_2 - \phi_3$. In $\phi_4 - \phi_6$ radix-2 search is completed using the switching scheme of [6] and 3 binary bits are obtained. The detailed conversion steps, including the comparison levels, are illustrated in Fig. 3. Fig. 4 explains the residual voltages of the proposed ADC.

Fig. 2(b) can be expanded for a $(N + M)$-bit hybrid SAR ADC containing N ternary bits and M binary bits. Defining C_u as the sum of all capacitors of $\text{DAC}_{3,4}$ and also as the unit capacitor of $\text{DAC}_{1,2}$ and C_i as the value of ith individual capacitor of DACs, we have

$$C_u = \sum_{l=1}^{M} C_l \tag{1}$$

$$C_i = \begin{cases} 2 \cdot 3^{i-M-1} C_u & \text{if } M+1 \le i \le N+M \\ \frac{2^{i-2}}{2^{M-1}} C_u & \text{if } 1 < i \le M \\ \frac{1}{2^{M-1}} C_u & \text{if } i = 1. \end{cases} \tag{2}$$

Fig. 5 shows the flow diagram of conversion steps of $(N + M)$-bit hybrid SAR ADC.

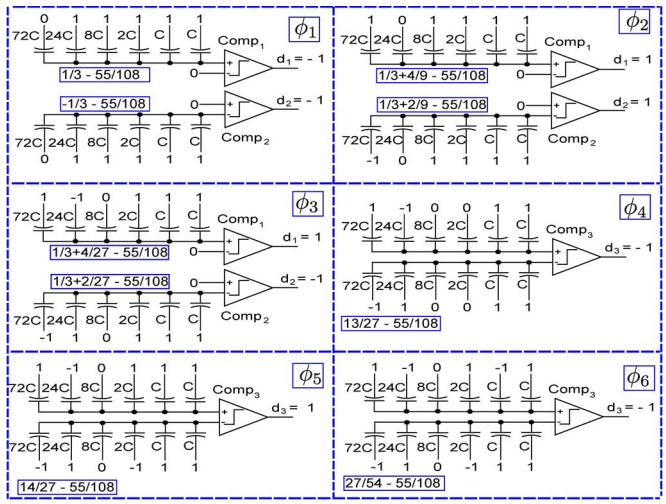

Fig. 3. Proposed hybrid ADC's conversion steps for input voltage of "55/108."

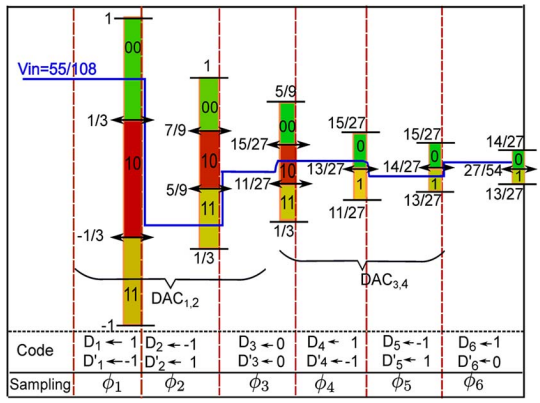

Fig. 4. Sampling and comparison phases for (3+3)-bit hybrid SAR ADC.

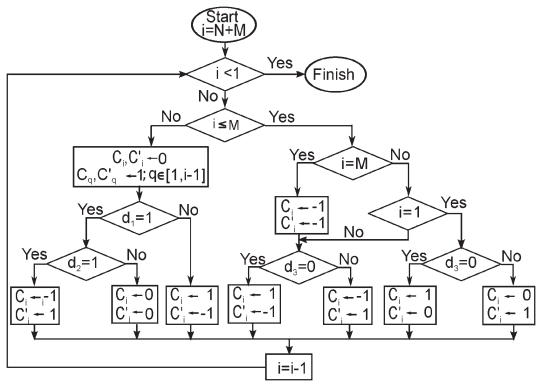

Fig. 5. Conversion flow diagram of the propsed hybrid SAR ADC.

TABLE I
COMPARISON OF HARDWARE COMPLEXITY OF MULTIBITS/STEP ADCS

ADC	SAR Arch	Average comparator/cycle	No. of DAC Array	Total unit capacitors	Control (Switches)	Mux/extra logic	Calibration	Conversion Cycles	Off Chip Sequencer
[2]	2b/cycle	3	6	378	42	Yes	Yes	3	No
[3]	1.6b/cycle	2	4	324	324	No	Yes	4	No
[4], [5]	1.6b/cycle	2	4	324	72	No	Yes	4	No
Proposed	hybrid	1.5	2	54	38	No	Yes	4	No

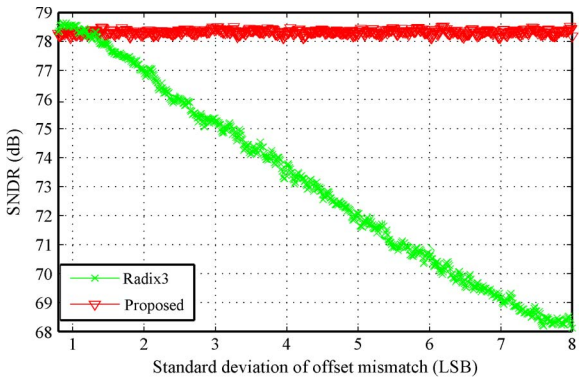

Fig. 6. Monte Carlo simulation to compare the effect of comparator offset.

Design complexity of hybrid SAR ADC, including three ternary bits and one binary bit, was estimated and compared with other multibits/cycle SAR ADCs with close to 6-binary bits resolution in Table I. It can be shown from Table I that, because of the architecture, the proposed ADC requires the lowest number of DAC arrays and capacitors than other ADCs. In addition, the switching between low- and high-power comparators in the proposed hybrid ADC helps to achieve less comparator power than [2, 3, 4, 5]. Thus, hybrid ADC benefits from a high convergence rate with simpler circuitry compared with other ADCs.

III. HYBRID ADC CHARACTERIZATION

A. Effect of Comparator Offset

The LSB of a hybrid SAR ADC with N ternary bits and M binary bits is $2V_{\rm ref}/2^{(1.6N+M)}$. During radix-3 search, comparator offset should be less than $V_{\rm ref}/2^{1.6N}$, which is $2^{(M-1)}$ times larger than the overall LSB and though two comparators are used simultaneously, the offset mismatch between the comparators should not affect the linearity as long as it does not cross the over range limit set by redundancy capacitor [7], which is 9 LSB in our design. During radix-2 search of hybrid ADC, a single comparator is used and its offset should not affect overall linearity. In radix-3 SAR ADC, linearity is affected by comparator offset mismatch as two comparators are used simultaneously during all the conversion steps. The variation of comparator offset is modeled by the Gaussian random variable with standard deviation. In Fig. 6, SNDR was plotted based on the result of 10,000-sample Monte Carlo simulations for (5+5)-bit hybrid ADC with redundancy. As explained earlier, hybrid SAR ADC shows consistent SNDR over the whole range of variation, whereas radix-3 ADC's linearity degrades significantly. Similarly, input common mode voltage variation of two different single-ended DACs is equivalent to comparator offset mismatch, and it will not affect the hybrid ADC's performance as long as the variation is within the over range limit.

TABLE II
SPEED GAIN OF HYBRID ADC OVER RADIX-2 AND RADIX-3 SAR ADCS

Resolution	$(T_{conv}$-$T_{hyb})/T_{conv}$ (%)			$(T_{hyb}$-$T_{rd3})/T_{rd3}$ (%)		
K (bits)	M=2	M=3	M=4	M=2	M=3	M=4
6	16.7	33	16.7	0	−25	−25
7	28.6	22	14.3	−20	−20	−20
8	25	37.5	12.5	−20	−20	−20
9	22.2	22.2	22.2	−16.2	−16.2	−16.2
10	30	30	20	0	0	−16
11	27.3	27.3	27.3	−14.3	−14	−14
12	33.3	25	25	−12.5	−25	−25

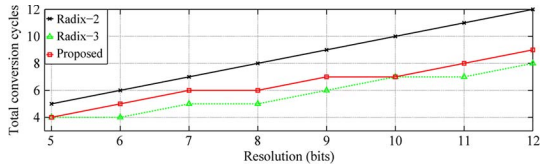

Fig. 7. Comparison of total conversion cycles.

B. Comparison of Speed

The proposed ADC exploits the conversion speed of radix-3 search and converges faster than radix-2 SAR ADC. To achieve in total an equivalent K binary bits of resolution, a hybrid ADC with M binary bits takes $(M + ((K - M)/1.6))$ cycles, and a radix-3 ADC requires $K/1.6$ cycles. Depending on the value of M, Table II shows the comparison between number of conversion cycles of hybrid ADC, $\rm T_{hyb}$ and that of radix-2 ADC, $\rm T_{\mathit{conv}}$ and that of radix-3 ADC, $\rm T_{\mathit{rd3}}$. Depending on the configuration, the proposed ADC can achieve a maximum speed gain of 37.5% over radix-2 ADC but can have a worst case speed loss of 25% compared with radix-3 ADC. Fig. 7 shows the comparison of total comparison cycles among radix-2, radix-3, and hybrid SAR ADC with $M = 3$. It follows the result in Table II.

C. Comparison of Power

One of the major contributors to power consumption in ADC is the capacitor DAC. To achieve a K binary bit, the conventional radix-2 ADC requires a total of 2×2^K unit capacitors. For the same binary resolution, radix-3 ADC requires $K/1.6$ ternary bits and a total of $4 \times 3^{K/1.6}$ unit capacitors. Assuming hybrid ADC contains equal ternary and binary bits, and it will require a total of $2 \times (2^{(K/2.6)-1}3^{K/2.6})$ unit capacitors. Thus, to have the same number of resolution, the proposed hybrid SAR ADC requires fewer capacitors than others.

During radix-3 conversion, the DAC capacitors are first connected to V_{cm}. If input voltage is within [−1/3, 1/3], then the MSB capacitors do not switch and thus, the DAC switching energy is zero. In addition, during radix-2 search, the proposed switching scheme ensures much less switching energy in the first two conversion cycles by adopting the technique of [6] and only one capacitor is switched in each comparison cycle, which also reduces the energy. Thus, hybrid SAR ADC gets benefited from the radix-3 and radix-2 switching approaches and also from its fewer number of capacitors. Fig. 8 shows the comparison of DAC reference energy for different techniques

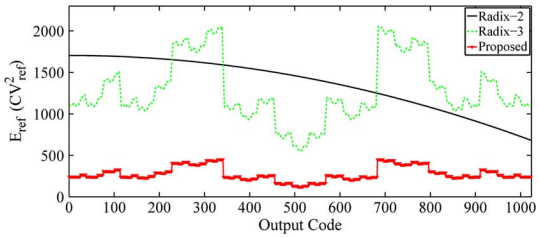

Fig. 8. Comparison of DAC switching energy.

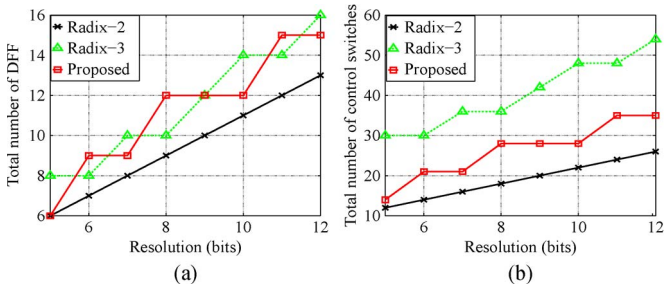

Fig. 9. Comparison of (a) the required DFFs and (b) the total number of control switches.

for a 10-bit SAR ADC. As can be seen, the proposed scheme has a significantly lower E_{ref} than the conventional radix-2 and radix-3 ADCs.

As discussed earlier, a redundant capacitor is added in the proposed ADC so that it can tolerate errors due to both comparator offset mismatch and noise. Thus, during radix-3 search, we can use low-power high-noise and large-offset comparators for $\text{Comp}_{1,2}$. During radix-2 search, the low-power comparators are switched off and we use a high-power but low noise comparator for Comp_3. This way, we can reduce the total comparator power. The total comparator power would be comparable to that for the radix-2 search when similar comparator power saving technique is adopted [8]. In contrast, conventional radix-3 ADC has to use two high-power low-offset comparators during all the cycles for accuracy purpose, and the total comparator power becomes higher than radix-2 and the proposed hybrid ADC.

The SAR logic power depends on the complexity of the switching logic, the number of DFFs for data storage, and the number of DAC switches. As discussed before and shown in Fig. 5, the switching logic for the proposed hybrid SAR ADC is simple and easy to implement. For K binary bit resolution, radix-2 ADC requires $(K+1)$ DFFs to latch the data for the capacitor DAC, where radix-3 ADC requires $((2K/1.6)+1)$ DFFs and hybrid ADC requires $((2K/2.6)+(K/1.6))$ DFFs. The required numbers of DAC control switches are $(2K+2)$, $6(K+1)/1.6$ and $((6K/2.6)+(2K/2.6))$, for conventional radix-2, radix-3, and the hybrid ADC, respectively. The comparisons of the total number of DFFs and switches are shown in Fig. 9. Overall, the SAR logic power for the proposed hybrid ADC is comparable to that for radix-2 and radix-3 ADCs with small differences among them.

Considering the aforementioned facts, hybrid ADC requires lower DAC power, comparable comparator power, and slightly more power in SAR logic circuits than radix-2 ADC. It offers lower power than radix-3 ADC, as previously discussed. Considering the speed gain over radix-2 ADC and accuracy gain over radix-3 ADC, the proposed hybrid ADC proves itself to be a good alternative way for high-speed data conversion.

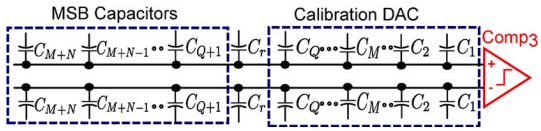

Fig. 10. Simplified DAC of hybrid SAR ADC.

IV. Capacitor Mismatch Calibration

Fig. 10 is a simplified version of $(N+M)$-bit hybrid SAR ADC. A redundant capacitor C_r is required for calibration purposes. Due to process variation, it has been assumed that each capacitor is varied by a proportion of ϵ [9]. If the number of LSB capacitors used for calibration is Q, then C_r can be defined in terms of unit capacitor of $\text{DAC}_{1,2}$, C_u as

$$C_r = 3^{Q-M-1}C_u(1+\epsilon_r). \tag{3}$$

Defining $A = 3^{Q-M-1}2^{M-1}$, $X = 2^M\sum_{i=M+1}^{M+N}3^{i-M-1}$, $Y = \sum_{i=1}^{M}2^{i-1}$, from (1), C_u can be redefined as

$$C_u = \frac{C_u\left((X+Y)(1+\epsilon_i)+(1+\epsilon_1)+A(1+\epsilon_r)\right)}{2^{M-1}(3^N+3^{Q-M-1})}. \tag{4}$$

From (4), it can be shown that

$$(X+Y)\epsilon_i+\epsilon_1+A\epsilon_r = 0. \tag{5}$$

The output voltage V_o can be found in terms of digital output coded D_i, $i\in[1,M+N]$ and digital code D_r for C_r

$$V_o = \frac{\sum_{i=1}^{N+M}C_iD_i+C_rD_r}{C_{\text{total}}} \tag{6}$$

$$V_o = \frac{(X+Y)(1+\epsilon_i)D_i+A(1+\epsilon_r)D_r+(1+\epsilon_1)D_1}{2^{M-1}(3^N+3^{Q-M})}. \tag{7}$$

If there is no mismatch, i.e., $\epsilon_i=\epsilon_r=0$, then ideal output

$$V_{\text{ideal}} = \frac{(X+Y)D_i+AD_r+D_1}{2^{M-1}(3^N+3^{Q-M})}. \tag{8}$$

Defining error voltage for nth capacitor as $V_{\epsilon n}$

$$V_{\epsilon n} = \begin{cases} \frac{2\cdot3^{i-M-1}\epsilon_n}{(3^N+3^{Q-M-1})} & \text{if } M+1\le n\le N+M \\ \frac{2^{i-M}\epsilon_n}{(3^N+3^{Q-M-1})} & \text{if } 1<n\le M \\ \frac{2^{1-M}\epsilon_n}{(3^N+3^{Q-M-1})} & \text{if } n=1 \\ \frac{3^{Q-M-1}\epsilon_n}{(3^N+3^{Q-M-1})} & \text{if } n=r. \end{cases} \tag{9}$$

Defining total error voltage as V_{error}

$$V_{\text{error}} = V_o - V_{\text{ideal}} = \sum_{i=1}^{N+M}V_{\epsilon i}D_i + V_{\epsilon r}D_r. \tag{10}$$

In the current ADC architecture, LSB capacitors C_i, $i\in[1,Q]$ do not require calibration as their mismatch error is negligible [9]. Thus, calibration is performed only on MSB capacitors C_i, $i\in[Q+1,M+N]$. Calibration is started by sampling "1" across C_{M+N} and "0" across the rest of the capacitors. Then, "1" is sampled on the bottom plate of all the capacitors except C_{M+N} and C_i, $i\in[1,Q]$, which will be connected to "-1." Thus, the residual charge at the top plate of the capacitors

$$Chg_{M+N} = 2\cdot C_u\left(3^{N-1}\epsilon_N - \sum_{i=Q+1}^{N+M-1}3^{i-M-1}\epsilon_i - A\epsilon_r\right). \tag{11}$$

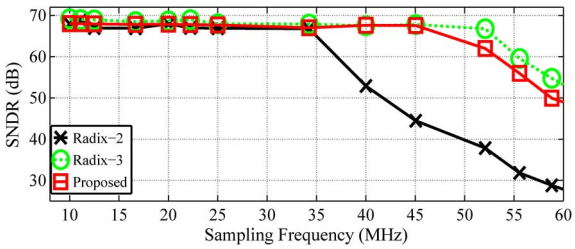

Fig. 11. Comparison of maximum speed.

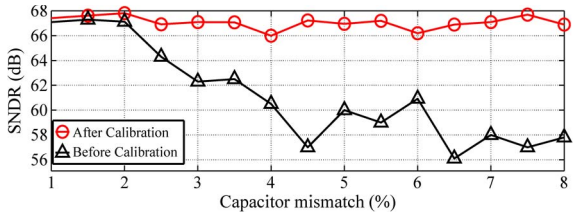

Fig. 12. SNDR of the proposed ADC before and after calibration.

From (9) and (11), residual voltage

$$V_{xM+N} = \frac{Chg_{M+N}}{C_{\text{total}}} = \frac{3}{2} V_{\epsilon_{M+N}}. \tag{12}$$

Similarly, error voltage $V_{\epsilon n}$, $n \in [Q+1, N+M-1]$ is

$$V_{\epsilon n} = \frac{2}{3}\left(V_{xn} - \sum_{i=n+1}^{M+N} V_{\epsilon i}\right). \tag{13}$$

After quantizing the error, digitized error voltages $DV_{\epsilon q}$ and quantized residue voltage, DV_{xq} are

$$DV_{\epsilon q} = \begin{cases} \frac{2}{3} DV_{xq} & \text{if } q = N+M \\ \frac{2}{3}\left(DV_{xq} - \sum_{i=Q+1}^{N+M} DV_{\epsilon i}\right) & \text{if } N+M > q \geq Q+1. \end{cases} \tag{14}$$

If ith bit is assigned as 1, 0, or -1, then corresponding error voltage $DV_{\epsilon i}$ will be $DV_{\epsilon i}$, $(1/2)DV_{\epsilon i}$ or 0, respectively. C_i, $i \in [1, Q]$ can be used for digitizing error terms. During normal conversion cycles, the calibration logic is deactivated and the converter works in the same way as the proposed hybrid SAR ADC. Finally, the error correction voltages are added based on the DAC digital output codes of the first $N+M-Q$ capacitors.

V. Simulation Results

A prototype (5+3)-bit hybrid ADC, a 7-bit radix-3 and an 11-bit radix-2 ADC were designed in a 180-nm CMOS process with $2fF$ minimum capacitor value, 1.8 V supply and simulated in SPICE with an input sine wave of amplitude of 1.7 V and with varying sampling frequency. The SNDR values are plotted in Fig. 11. It can be seen that, to achieve the desired SNDR, radix-2 ADC can operate at a maximum speed of 34 MHz, where hybrid and radix-3 ADC can operate at 45 and 52 MHz, respectively. The simulation result closely follows the data of Table II.

To verify calibration, capacitor ratio error was varied using Monte Carlo simulation from 0.5% to 8%, and SNDR was plotted in Fig. 12 based on SPICE simulation. After calibration, SNDR is maintained above 67 dB, which proves the efficiency of the proposed calibration technique. INL and DNL are plotted with 5% capacitance mismatch in Fig. 13. Before and after calibration DNL was $+1.4/-.65$ LSB and $+0.25/-.08$ LSB, respectively, and INL was $+1.64/-1.66$ LSB and $+0.3/-.298$ LSB, respectively. The 1024-point DFT plot of the hybrid ADC simulating with sampling frequency 45 MHz and with 5% mismatch is shown in Fig. 14. The SNDR is 53 dB before calibration and 67 dB after calibration, which verifies the proposed calibration idea.

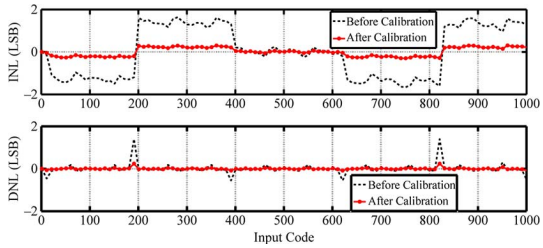

Fig. 13. INL and DNL of the proposed ADC with 5% mismatch.

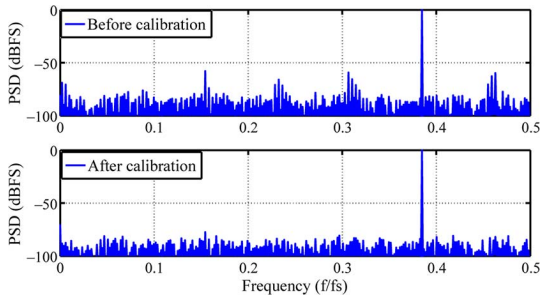

Fig. 14. The 1024-point DFT plot to compare SNDR before and after calibration.

VI. Conclusion

In this brief, a novel hybrid SAR ADC and its characteristics have been proposed. It offers a fast conversion technique with less hardware complexity. A digital calibration method was also introduced. Theoretical analysis and circuit-based simulation also verified the proposed idea.

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