Digital Background Calibration for Pipelined ADCs Based on Comparator Decision Time Quantization

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***Abstract*—This brief presents a digital background calibration technique that embraces comparator decision time to calibrate interstage gain errors and capacitor mismatches in pipelined analog-to-digital converters (ADCs). It does not modify the original analog signal path except for the addition of a comparator decision time binary quantizer built by simple digital gates. The technique does not limit either the ADC input signal swing or bandwidth. Simulation results for a 12-bit pipelined ADC show that the proposed technique can improve the signal-to-noise-and-distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) from 44 and 48 dB to 72 and 86 dB, respectively. The SNDR convergence time is less than 3×10^6 cycles.**

***Index Terms*—Comparator decision time, digital background calibration, pipelined analog-to-digital converters (ADCs).**

I. Introduction

CONVENTIONAL pipelined analog-to-digital converters (ADCs) rely on the use of a high-gain operational transconductance amplifier (OTA) to ensure an accurate interstage gain. Over the past decade, researchers have proposed to use low-gain amplifiers to reduce power [1]–[6]. The problem for this approach is that the interstage gain is inaccurate and depends on ambient environment, such as temperature, which introduces conversion errors. To address this issue, various digital background calibration techniques have been developed. Most of them require major modifications to the original analog signal path, such as adding dithers to the input [1] or arranging two operational modes [2]. Several other techniques aim to minimize analog complexity. For example, the skip-and-refill approach of [3] does not modify the analog signal path; however, it undesirably limits the input signal bandwidth. The technique of [4] also does not modify the analog signal path, but its parameter estimation is very sensitive to noise and variations in input distribution. The technique of [5] has low complexity. It only requires dithering comparator threshold voltages. Nevertheless, its convergence time is very long. To accelerate convergence, it splits the ADC into two channels, which increases design efforts. Recently, we have proposed a low-complexity background calibration technique [6]. It only requires an identical copy of comparators and has much faster convergence. It is suitable for pipeline stages with a small number of comparators. However, for architectures with a large number of bits per stage, the number of extra comparators can be large, such as 31 for a 5-bit stage, which increases power and area. Another limitation of [6] is that its convergence time is proportional to comparator offset, which could be large if small dynamic comparators are used.

In this brief, we report a new digital background calibration technique that builds upon the key idea in [6] but does not require doubling the number of comparators. The only modification to the analog path is the addition of decision time binary quantizers (DTQs) built by simple digital gates. Compared to a similar independently developed technique [7], this brief proposes an improved replica-based DTQ that is insensitive to process, voltage, and temperature (PVT) variations. The technique can correct ADC conversion errors due to insufficient amplifier gain and capacitor mismatch and achieves short convergence time that does not depend on the comparator offset. It can be easily adapted to calibrate cyclic ADCs and capacitor mismatch in successive approximation register ADCs [8].

This short brief is organized as follows. Section II presents the calibration technique and convergence time analysis. Section III shows simulation results. Section IV draws the conclusion.

II. Proposed Calibration Technique

This section explains the proposed calibration technique using a 1.5-bit stage as an example. It can be easily generalized to other multibit-per-stage cases.

A. Basic Idea

For simplicity of presentation, let us make the following assumptions.

1) Only the first stage is nonideal with a low-gain ($G \neq \infty$) amplifier and capacitor mismatch ($\Delta \equiv C_1/C_2 - 1 \neq 0$) [see Fig. 1]. Although the following analysis assumes that the amplifier is configured in a closed loop, the calibration technique also works for an open-loop amplifier.
2) The signal range of the input $V_{\rm in}$ is $[-1, 1]$.
3) The reference voltages are ± 1 V.

In the sampling phase [see Fig. 1(a)], two comparators are arranged to compare $V_{\rm in}$ with $\pm 1/4$. The only modification is that each comparator is equipped with a DTQ, which is shown in Fig. 2 [9]. A replica-based delay block, whose implementation details are discussed in Section II-C, replaces the tunable delay buffer in [9]. An active low comparator "Ready" signal is generated by the XNOR gate. The XNOR output is initially high in the reset phase and goes low once the comparator decision is ready. The ready signal is latched using a clock that is delayed relative to the comparator clock by time

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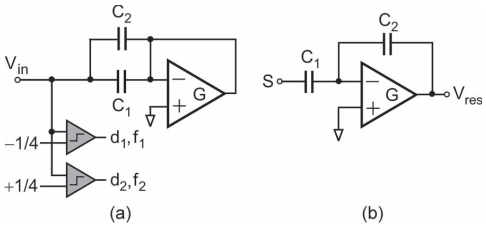

Fig. 1. 1.5-bit case. (a) Sampling phase. (b) Charge transfer phase.

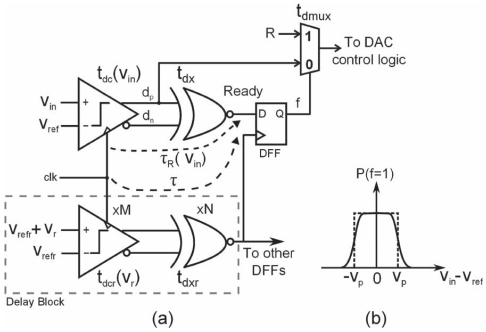

Fig. 2. (a) Schematic of a comparator with DTQ. Subscripted variable beside each block represents its propagation delay. (b) Probability distribution of flag generation: (dashed) ideal; (solid) with noise.

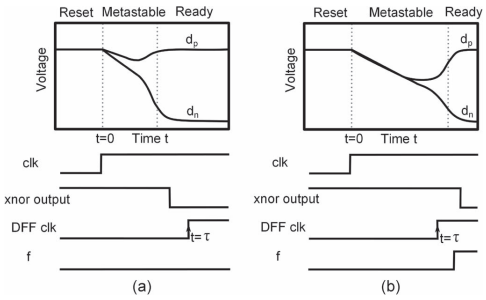

Fig. 3. Comparator and decision time quantizer waveforms for (a) large input and (b) small input.

τ to generate the flag signal f. Comparator outputs are initially high in the reset phase, as shown in Fig. 3. Once triggered, both comparator outputs start to decrease with their difference increasing at a rate that is proportional to the comparator input. For large inputs, comparator outputs regenerate in a short time and $f = 0$, as shown in Fig. 3(a). By contrast, for inputs that are very close to the comparator threshold, the comparator decision is not ready at $t = \tau$. Assuming that both outputs are still resolved by the XNOR gate as logic high and ignoring D flip-flop (DFF) setup time for now, then $f = 1$, indicating that comparator input is in proximity of its threshold, as shown in Fig. 3(b). In effect, the DTQ acts as an analog window detector detecting comparator inputs within V_p from its threshold. We refer to these as proximity inputs. For inputs where "Ready" is close to the DFF master latch threshold at $t = \tau$, the final value of f is stochastic and determined by the master latch noise and clock jitter. This smoothes the detection window edges, as shown in Fig. 2(b). Comparator noise has a similar effect [10]. It will be shown in the next section that noise sets a lower limit on the detection window width $2V_p$.

In a conventional pipeline ADC and for a given bit error rate (BER), comparators are allocated sufficient regeneration time $t_{\rm regen}$ to ensure a low metastability probability. For our proposed architecture, it can be shown that metastability errors occur due to f DFF metastability. The error mechanisms are similar to those of a conventional pipeline ADC [11]. Assuming that DFF and comparator latches have the same regeneration time constant, the total time allocated for comparator evaluation phase increases to $t_{\rm regen} + \tau + t_{\rm dmux}$, where $t_{\rm dmux}$ is the multiplexer propagation delay, in order to keep a similar BER. This leads to a small speed penalty. For instance, in 180-nm CMOS, $\tau + t_{\rm dmux}$ is about 500 ps for $V_p = 3$ mV. For a 100-MS/s ADC, this corresponds to a speed reduction of only 5%.

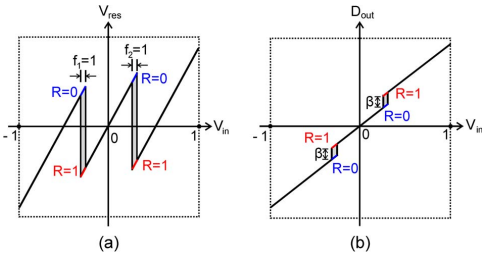

Fig. 4. 1.5-bit case. (a) Residue curve. (b) Transfer curve.

In the subsequent charge transfer phase [see Fig. 1(b)], both f_1 and f_2 are exploited in choosing the reference voltage S.

1) If no proximity inputs are detected ($f_1 = f_2 = 0$), S is the same as that in the standard 1.5-bit stage: $S = -1$ for $d \equiv d_1 + d_2 = 0$; $S = 0$ for $d = 1$; and $S = 1$ for $d = 2$.
2) If proximity inputs are detected (either $f_1 = 1$ or $f_2 = 1$), a pseudorandom number R (1 or 0) is used to select S: if $f_1 = 1$, $S = 0$ for $R = 1$, and $S = -1$ for $R = 0$; if $f_2 = 1$, $S = 1$ for $R = 1$, and $S = 0$ for $R = 0$.

Mathematically speaking

$$S = (1 - f_1 - f_2)(d - 1) + Rf_2 - (1 - R)f_1. \quad (1)$$

The residue voltage $V_{\rm res}$ is related to $V_{\rm in}$ through

$$V_{\rm res} = 2\alpha V_{\rm in} - S(1 - 2\beta) \quad (2)$$

where α and β are given by

$$\alpha \equiv 1 + \Delta/2 - (2 + \delta)/G \quad (3)$$

$$\beta \equiv -\Delta/2 + (2 + \delta)/(2G) \quad (4)$$

where $\delta \equiv C_{\rm in}/C_1$ ($C_{\rm in}$ is the input capacitance of the amplifier). For simplicity, only first-order terms in (3) and (4) are shown. $V_{\rm res}$ versus $V_{\rm in}$ is depicted in Fig. 4(a). When $f_1 = f_2 = 0$, the residue curves for both $R = 1$ and $R = 0$ are the same and identical to the standard 1.5-bit stage; when $f_1 = 1$ or $f_2 = 1$, the residue curves for $R = 1$ are below those for $R = 0$. Now let us relate $V_{\rm in}$ to the digital output $D_{\rm out}$. $D_{\rm out}$ is a combination of S and the digital representation of $V_{\rm res}$, which is denoted by $D(V_{\rm res})$, and is given by

$$D_{\rm out} = \frac{[D(V_{\rm res}) + S]}{2} \quad (5)$$

where $D(V_{\rm res})$ is the digital output of the backend pipelined ADC consisting of the second through the last stages, whose analog input is $V_{\rm res}$. Since these stages are assumed to be ideal,

$D(V_{\rm res})$ is equal to $V_{\rm res}$. Using this relation and plugging (2) into (5), $D_{\rm out}$ can now be expressed as

$$D_{\rm out} = \alpha V_{\rm in} + S \cdot \beta. \tag{6}$$

$D_{\rm out}$ versus $V_{\rm in}$ of (6) is visualized in Fig. 4(b). The discontinuities at the first-stage bit decision boundaries cause conversion errors and nonlinearities. If the gap length β is extracted, the errors can be removed by

$$D'_{\rm out} = D_{\rm out} - S \cdot \beta = \alpha V_{\rm in}. \tag{7}$$

$D'_{\rm out}$ is the **calibrated** digital output, which is linearly proportional to $V_{\rm in}$. Thus, nonlinear errors caused by gain insufficiency and capacitor mismatches are removed. The key to the calibration is the knowledge of β, which can be obtained by extracting the missing code lengths at $V_{\rm in} = \pm 1/4$, as shown in Fig. 4(b). It is easy to show that

$$\beta = D_{\rm out}|_{V_{\rm in}=-1/4,R=1} - D_{\rm out}|_{V_{\rm in}=-1/4,R=0} \tag{8}$$

$$= D_{\rm out}|_{V_{\rm in}=+1/4,R=1} - D_{\rm out}|_{V_{\rm in}=+1/4,R=0} \tag{9}$$

where "|" means "conditioning on." Equations (8) and (9) represent a foreground way of measuring β, but they cannot be used in the background because $V_{\rm in}$ cannot be intentionally set at $-1/4$ or $+1/4$. To estimate β in the background, f_1 and f_2 are exploited to identify those $V_{\rm in}$'s that are at the vicinity of $\pm 1/4$. More specifically, two estimators $\hat{\beta}_1$ and $\hat{\beta}_2$ can be formed by

$$\hat{\beta}_1 = D_{\rm out}|_{f_1=1,R=1} - D_{\rm out}|_{f_1=1,R=0} \tag{10}$$

$$\hat{\beta}_2 = D_{\rm out}|_{f_2=1,R=1} - D_{\rm out}|_{f_2=1,R=0}. \tag{11}$$

It is easy to show that both $\hat{\beta}_1$ and $\hat{\beta}_2$ are close estimates for β with only small errors due to the variations of $V_{\rm in}$ inside the detection window. As a result, a least-mean-square (LMS) adaptive filter can be designed to estimate β in the background using $\hat{\beta}_1$ and $\hat{\beta}_2$, i.e.,

$$\hat{\beta}[n] = \hat{\beta}[n-1] + \mu \left(\hat{\beta}_1 f_1[n] + \hat{\beta}_2 f_2[n] \right) \tag{12}$$

where μ is the step size of the LMS filter. It is easy to prove that $\hat{\beta}$ converges to β after the LMS loop is closed by replacing $D_{\rm out}$ in (10) and (11) by $D'_{\rm out}$ of (7). Fig. 5(a) shows the architecture of the proposed calibration technique. The operation of the first stage is controlled by R from a pseudorandom number generator (PRNG). The correction block performs the operation of (7) to remove errors from $D_{\rm out}$ to yield $D'_{\rm out}$, which is sent, together with f_1, f_2, and R, to the LMS adaptive filter to update $\hat{\beta}$. Fig. 5(b) shows the detailed block diagram of the LMS adaptive filter that implements (12). It is composed of two channels. Within each channel, a demultiplexer controlled by R separates $D'_{\rm out}$ into two categories ($R = 1$ and $R = 0$), and an adder takes the difference between the two categories to obtain $\hat{\beta}_1$ or $\hat{\beta}_2$. Whenever a new $\hat{\beta}_1$ or $\hat{\beta}_2$ is generated, it is directly used to update $\hat{\beta}$. Note that the two channels are enabled only when proximity inputs are detected ($f_1 = 1$ or $f_2 = 1$). Otherwise, $D_{\rm out}$'s are identical for both $R = 1$ and $R = 0$ [see Fig. 4(b)] and, thus, do not contribute to the extraction of $\hat{\beta}_1$ and $\hat{\beta}_2$ and the update of $\hat{\beta}$. Last but not least, to accelerate

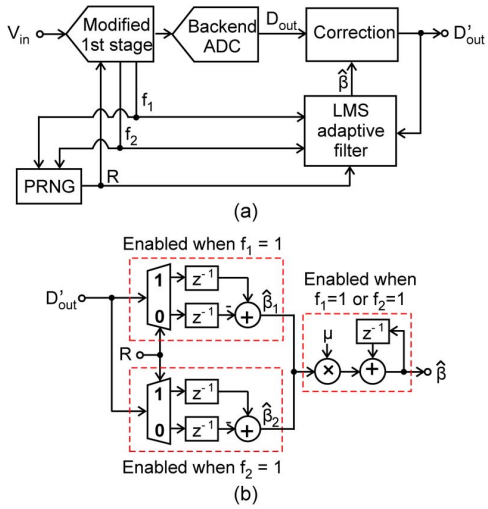

Fig. 5. (a) Main calibration architecture. (b) Detailed block diagram of the LMS adaptive filter.

the convergence of the LMS loop, adjacent R values when $f_1 = 1$ and $f_2 = 1$ should be paired in such a way that each pair contains a "1" and a "0"; in other words, the R sequence should be composed of random pairs of (0,1) or (1,0). The reason is that each update of $\hat{\beta}$ requires a complementary pair of "1" and "0" [see Fig. 5(b)]. Therefore, using random pairs accelerates $\hat{\beta}$ update compared to a pseudorandom number. Additionally, this minimizes interaction between the different LMS loops, as using random pairs minimizes the time span between the complementary samples used to update $\hat{\beta}$, and hence minimizes errors introduced by other LMS loops updates. To this end, f_1 and f_2 need to be fed back to the PRNG [see Fig. 5(a)]. Note that this requirement does not necessarily make R to be correlated with $V_{\rm in}$. For instance, a simple scheme based on Manchester coding can produce a random but paired R [6].

So far, we have assumed that amplifier gain G is a constant. In reality, G may be signal dependent, which introduces distortion. To address this issue, the proposed technique can be modified by placing comparator thresholds at asymmetric locations, e.g., $-1/8$ and $+1/4$ [6]. This way, the third-order amplifier gain nonlinearity can also be extracted and compensated.

B. Convergence Time Analysis

This section performs a first-order analysis on the dependence of the convergence time T on comparator offset, input referred noise, and timing jitter. This analysis ignores different LMS loop interactions assuming a Manchester coding scheme is used as explained in the previous section. As discussed in Section II-A, $\hat{\beta}$ is updated only when $f_1 = 1$ or $f_2 = 1$, and thus, T is inversely proportional to $\mathrm{P}(f_1 = 1)$ and $\mathrm{P}(f_2 = 1)$. T is also inversely proportional to μ, but we cannot arbitrarily enlarge μ for it sets $\mathrm{Var}\{\hat{\beta}\}$, which determines the ADC signal-to-noise-and-distortion ratio (SNDR) after calibration. It is easy to derive from (10) and (11) that μ is inversely proportional to $\mathrm{Var}(D_{\rm out}|_{f_1=1})$ and $\mathrm{Var}(D_{\rm out}|_{f_2=1})$ for the same target ADC accuracy. Thus, overall, T is essentially set by $\mathrm{Var}(D_{\rm out}|_{f_1=1})/\mathrm{P}(f_1 = 1)$ and $\mathrm{Var}(D_{\rm out}|_{f_2=1})/\mathrm{P}(f_2 = 1)$. Let us first analyze $\mathrm{P}(f_1 = 1)$, i.e.,

$$\mathrm{P}(f_1 = 1) = \mathrm{P}(V_{l1} \le V_{\rm in} \le V_{r1}) \tag{13}$$

where V_{l1} and V_{r1} are the window detector left and right boundaries, given by

$$V_{l1} = -1/4 - V_{p1} + V_{\rm os1} + v_{n,\rm comp1} - v_{n,\rm jitter1} \quad (14)$$

$$V_{r1} = -1/4 + V_{p1} + V_{\rm os1} + v_{n,\rm comp1} + v_{n,\rm jitter1} \quad (15)$$

where $2V_{p1}$ is the nominal width of the window detector, $V_{\rm os1}$ is the comparator offset, $v_{n,\rm comp1}$ is the comparator noise, and $v_{n,\rm jitter1}$ indicates the input referred variation in the window width due to timing jitter. $v_{n,\rm jitter1}$ is given by

$$v_{n,\rm jitter1} = t_{\rm jitter1}\frac{dV_{\rm comp}}{dt} = t_{\rm jitter1}\frac{V_{p1}}{\tau_{c1}} \quad (16)$$

where τ_{c1} is the comparator regeneration time constant, and $t_{\rm jitter1}$ is the total timing jitter due to comparator, XNOR, and replica-based delay block (see Fig. 2). Plugging (14), (15), and (16) into (13)

$$\mathrm{P}(f_1 = 1) \approx 2g_1V_{p1} \quad (17)$$

where g_1 is the probability density of $V_{\rm in}$ at $-1/4$. This shows that offset, noise, and jitter do not affect $\mathrm{P}(f_1 = 1)$. Based on previous analyses and (6), we can also calculate $\mathrm{Var}(D_{\rm out}|_{f_1=1})$, as given by

$$\begin{aligned}\mathrm{Var}(D_{\rm out}|_{f_1=1}) &\approx \mathrm{Var}(V_{\rm in}|_{f_1=1}) \\ &\approx \left(\frac{1}{3} + \frac{\sigma^2_{\rm jitter1}}{\tau^2_{c1}}\right)V^2_{p1} + \sigma^2_{\rm comp1} \quad (18)\end{aligned}$$

where we have assumed that $\alpha \approx 1$ and $\beta \approx 0$. The first term in (18) is due to $V_{\rm in}$ variation in the nominal window; the second one is due to timing jitter; and the last is due to comparator noise. Combining (17) and (18), we have

$$\frac{\mathrm{Var}(D_{\rm out}|_{f_1=1})}{\mathrm{P}(f_1=1)} \approx \frac{1}{2g_1}\left[\left(\frac{1}{3} + \frac{\sigma^2_{\rm jitter1}}{\tau^2_{c1}}\right)V_{p1} + \frac{\sigma^2_{\rm comp1}}{V_{p1}}\right]. \quad (19)$$

Interestingly, there is an optimum value for V_{p1} that minimizes (19) and leads to the shortest T, i.e.,

$$V_{p1,\rm opt} = \frac{\sigma_{\rm comp1}}{\sqrt{\frac{1}{3} + \frac{\sigma^2_{\rm jitter1}}{\tau^2_{c1}}}}. \quad (20)$$

$V_{p1,\rm opt}$ balances the variance contributions from all three sources. For example, if we assume that $\sigma_{\rm comp1} = 2$ mV, $\sigma_{\rm jitter1} = 10$ ps, and $\tau_{c1} = 20$ ps, $V_{p1,\rm opt} = 2.6$ mV. In general, we want V_{p1} to be slightly bigger than the RMS comparator noise to minimize T. Either a too large or a too small V_{p1} increases T. Following the same calculation, we obtain

$$\frac{\mathrm{Var}(D_{\rm out}|_{f_2=1})}{\mathrm{P}(f_2=1)} \approx \frac{1}{2g_2}\left[\left(\frac{1}{3} + \frac{\sigma^2_{\rm jitter2}}{\tau^2_{c2}}\right)V_{p2} + \frac{\sigma^2_{\rm comp2}}{V_{p2}}\right] \quad (21)$$

where g_2 is the probability density of $V_{\rm in}$ at $+1/4$. In summary, based on (19) and (21), we see the following.

1) For large busy ADC input signals, the proposed algorithm provides short convergence time. However, small dc-like input signals with too small g_1 and g_2 lead to a long convergence time. This problem can be alleviated by dynamically changing comparator thresholds in the background from $\pm 1/4$ to values with larger g_1 and g_2. This restriction only mildly affects the algorithm's practicality as discussed in [2] and [6].
2) Comparator noise $\sigma_{\rm comp}$ and timing jitter $\sigma_{\rm jitter}$ set a lower limit on T.
3) Optimal V_p given by (20) minimizes convergence time and would be comparable to comparator noise, as long as timing jitter is smaller than comparator regeneration time constant.
4) T does not depend on the comparator offset, which is favorable compared to [6] whose T increases with $\sigma_{\rm os}$.

C. Delay Block

Ignoring DFF setup time in Fig. 2, V_p is set by the condition $\tau_R(V_p) = \tau$. The delay block is shared by all sub-ADC comparators and is realized using a replica path consisting of a comparator with a differential input V_r and an XNOR gate, as shown in Fig. 2, to ensure good tracking of τ and τ_R across PVT variations. The XNOR size is scaled up by a factor $N > 1$ as it drives the entire DFF array. For instance, $N > 16$ for a 4-bit stage to account for parasitics. N can be adjusted to account for DFF setup time. The replica comparator size is scaled by M, where $M < N$, such that its capacitive load and regeneration time constant $\tau_{\rm cr}$ are larger than those of main comparators by a factor $\alpha \approx N/M$. The differential input of the replica comparator V_r sets V_p. For a desired V_p, $V_r = V_pe^{\alpha}$. As each comparator in the sub-ADC has a different $V_{\rm ref}$, this can represent a systematic mismatch in V_p if the comparator transient response for small differential inputs depends on $V_{\rm ref}$. This systematic mismatch can be eliminated by using a switched capacitor technique to perform subtraction at each comparator's input as in [13]. In this case, the replica comparator reference $V_{\rm refr}$ can be set to any of the sub-ADC comparator references. In the presence of replica comparator offset $V_{\rm os}$ and assuming $V_r = V_{\rm ro} + \delta_{\rm vr}$, where V_{r0} is the nominal value and $\delta_{\rm vr}$ represents an error, V_p is given by

$$V_p = (V_r + V_{\rm os})e^{-\frac{\tau_{\rm cr}}{\tau_c}} = V_{p,0} + (V_{\rm os} + \delta_{\rm vr})e^{-\alpha} \quad (22)$$

where $V_{p,0}$ is the nominal value. This shows that V_p has low sensitivity to $V_{\rm os}$ and $\delta_{\rm vr}$. For instance, for $\alpha = 4$, the impact of these errors is attenuated by 55 times. This is in contrast to [6], where replica comparator offset sets the window width. Relying on comparator decision time enables the generation of smaller and better controlled detection windows around comparator thresholds and hence reduces convergence time. In general, for small V_p, random mismatches in τ have a small impact. For a timing mismatch δ_τ in τ, V_p is given by

$$V_p = V_{p,0}e^{\frac{\delta_\tau}{\tau_c}}. \quad (23)$$

A large timing mismatch of $\delta_\tau = \tau_c$ approximately triples the window size, which for small window sizes is a much smaller increase compared to the impact of comparator offset in [6]. For instance, for a target V_p of 3 mV, a timing mismatch of τ_c increases V_p to 8 mV, which is much smaller than a dynamic comparator offset that sets the window width in [6]. The circuit shown in Fig. 2 was designed and simulated in 180 nm CMOS technology assuming a 4-bit stage. A dynamic comparator [10] was used with regeneration time constant and three-sigma offset of 30 ps and 25 mV, respectively. V_p was

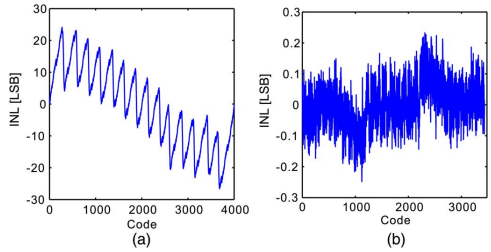

Fig. 6. 12-bit ADC INL. (a) Before calibration. (b) After calibration.

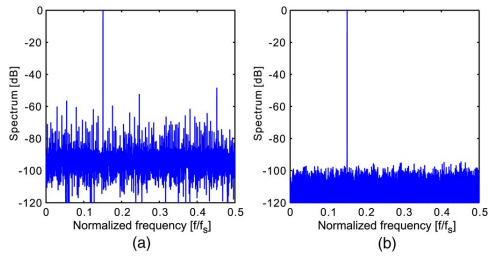

Fig. 7. ADC output spectra. (a) Before calibration. (b) After calibration.

set to 3 mV and $\alpha = 4$. δ_τ was obtained using Monte Carlo simulation results, including both random process variations and mismatches. A three-sigma value of 15 ps was obtained for δ_τ that is dominated by random mismatches. This corresponds to a worst case detection window width of $2V_p \approx 10$ mV, which compares to 35 mV for [6] that relies on comparator offset. A temperature sweep from -25 to 90 °C had a negligible effect on V_p. This verifies the robustness of the proposed technique.

III. Simulation Results

A 12-bit pipelined ADC similar to the one used in [2], [6], and [12] is modeled in MATLAB. It consists of a first 3.5-bit stage followed by ten 1.5-bit stages. The model parameters are as follows:

1) OTA gain mean $\mu_G = 10^2$ and variance $\sigma_G^2 = 10$;
2) capacitor mismatch $\sigma_\Delta = 0.1\%$;
3) detection window width $2V_p = 6$ mV;
4) comparator offset $\sigma_{\rm os} = 10$ mV;
5) comparator noise $\sigma_{\rm comp} = 2$ mV;
6) jitter in DTQ $\sigma_{\rm jitter} = 10$ ps;
7) comparator regeneration time constant $\tau_c = 20$ ps.

Fig. 6 shows the INL. Before calibration, INL is $+24.1/-26.6$ LSB; after calibration, INL is reduced to $+0.23/-0.25$ LSB. The postcalibration INL is limited by the uncalibrated stages and fluctuations in the extracted $\hat{\beta}$s. Other error sources, such as sample-and-hold nonlinearity, amplifier offset, and charge injection, are ignored, as in [2] and [6]. For the target 12-bit accuracy, it is sufficient to calibrate only the first five stages. All stages are simultaneously calibrated as in [6] and [12]. After calibration, the digital output $D'_{\rm out}$ is truncated to 12 bits. Fig. 7 shows ADC output spectra (8192-point fast Fourier transform). Before calibration, SNDR and spurious-free dynamic range (SFDR) are 44 and 48 dB, respectively. After calibration, they are improved to 72 and 93 dB. The calibrated SNDR is not equal to the ideal 12-bit value of 74 dB, for the effective radix of each stage is less than 2 due to the low amplifier gain. Fig. 8(a) shows the convergence of $\{\hat{\beta}_i\}(i \in [1, 7])$ of the first 3.5-bit stage. Here, the step size

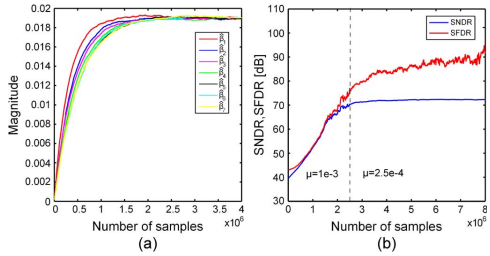

Fig. 8. Convergence of (a) $\hat{\beta}$ of the first stage and (b) ADC SNDR/SFDR.

is chosen to be 10^{-3}. Fig. 8(b) shows corresponding SNDR and SFDR. The LMS loop converges, and an SNDR beyond 70 dB is reached after 2.5×10^6 samples, which translates to 25 ms assuming an ADC sampling rate of 100 MS/s. At this point, μ is decreased to 2.5×10^{-4}, which is to reduce the RMS error of the estimated coefficients and hence obtain a higher SFDR without impacting SNDR convergence time. SFDR is better than 86 dB after 6×10^6 samples. As environmental changes, e.g., temperature variations, are typically associated with large time constants, a smaller steady-state μ, i.e., slower tracking, is usually acceptable.

IV. Conclusion

This brief introduced a novel digital background calibration technique with low analog complexity. It embraces comparator DTQ to identify analog inputs that fall close to comparator thresholds for calibration purposes. Fast convergence is achieved by using an optimum PVT-insensitive comparator input detection window size. The technique enables the use of low-gain amplifiers and simple capacitor layout to save power and area.

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