A Very High Energy-Efficiency Switching Technique for SAR ADCs

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***Abstract*— A high energy-efficiency capacitor switching scheme for a successive approximation register (SAR) analog-to-digital converter (ADC) is presented in this paper. The proposed switching technique achieves a zero energy dissipation in the first 2 comparison cycles and a 4X reduction in total capacitance used in the digital-to-analog converter (DAC), i.e., for the same total capacitance, the proposed technique can produce 2 additional bits of resolution than a conventional SAR. The proposed method can achieve 95% savings in switching energy over a conventional SAR. The result has been verified through behavioral simulations.**

I. Introduction

SAR ADC is a very popular choice for low speed, high resolution applications primarily because of its digital nature and low power consumption [1]–[3]. For a high resolution SAR, switching power can constitute a significant part of the total power consumption, and hence, a high energy-efficiency switching scheme can go a long way towards reducing the overall power consumption. The conventional SAR capacitive DAC is energy-efficient if its initial guess of the input is correct, but dissipates a lot of switching energy when its guess is wrong, and it has to charge up a capacitor from ground to V_{ref} during a 'down' transition. A lot of study has been done on reducing the switching energy. [4] uses a split-capacitor technique to make the switching energy required to charge up a capacitor from ground to V_{ref} the same for both 'up' and 'down' transitions of the DAC. The split-capacitor technique provides 37% savings in switching energy over a conventional SAR. [5] uses an energy saving technique in combination with capacitor splitting, to achieve 56% savings in switching energy. [6] has a monotonic switching scheme that can achieve 81% switching energy savings. Both [7], [8] have a similar V_{cm} based switching and achieve 88% savings in switching energy . [9] proposes a V_{cm} based switching technique but switches the last bit between V_{cm} and '0' to get an additional bit of resolution.

A new, highly energy-efficient switching technique will be presented in this paper. A key to reducing switching energy in the capacitor array is to cut down on the energy dissipated in the first few comparison cycles as well as to reduce the number of capacitors. Most of the energy is dissipated in the first two comparison cycles. For the switching technique presented, no energy is dissipated in the first two comparisons. The second method of lowering energy consumption is to reduce the total capacitance in the DAC. [4]–[8] all achieve a 2X reduction in the capacitance in the DAC. This paper will show that a further 2X reduction is possible, i.e, for the same total capacitance, 2 additional bits of resolution can be obtained compared to the conventional SAR. The 4X reduction in capacitance in a SAR is the highest reduction demonstrated to the best of the authors' knowledge. For a 10-bit SAR, the proposed switching technique achieves 95% savings in switching energy over the conventional one. The proposed technique does not require an accurate V_{cm} and a 5% error in V_{cm} results in an INL of 0.05 LSB. The authors have shown in [10] that 98% switching energy savings can be achieved if an accurate V_{cm} can be ensured. The proposed switching technique can also be readily extended to incorporate bottom-plate sampling for a high resolution (>10-bits) SAR. A comparison of the proposed technique with the existing art is summarized in Table I.

The switching technique is discussed in detail in Section II. Section III discusses how the proposed switching technique can be combined with bottom-plate sampling for high resolution SAR ADCs. Finally the conclusion is brought up in Section IV.

II. Proposed switching technique

As already discussed in Section I, the keys to reducing switching power is to reduce the capacitance in the DAC and to reduce energy in the initial comparison cycles, as they account for most of the switching energy. The techniques used in this work, which achieve these goals, are discussed in detail in the following sub-sections.

A. Reduction of switching energy in conversion cycles

Use of top-plate sampling ensures that the first comparison does not draw any energy from V_{ref}. For the proposed scheme, no energy is drawn from V_{ref} during the second comparison either. The energy dissipated in charging up a most-significant-bit (MSB) capacitor from ground to V_{ref} in the second comparison cycle accounts for almost two-thirds of the total switching energy in [6] and by designing a switching scheme in which this energy can be set to '0', a very high energy-efficiency is achieved. A better understanding of how the proposed scheme can nullify the switching energy during the second comparison, can be obtained from Fig. 1.

Let us assume that initially the charge stored in the top-plate of the capacitors is 'Q'. Therefore, from Fig. 1(a), applying charge conservation at the top-plate, $V_x - V_y = -V_{ref}/2$. The

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TABLE I

COMPARISON WITH EXISTING SWITCHING TECHNIQUES FOR AN n-BIT SAR.

switching method	conventional	split-capacitor [4]	monotonic [6]	V_{cm} based [7], [8]	This work	
sampling plate	bottom	bottom	top	top/bottom	top	bottom
norm. switching power	1	0.63	0.19	0.12	0.05	0.14
no. of unit capacitors	2^n	2^n	2^{n-1}	2^{n-1}	2^{n-2}	

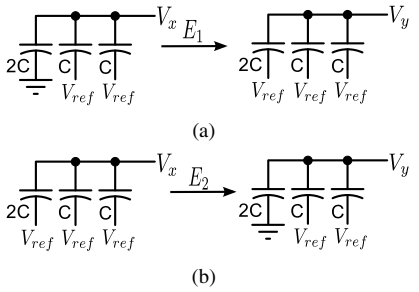

Fig. 1. Illustration of the idea behind energy saving.

switching energy can be calculated as $E_1 = V_{ref} \cdot 2C\{V_{ref} + 2(V_x - V_y)\} = 0$. However, if the switching sequence is reversed as in Fig. 1(b), applying charge conservation at the top-plate gives $V_x - V_y = V_{ref}/2$. The switching energy is given by $E_2 = V_{ref} \cdot 2C\{V_x - V_y\} = CV_{ref}^2 \neq 0$. The switching sequence in Fig. 1(b) is used in the monotonic switching scheme of [6], while the proposed scheme applies the concept of zero energy transfer of Fig. 1(a) to the second comparison cycle to get an energy saving of almost two-thirds over [6]. An added benefit of having the MSB capacitors starting from ground potential at the first comparison cycle is the reduction in common-mode voltage swing at the virtual node. With the proposed switching technique, the common-mode voltage at the virtual node starts at V_{cm}, swings up to $3V_{ref}/4$ and then gradually comes down to V_{cm} again. This swing is half of the common-mode variation in [6] and the dynamic offset associated with the common-mode variation is also reduced. The common-mode voltage variation is shown in Fig. 2. The common-mode voltage for the proposed scheme stays very close to V_{cm} for most of the comparison cycles, thus enabling the use of well-known and often-used comparator designs.

The reduced common-mode voltage variation also reduces the non-linearities associated with a signal dependent offset, particularly, if a fully differential comparator is not used. It should be pointed here that by switching the last unit capacitor only between (V_{ref}, V_{cm}), a zero average energy dissipation for the penultimate comparison cycle is achieved.

B. Capacitance reduction

The existing energy-efficiency switching techniques already achieve a 2X reduction in the total capacitance in the DAC. Therefore, for the same total capacitance, while a conventional SAR divides the voltage interval $[0, V_{ref}]$ into 2^m levels, the existing energy-efficient techniques partition the same interval into 2^{m+1} levels. The interval $[0, V_{ref}]$ can be partitioned

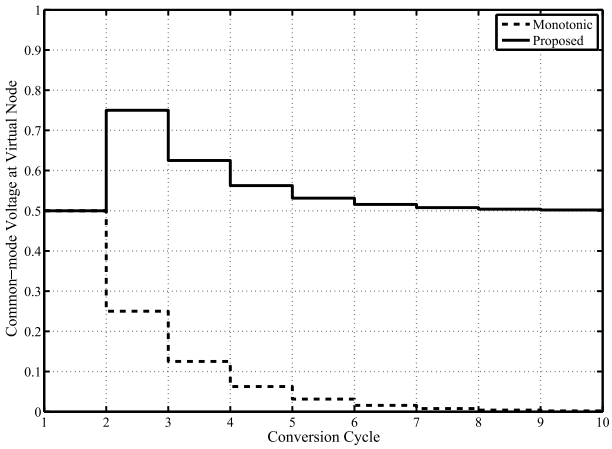

Fig. 2. Common-mode voltage variation at the comparator input ($V_{ref} = 1$).

further to yield 2^{m+2} levels. This can be easily done by switching the last unit capacitor in the DAC between (V_{ref}, V_{cm}) instead of $(V_{ref}, 0)$. Thus, for the same total capacitance, the proposed technique can yield 2 additional bits of resolution over a conventional SAR, or, in other words, a 4X reduction in capacitance can be achieved for the same resolution.

An example 4-bit SAR which uses the proposed switching technique is shown in Fig. 3, which illustrates the concepts of energy saving in the comparison cycles, as well as the capacitance reduction. For the same capacitive DAC, a conventional SAR would have only a 2-bit resolution.

C. Switching energy comparison

The average switching energy dissipation for an n-bit SAR using the proposed technique can be shown to be $E_{avg} = \left(\sum_{i=2}^{n-2} 2^{n-3-i}\right) CV_{ref}^2$ while that for an n-bit conventional SAR ADC is given by $E_{avg,conv} = \left(\sum_{i=1}^{n} 2^{n+1-2i}\left(2^i - 1\right)\right) CV_{ref}^2$ Thus for a 10-bit SAR, the conventional method has an average switching energy of $1363.3\ CV_{ref}^2$ while the proposed technique has an average switching energy of $65.3\ CV_{ref}^2$, which is a reduction of 95.2%. A MATLAB simulation was performed to compare the average switching energy of the proposed technique with the existing art, and is shown in Fig. 4. It can be seen that the proposed switching technique indeed achieves a significant saving in switching energy. Also, during each comparison cycle, only one capacitor is switched. This simplifies the digital control logic and at the same time reduces the power dissipated in driving the switches.

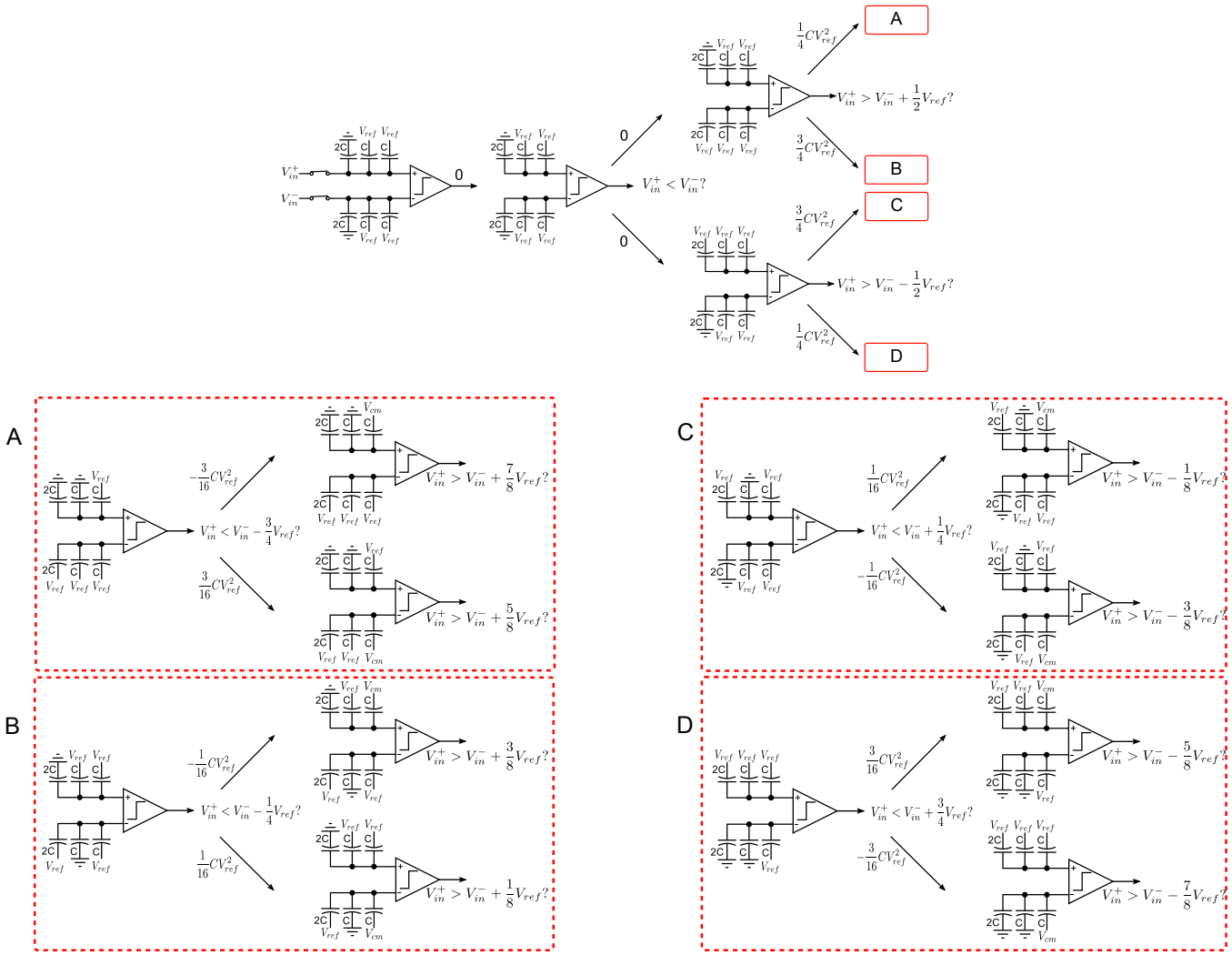

Fig. 3. Proposed switching technique for a 4-bit SAR ADC with top-plate sampling.

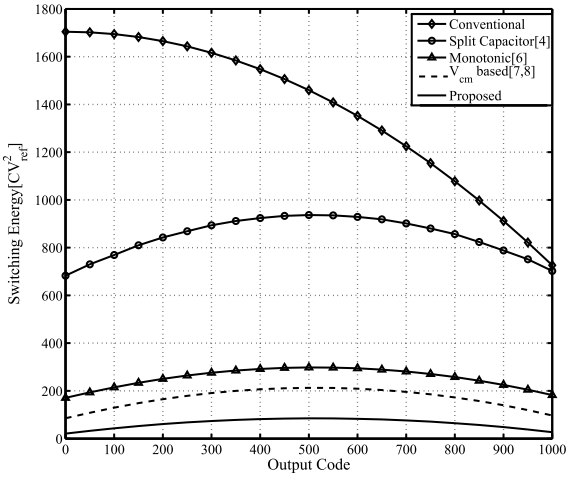

Fig. 4. Comparison of the proposed scheme with existing art.

III. Switching Technique for High Resolution SARs

For SAR ADCs striving for high resolution (>10-bits), bottom-plate sampling is necessary for canceling input-dependent charge injection. Consequently, the energy reduction schemes associated with top-plate sampling have to be modified to incorporate bottom-plate sampling. The proposed scheme can easily be adapted to bottom-plate sampling, and an example 4-bit SAR ADC incorporating the modified switching scheme is shown in Fig. 5. With the introduction of bottom-plate sampling, the switching energy in the first conversion cycle is no longer '0'. The average switching energy is given by $E_{avg} = \left(\frac{2^{2n-4}-2^{n-3}-1}{2^{n-1}} + \left(2^{n-3} - \frac{1}{2}\right) \sum_{i=2}^{n-1} \frac{1}{2^i} \right) CV_{ref}^2$. For a 12-bit SAR, the switching energy dissipated in a conventional DAC is 5459.3 CV_{ref}^2, while the switching energy consumed by the proposed technique is 767.25 CV_{ref}^2, which amounts to 86% energy efficiency for the proposed technique. Thus, even with bottom-plate sampling incorporated, the proposed technique still has a very high energy-efficiency while not degrading the linearity of a high resolution SAR. The switching energy is slightly more than that reported in [7], [8], but the energy spent in driving the switches themselves is one-half

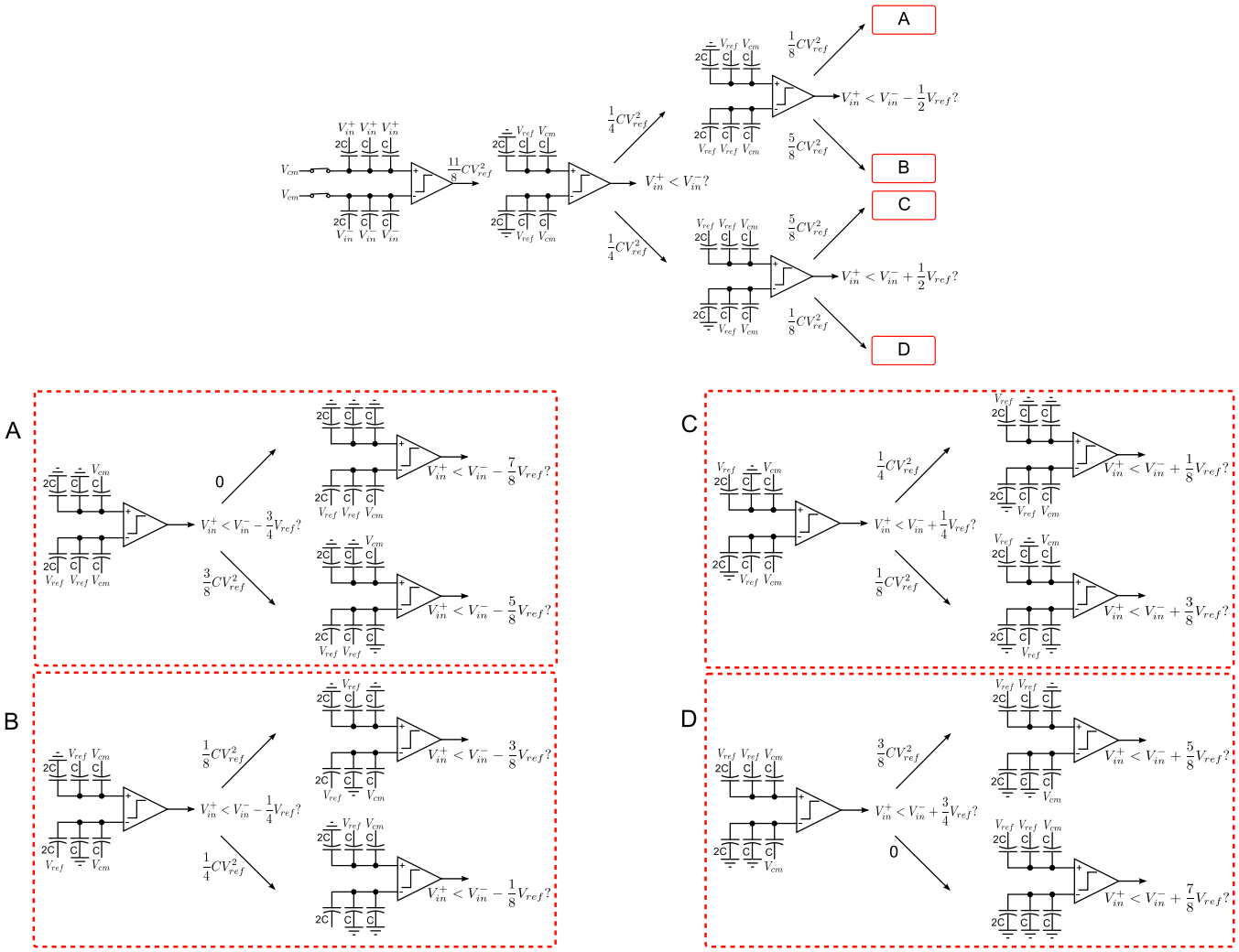

Fig. 5. Proposed switching technique for a 4-bit SAR ADC with bottom-plate sampling.

that reported in [7], [8].

IV. Conclusion

A high energy-efficiency capacitor switching method with energy savings of 95% for a SAR ADC, has been presented. Using the proposed method, the switching power is almost one-third of the highest efficiency technique reported. The proposed scheme also ensures that for the same total capacitance, 2 additional bits of resolution can obtained when compared with a conventional SAR. The proposed technique can readily be extended to incorporate bottom-plate sampling for high resolution SAR ADCs. An additional benefit of the proposed technique is the relaxation of the matching criteria in the DAC as for the same total capacitance, the proposed technique can make use of a 4 times larger unit capacitor which reduces the integral and differential non-linearities by 2 times compared to a conventional SAR.

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