An Energy-Efficient Hybrid SAR-VCO ΔΣ Capacitance-to-Digital Converter in 40-nm CMOS

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***Abstract*— This paper presents a highly digital, 0-1 MASH capacitance-to-digital converter (CDC). The CDC works by sampling a reference voltage on the sensing capacitor and then quantizing the charge stored in it by a 9-bit successive approximation register analog-to-digital converter. The residue is fed to a ring voltage-controlled oscillator (VCO) ΔΣ and quantized in time domain. The outputs from the two stages are combined to produce a quantized output with the first-order noise shaping. The proposed two-stage architecture reduces the impact of the VCO's nonlinearity. A digital calibration technique is used to track the VCO's gain across process, voltage, and temperature. The absence of any operational amplifier and low oversampling ratio for the VCO results in high energy efficiency. A prototype CDC in a 40-nm CMOS process achieves a 64.2-dB SNR while operating from a 1-V supply and using a sampling frequency of 3 MHz. The prototype achieves a CDC figure of merit of 55 fJ/conversion-step.**

***Index Terms*— Capacitance sensing, capacitance-to-digital converters (CDCs), noise shaping, successive approximation register (SAR), voltage-controlled oscillator (VCO).**

I. Introduction

CAPACITIVE sensors are widely used to measure a variety of physical quantities, such as pressure, position, proximity, and humidity to name a few [1]–[6]. Capacitive sensors are also increasingly being used in biomedical applications [7], [8]. A key reason for the widespread use of capacitive sensors is that the sensor itself does not consume any static power, and hence, it is very suitable for low-power applications [9]. The bulk of the power consumption comes from the electronic readout circuit used to digitize the sensor capacitance. Hence, a capacitance-to-digital converter (CDC) needs to have high energy efficiency while having a high resolution.

A wide variety of architectures have been reported in the literature for the CDC design, including successive approximation register (SAR) [10]–[13], ΔΣ [4], [14]–[17], dual-slope [2], [18], zoomed-in [19]–[21], and period/pulsewidth modulation (PM/PWM) [9], [22]–[25], to name a few. An SAR-CDC samples a reference voltage across the sensing capacitor and performs quantization by redistributing the stored charge across a capacitive digital-to-analog converter (DAC), similar to an SAR analog-to-digital converter (ADC). Since an SAR ADC has very high energy efficiency for medium resolution, it seems intuitive that simply using an ADC with high energy efficiency will result in a CDC with high energy efficiency. Thus, an SAR ADC should be a good candidate for a CDC. However, charge sharing between the sensing capacitor and the capacitive DAC lowers the voltage swing at the comparator input, forcing the comparator to burn more power to resolve its input with high accuracy. This results in reduced energy efficiency for an SAR-based high-resolution CDC. To address charge sharing between the sensing capacitor and the SAR DAC, the technique in [10] uses an operational transconductance amplifier (OTA) to perform an active charge transfer. In addition, correlated double sampling used in [10] results in immunity to large parasitic capacitances on the sensor node as well as variations in reference voltage and amplifier offset. While this technique solves the issue of reduced swing at the comparator input, the problem of the power hungry OTA still remains and the energy efficiency is 1.33 pJ/step. Recent works [11]–[13] have shown that the use of power efficient inverter-based amplifiers as SAR comparator can result in purely SAR CDCs with energy efficiency as high as 35 fJ/conversion-step.

Switched capacitor ΔΣ CDCs [4], [14]–[17] are suitable for high resolution but have low energy efficiency. This is because a single-bit ΔΣ CDC requires large oversampling ratio (OSR) to achieve high resolution. Thus, the CDC has to charge/discharge the large sensing capacitor many times to produce the digitized output, which lowers its energy efficiency. In addition, the integrators used to build the loop filter generally use power hungry OTAs, which also contributes to low energy efficiency. As in [4], a programmable capacitor is often used to cancel the baseline capacitance of the sensor.

Thedual-slope converter [2], [18] is another popular choice for CDCs due to its simplicity. The sensing capacitor is first charged using a known reference voltage. The charge stored across the sensing capacitor is then transferred to another capacitor and discharged iteratively using a reference capacitor, C_{REF}. The number of iterations required to discharge is proportional to the sensing capacitance. A capacitor,

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C_B, is used to shorten the conversion time of the CDC by negating the base capacitance. However, dual-slope CDCs do not usually have a high resolution as the iterative discharging process requires 2^N cycles for N-bit resolution. In addition, OTAs are often used in the reference buffer, which control the amount of charge subtracted through C_{REF}, resulting in low energy efficiency.

Yet another often used CDC utilizes the zoomed-in architecture [19]–[21]. The zoomed-in architecture combines an SAR with a ΔΣ value. The SAR stage performs a coarse quantization of the sensing capacitance, and the residue is sent to the ΔΣ value. Since the first-stage SAR already performs a coarse quantization, the resolution requirement from the ΔΣ value is low, and only a modest OSR is required which improves energy efficiency compared to stand-alone ΔΣ CDC. However, existing zoomed-in CDCs use OTAs in the ΔΣ loop filter, which results in low energy efficiency.

PM/PWM CDCs have an intrinsic semidigital nature as quantization is carried out using digital counters. Most PM/PWM CDCs use a relaxation oscillator to transform the sensing capacitance into a time period through PM or PWM. However, PM/PWM CDC techniques typically use an OTA for charge transfer, which degrades their energy efficiency. The technique in [26] proposes a highly digital alternative by using a ring oscillator whose delay is controlled by the sensing capacitor. A frequency domain 1-bit ΔΣ ADC is formed by comparing the oscillator delay with that of a reference oscillator by using a bang-bang phase/frequency detector (PFD). The PFD output is fed back to the oscillator to close the feedback loop. While the technique is highly digital, it has a low energy efficiency due to its high OSR of 825. A recent work [27] presents a highly digital C-F CDC by using a delay chain to discharge the sensing capacitor. The time taken for the delay in the inverter chain to catch up with delay in a reference inverter chain is proportional to the sensing capacitor. While the technique in [27] is highly digital, its resolution is limited and is not suitable for sensing small capacitors despite its wide sensing range.

To address the challenge of designing high-resolution, energy-efficient CDC, we present a two-stage ΔΣ CDC architecture that combines an SAR and a ring voltage-controlled oscillator (VCO). The SAR+VCO architecture has been shown to have a very high energy efficiency when used as an ADC [28]. The SAR performs a 9-bit coarse quantization, and the residue is sent to the VCO for fine quantization. VCO is effective at quantizing small voltages in the time domain. Moreover, it provides an intrinsic first-order noise shaping, which increases the resolution of the CDC. The combination of SAR with VCO addresses the challenges faced by stand-alone SAR and ΔΣ CDCs: 1) reduced swing at comparator input for SAR CDC and 2) high OSR requirement for ΔΣ CDC. The VCO can absorb quantization errors in the SAR and, thus, relaxes the precision requirement for the SAR comparator and permits the use of a small dynamic comparator for power saving. The 9-bit SAR greatly reduces requirements on the VCO linearity and allows the use of low OSR. In addition, the proposed ΔΣ CDC is highly digital, scaling friendly, and OTA-free. While [29] introduces the proposed CDC, this paper explores the proposed architecture in greater detail and identifies the tradeoffs involved in the design. The remainder of this paper is organized as follows. The proposed CDC design is presented in Section II, the measurements results are presented in Section III, and the conclusion is brought up in Section IV.

II. Proposed CDC Design

A. CDC Architecture

Fig. 1 shows the proposed SAR+VCO CDC with its timing diagram. The CDC digitizes the sensing capacitor C_{SENSE} in a single-ended fashion.The proposed CDC architecture can easily be modified for differential operation by using a differential SAR first-stage and dual VCOs in the second stage. The capacitor C_{OFF} is used for range extension of the CDC. Both C_{SENSE} and C_{OFF} are off-chip capacitors. During the sensing phase ϕ_1, V_{dd} is sampled onto C_{SENSE}. The bottom plate of 9-bit SAR capacitive DAC (C_{DAC}) as well as C_{OFF} is reset during ϕ_1, while their top plates are held at V_{cm}. The net charge on the SAR comparator input during ϕ_1 is given by

$$Q_{\text{comp},\phi_1} = C_{\text{SENSE}}(V_{\text{cm}} - V_{\text{dd}}) + (C_{\text{OFF}} + C_{\text{DAC}} + C_{\text{PAR}})\, V_{\text{cm}} \quad (1)$$

where C_{PAR} consists of parasitic capacitance at the comparator's input, input capacitance of VCO quantizer (VCOQ), the CDAC bottom-plate parasitic capacitance, capacitance due to the electrostatic discharge devices, bond-pad capacitance, and printed circuit board trace capacitance, and is represented by a lumped capacitance in Fig. 1.

At the end of ϕ_1, C_{SENSE} is switched to V_{ss}, C_{OFF} is switched to V_{dd}, and the top plate of C_{DAC} is left floating. The SAR ADC starts quantizing the charge transferred onto C_{DAC} during the phase ϕ_2. After the SAR has finished quantization, the residue voltage at the comparator's input is given by

$$V_{\text{res}} = V_{\text{cm}} + GV_{\text{dd}}\left[\left(\frac{C_{\text{SENSE}} - C_{\text{OFF}}}{C_{\text{DAC}}}\right) - d_1\right] \quad (2)$$

where $G = \{C_{\text{DAC}}/(C_{\text{SENSE}} + C_{\text{OFF}} + C_{\text{DAC}} + C_{\text{PAR}})\}$, d_1 is the first-stage SAR digital output, and $\{d_1 - (C_{\text{SENSE}} - C_{\text{OFF}})/C_{\text{DAC}}\}$ is the SAR quantization error q_1. The size of unit capacitor in the capacitive DAC is 12 fF. Hence, the 9-bit SAR ADC can sense a maximum capacitance difference of $(C_{\text{SENSE}} - C_{\text{OFF}})$ of 6 pF. It can be seen from (2) that increase in C_{DAC} leads to more attenuation in the input swing of the SAR comparator. A higher resolution SAR will have a higher value of C_{DAC} for the same unit capacitance and thus will suffer from more attenuation in the comparator input voltage swing. For every two times reduction in input swing, the comparator has to burn four times more power to reduce its thermal noise so that the SAR can achieve the desired accuracy. In contrast, the proposed two-stage architecture allows the front-end SAR to have a medium resolution, which allows a smaller C_{DAC} value and, hence, lower attenuation of the comparator input swing. In addition, any error in the SAR stage is corrected in the second-stage VCO as long as the VCO stage is not overloaded by error in the SAR stage. This allows the use

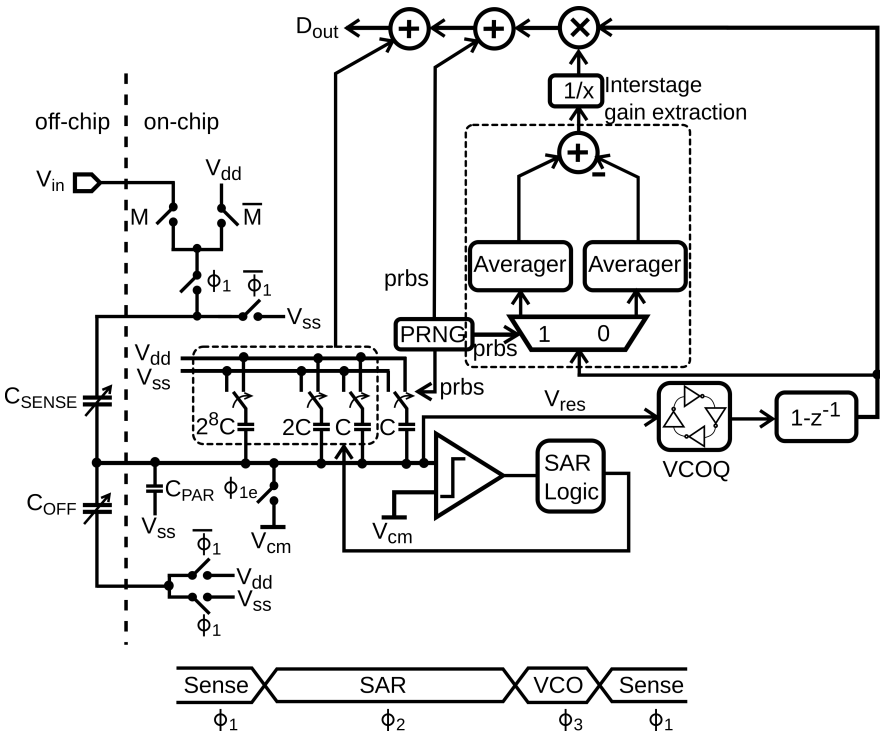


Fig. 1. Circuit diagram showing the proposed SAR+VCO CDC.

of a low-power comparator in the proposed design which, in turn, improves energy efficiency.

The residue voltage, V_{res}, is sent to the VCOQ during the phase ϕ_3. The VCO performs a phase-domain integration of V_{res} [30] and its output d_2 is obtained by sampling the phase and performing a digital differentiation $(1-z^{-1})$ on it. Thus, the second-stage output is given by

$$d_2 = G_A V_{\text{res}} + (1-z^{-1})q_2 = G_A^{'} \cdot \frac{V_{\text{res}}}{V_{\text{dd}}} + (1-z^{-1})q_2 \tag{3}$$

where G_A is the analog interstage gain given by $Gk_{\text{vco}}T_{\phi_3}$, k_{vco} is the VCO tuning gain, T_{ϕ_3} is the time over which the VCO integrates V_{res}, and $G_A^{'}$ is the scaled unit-less analog interstage gain given by $G_A^{'} = G_A \cdot V_{\text{dd}}$. The VCO consists of a seven-stage current-starved inverter chain. At any time instant, only one of the inverters is in a state of either positive or negative transition. Thus, for a seven-stage VCO, the instantaneous phase is quantized into 14 levels between $(0, 2\pi)$ corresponding to 7 positive and 7 negative transitions. The VCO gain is chosen carefully to ensure that there is no phase overflow during any sampling period. The final CDC output, D_{out}, is obtained by combining the first-stage SAR output d_1 and the second-stage VCO output d_2 scaled by a digital gain G_D that matches $G_A^{'}$. This is a challenge since $G_A^{'}$ depends on k_{vco} which is process, voltage, and temperature (PVT) sensitive.

A simple digital calibration technique is used to track $G_A^{'}$ across PVT. A pseudorandom number generator (PRNG) is built on-chip using a 20-stage linear feedback shift register. Its output $prbs$ (see Fig. 1) controls an LSB capacitor in the SAR capacitive DAC. When $prbs = 0$, the LSB capacitor is always connected to V_{ss}. When $prbs = 1$, the LSB capacitor is switched to V_{dd} at the end of ϕ_2. As a result, V_{res} increases by an LSB change in d_1. Thus, the change in d_2 due to $prbs = 1$ corresponds exactly to the interstage gain$G_A^{'}$. Hence, we can extract $G_A^{'}$ from the difference between the d_2 averages for $prbs = 1$ and $prbs = 0$. This is implemented easily in hardware by passing d_2 through a 1-to-2 DEMUX followed by two averaging blocks and a subtractor. This calibration technique operates without disturbing the normal operation of the CDC. To facilitate testing of the CDC, two operation modes are provided in the design. The operation modes are controlled by a 1-bit control word, M. When $M = 1$, the CDC is in its normal operation mode. When $M = 0$, the CDC is in test mode in which an external voltage V_{in} is sampled onto C_{SENSE} during ϕ_1. This allows a convenient way to test the linearity and resolution of the CDC by sampling a sine wave onto C_{SENSE} during ϕ_1 and plotting the output spectrum. It should be pointed out here that CDC performance measured with a fixed sensing capacitor and a variable voltage may not be fully representative of CDC performance measured with a variable sensing capacitor. The most accurate way to measure CDC performance is to sweep the sensing capacitor over its full range.

B. CDC Model

Fig. 2 shows the signal flow diagram of the proposed SAR+VCO CDC. Based on Fig. 2, the output of the CDC can be written as

$$D_{\text{out}} = \frac{(C_{\text{SENSE}} - C_{\text{OFF}})}{C_{\text{DAC}}} + q_1\left(1 - \frac{G_A^{'}}{G_D}\right) + \frac{q_2(1-z^{-1})}{G_D} - \text{prbs}\left(1 - \frac{G_A^{'}}{G_D}\right). \tag{4}$$

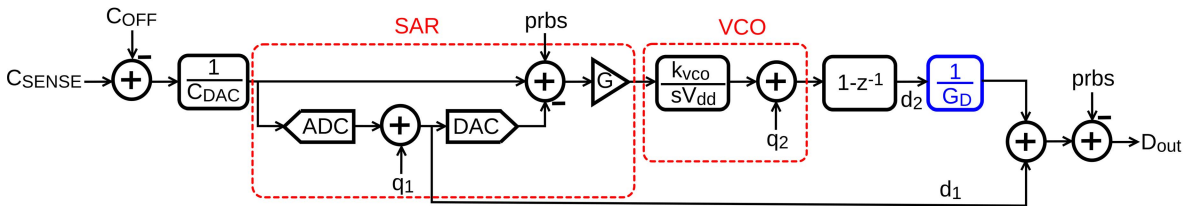


Fig. 2. Block diagram of the proposed CDC architecture.

If $G_A^{'} = G_D$, the SAR quantization noise q_1 as well as $prbs$ is canceled at the output. The final quantization noise at D_{out} comes solely from the VCO stage and is first order shaped. Any mismatch between $G_A^{'}$ and G_D will result in q_1 and $prbs$ leaking to the output, thus increasing the in-band noise floor and distortion. To ensure $G_A^{'} = G_D$, we digitally adjust G_D to match $G_A^{'}$. More specifically, we set

$$G_D \equiv G_A^{'} = \overline{d_2(\text{prbs} = 1)} - \overline{d_2(\text{prbs} = 0)} \tag{5}$$

where

$$d_2 = -q_1 G_A^{'} + q_2(1 - z^{-1}) + G_A^{'} \cdot \text{prbs}. \tag{6}$$

The averaging is done by an infinite-impulse response (IIR) filter. q_1 does not depend on $prbs$ and, hence, has very low correlation with $prbs$. Thus, q_1 is canceled in the subtraction between d_2 for $prbs = 1$ and $prbs = 0$. q_2 is the quantization noise of multi-bit VCOQ and has low power. Thus, q_2 can be easily averaged out by the IIR filter. It should be noted here that the calibration used in this paper removes any bias in $prbs$ by separately averaging d_2 for $prbs = 1$ and $prbs = 0$. Directly correlating d_2 with $prbs$ will result in the same accuracy as the method in (5) but will take longer to converge due to the bias in $prbs$.

C. Noise Analysis

Noise in the CDC comes from three sources: 1) kT/C sampling noise from the first stage; 2) thermal noise of the VCO; and 3) quantization noise. The comparator's thermal noise and the 0SAR quantization noise are canceled at the CDC output when the SAR output and the VCO output are combined. The rms capacitance noise due to sampling, when referred to the sensor input, is given by

$$\overline{C_{\text{sample},n}} = \sqrt{\frac{kT}{C_{\text{DAC}} + C_{\text{SENSE}} + C_{\text{OFF}} + C_{\text{PAR}}}} \cdot \frac{1}{G} \cdot \frac{C_{\text{DAC}}}{V_{\text{dd}}\sqrt{\text{OSR}}}. \tag{7}$$

For $C_{\text{DAC}} = 6$ pF and $C_{\text{SENSE}} = 6$ pF, $C_{\text{OFF}} = 0$, $C_{\text{PAR}} = 2$ pF, $V_{\text{dd}} = 1$V, and OSR =3, the rms capacitance noise is calculated to be 150 aF.

The rms capacitance noise due to the VCO, when referred to the sensor input, is given by

$$\overline{C_{\text{vco},n}} = \frac{\sqrt{2D_1(T_s - T_{\phi_3}) + 2D_2T_{\phi_3}}}{2\pi k_{\text{vco}} T_{\phi_3}} \cdot \frac{1}{G} \cdot \frac{C_{\text{DAC}}}{V_{\text{dd}}\sqrt{\text{OSR}}} \tag{8}$$

where D_1 is the phase diffusion constant [31] of the VCO during ϕ_1 and ϕ_2 phases, and D_2 is the phase diffusion constant of the VCO when it is integrating in the ϕ_3 phase. The phase diffusion constant D is evaluated from the value of phase noise $\mathcal{L}(\Delta\omega)$ at an offset of $\Delta\omega$ as $D = \{\mathcal{L}(\Delta\omega) \cdot (\Delta\omega)^2\}/2$.

A first glance at (8) indicates that the VCO noise, referred to the sensor input, is scaled up by $1/G$. It would therefore appear that the proposed architecture has no advantage over SAR CDC as $\overline{C_{\text{vco},n}}$ can only be reduced by dissipating more power in the VCO stage. However, a closer inspection will reveal that it is indeed not the case. This is mainly due to two reasons. First, as mentioned in Section II-A, for the same overall resolution as an SAR CDC, the SAR-stage in the proposed CDC has a lower resolution and, hence, a smaller C_{DAC} value. This results in a larger value of G for the proposed architecture and, hence, smaller amplification of VCO noise when referred to sensor input. Second, unlike comparator noise in SAR-CDC, $\overline{C_{\text{vco},n}}$ can be reduced without increase in power dissipation. It can be seen from (8) that $\overline{C_{\text{vco},n}}$ can be reduced by lowering the VCO frequency during the phases ϕ_1 and ϕ_2, which reduces D_1. Lowering the VCO frequency also reduces power consumption from the VCO-stage during the phases ϕ_1 and ϕ_2. While it may seem counter intuitive that we can achieve simultaneous reduction in VCO input-referred phase noise and power consumption, this only happens because we are reducing the VCO frequency during its idle phase (phases ϕ_1 and ϕ_2) and not reducing the VCO integration gain. This is implemented in a circuit design by lowering the VCO tail current. Stopping the VCO in phases ϕ_1 and ϕ_2 will result in even lower noise and power consumption, but is avoided as charge leakage will corrupt the phase value held by the VCO during the phases ϕ_1 and ϕ_2. Instead, the VCO is run at a low frequency during those two phases. Increasing the VCO integration gain $k_{\text{vco}}T_{\phi_3}$ is another way to reduce $\overline{C_{\text{vco},n}}$. However, increase in VCO gain increases the likelihood of VCO phase overflow. VCO phase overflow can be effectively addressed by using a counter to record the number of times the VCO phase overflows during any sampling period [32]. Thus, the use of the second-stage VCO provides increased immunity to charge sharing than SAR-CDC.

During the phases ϕ_1 and ϕ_2, the simulated $\mathcal{L}(\Delta\omega)$ at an offset of 0.1 MHz is -75.1 dBc/Hz and during ϕ_3, and the simulated $\mathcal{L}(\Delta\omega)$ at an offset of 0.1 MHz is -72.8 dBc/Hz. T_{ϕ_3} is 23.8 ns and T_s is 333.3 ns. The VCO was designed to have a k_{vco} of 5 GHz/V and a C_{PAR} of 2 pF is assumed for the calculations. Plugging these numbers into (8), $\overline{C_{\text{vco},n}}$ is calculated to be 0.71 fF.

In order to calculate the quantization noise of the CDC, we only need to calculate the quantization noise from the

VCO as quantization noise of the SAR stage will be canceled at the output. The VCO has a quantization step given by $1/(2Nk_{\rm vco}T_{\phi_3})$. When referred to the CDC input, the VCO quantization step can be written as $\Delta C_{\rm vco} = (C_{\rm DAC}/GV_{\rm dd})/(2Nk_{\rm vco}T_{\phi_3})$. Thus, the quantization noise for the CDC can be written as

$$q_{\rm CDC} = \frac{\Delta C_{\rm vco}}{\sqrt{12}} \cdot \left(\frac{\pi}{\sqrt{3}}({\rm OSR})^{-3/2}\right) = \frac{C_{\rm DAC}}{2\sqrt{12}GV_{\rm dd}Nk_{\rm vco}T_{\phi_3}} \cdot \left(\frac{\pi}{\sqrt{3}}({\rm OSR})^{-3/2}\right) g \quad (9)$$

where the term in parentheses comes from the first-order shaping [33] of VCO quantization noise. It can be seen from (9) that as long as the SAR and VCO stages are linear enough to meet the CDC linearity specification, the CDC SQNR is determined by the VCO quantization noise alone and does not depend on the number of bits from the SAR stage. The rms quantization noise is calculated to be 0.87 fF. Hence, the total rms capacitance noise referred to the sensor input is calculated to be 1.13 fF for an SNR of 65.7 dB at an OSR of 3.

D. Circuit Design

1) SAR Design: A strong-arm latch, shown in Fig. 3, is used as the comparator for the SAR stage. Noise and offset of the comparator do not affect the CDC linearity, and hence, a low-power comparator is used.

Quantization noise of the SAR stage as well as the comparator thermal noise does not contribute toward the CDC noise. Instead, the VCO noise determines the overall CDC noise as has been shown in Section II-C, provided the VCO is not overloaded, and both the SAR and VCO stages meet the overall linearity specification. For this design, a 9-bit SAR is sufficient to ensure that VCO has adequate linearity and does not require any linearity correction. Hence, the number of bits in the SAR stage does not affect the CDC SNR. However, if the number of bits in the SAR stage is set too low, the VCO input swing will increase and will result in VCO nonlinearity. The increased VCO input swing may result in VCO overflow, but this can be handled by using a counter to record the number of VCO phase overflows in one sampling period. Also, if the number of bits in the SAR stage is low, SAR quantization noise power will be high. For every 1-bit reduction in SAR resolution, quantization noise power will increase by four times and this will result in four times reduction in calibration convergence speed (see Section II-D3). Thus, from VCO linearity and convergence speed perspective, it is better to set SAR resolution high. However, for every 1-bit increase in SAR resolution, the comparator power has to quadruple to reduce thermal noise by 1 bit. Thus, there is an optimum resolution for the SAR stage. For the current design with a 9-bit SAR, the comparator power is 8 μW out of the 75-μW power consumption by the CDC. If the SAR resolution is increased by 1 bit, the comparator power will increase from 8 to 32 μW. This will increase the CDC power by 30% without any increase in SNR. On the other hand, if the SAR resolution is reduced by 1 bit, the comparator power can be reduced from 8 to 2 μW which will reduce the CDC power by 8% but will double the VCO input swing and quadruple the convergence time. The power saving will reduce further considering that we will require a counter to account for VCO overload. Thus, considering VCO linearity, calibration convergence, and CDC power, the SAR resolution is of 9 bit that is an optimal choice for this design.

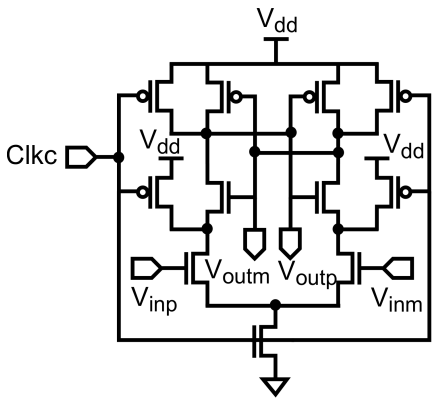


Fig. 3. Clocked comparator schematic.

In contrast to the proposed two-stage design, if an 11-bit SAR is used, the comparator power needs to scaled up by 16 times from 8 to 128 μW. Also, for the same unit capacitor, $C_{\rm DAC}$ will increase by four times and SAR switching power will increase from 24 to 96 μW. Hence, the CDC power will increase from 75 to 267 μW. The use of VCO as a phase-domain integrator to increase CDC resolution is also promising in the light of technology scaling. Unlike an SAR-based CDC which will not see improvement in SNR without burning more power, a VCO can lower its quantization noise through technology scaling. This is because technology scaling will result in lower gate delay and increased VCO gain ($k_{\rm vco}$). Increase in $k_{\rm vco}$ results in lower CDC quantization noise as can be seen from (9). Thus, technology scaling also allows for reduction in VCO power to maintain the same level of noise.

A key component of SAR design is the capacitive DAC array. Static element mismatch in the capacitor array will lead to increased in-band noise floor as well as harmonic distortion, which will show up at the CDC output. Fig. 4(a) shows the effect of capacitor array mismatch on the CDC performance. A behavioral-level MATLAB model of CDC was used for the simulations. Quantization noise and capacitor array mismatch are the sources of noise and distortion in the model. 2^{15} point simulation was performed with an input sine wave of 1.6 kHz and a sampling frequency of 3 MHz. $C_{\rm SENSE}$ of 6 pF was used for the simulation. At an OSR of 3, the CDC SNDR for ideal capacitor array was 66.8 dB, which reduced to 66.4 dB for capacitor array with a mismatch standard deviation of 0.3%. When the capacitor mismatch standard deviation was set to 1%, SNDR reduced to 63.3 dB with a rise in in-band noise floor and distortion. Fig. 4(b) shows the variation of SNDR with a mismatch standard deviation. Based on the simulation result, a capacitor mismatch 0.3% was chosen to achieve the desired CDC resolution. A 12-fF unit capacitor is

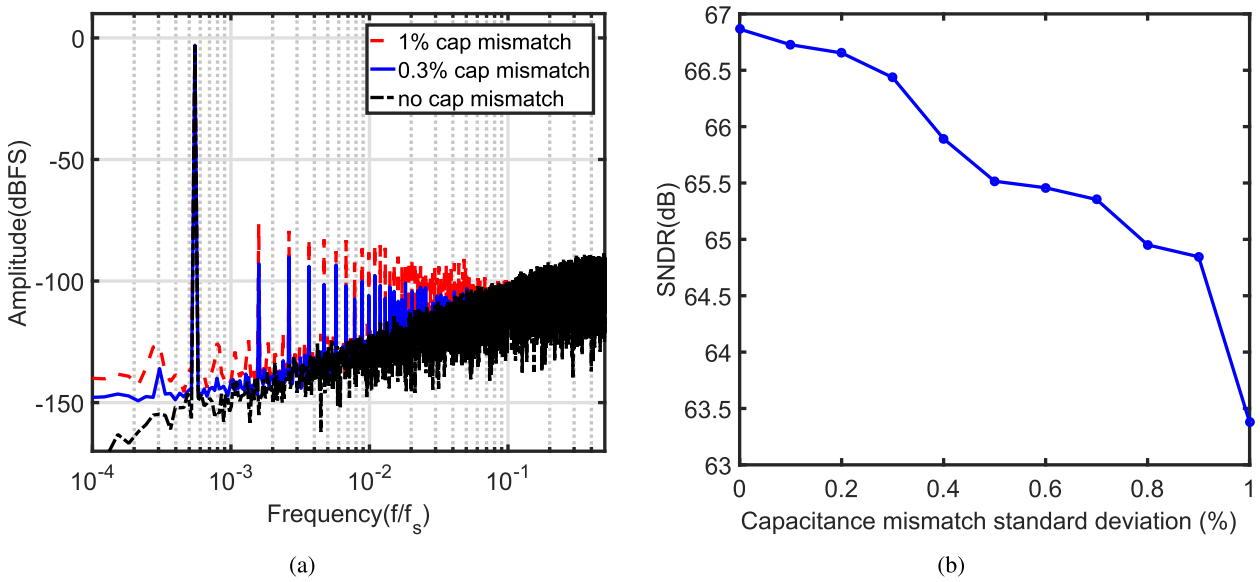


Fig. 4. (a) Effect of SAR capacitor array mismatch. (b) CDC SNDR versus capacitance mismatch.

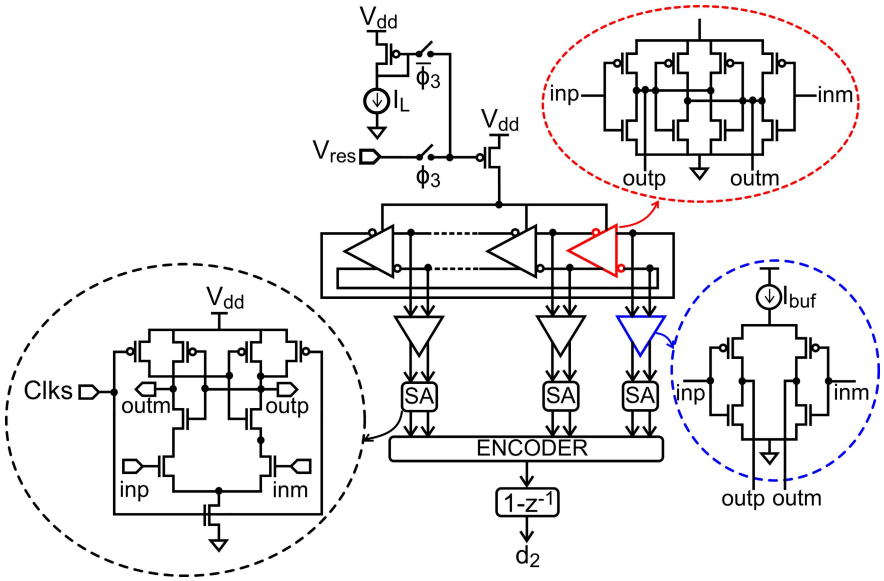


Fig. 5. Second-stage VCO circuit.

chosen by performing Monte Carlo simulations. A 1000 run Monte Carlo simulation was performed which confirmed that standard deviation for the 12-fF unit capacitor is 0.29%.

2) VCO Design: The second-stage VCO circuit is shown in Fig. 5. A seven-stage current-starved ring inverter chain is used as the VCO. Each VCO cell is made pseudodifferential to improve power supply rejection. PMOS tail current is chosen over NMOS to reduce flicker noise. During ϕ_1 and ϕ_2, the VCO is not switched OFF as charge leakage will introduce error in the phase value held by the VCO and degrade the CDC linearity. Instead, the VCO is controlled by a small current source, I_L which keeps the VCO running at a low frequency. I_L is kept low to reduce VCO's input-referred phase noise and power consumption. The comparator noise standard deviation is 0.3 SAR LSB and it results in a swing of ±0.9 SAR LSB at the VCO input. Comparator thermal noise, combined with SAR quantization noise and pseudorandom dither, $prbs$, results in a 4 SAR LSB swing at the VCO input. The VCO gain, k_{vco}, is set, such that the VCO can handle this swing without phase overflow.

The differential outputs from each VCO cell are latched using sense-amps (SA). Current-starved buffers are used to prevent the SA kickback noise from affecting the VCO phase. The phase encoder maps the outputs of the SAs into a binary phase value by deciding which VCO cell is in transition when the VCO phase is sampled, and the direction of transition, i.e., positive or negative. Each VCO cell is defined to be undergoing a positive transition when its positive input is less than $V_{\text{dd}}/2$ and its positive output is greater than $V_{\text{dd}}/2$. Similarly, a VCO cell is defined to be undergoing a negative

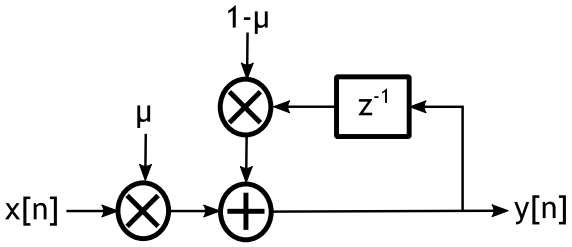


Fig. 6. IIR filter used as an averager in interstage gain extraction.

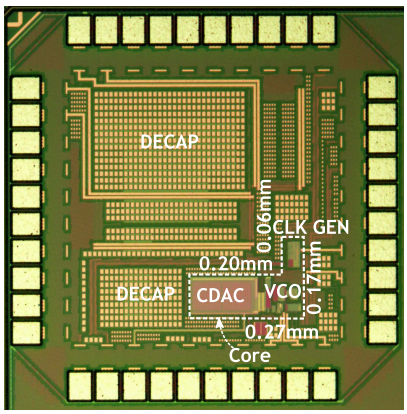


Fig. 7. Die photograph.

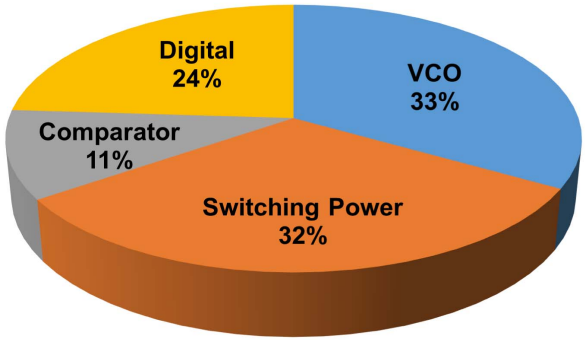


Fig. 8. CDC power breakdown.

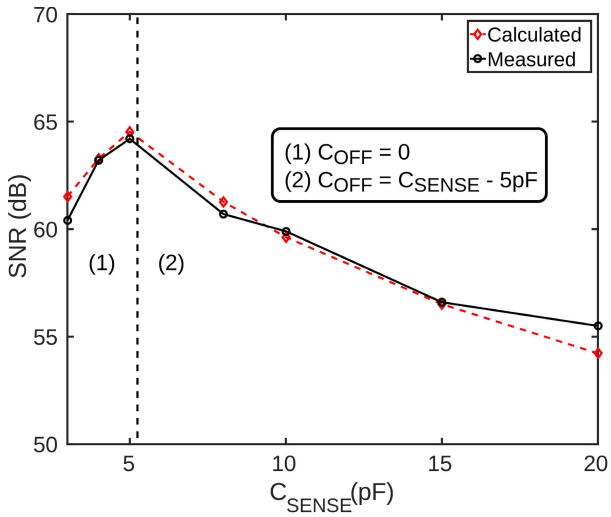


Fig. 9. Measured SNR versus C_{SENSE}.

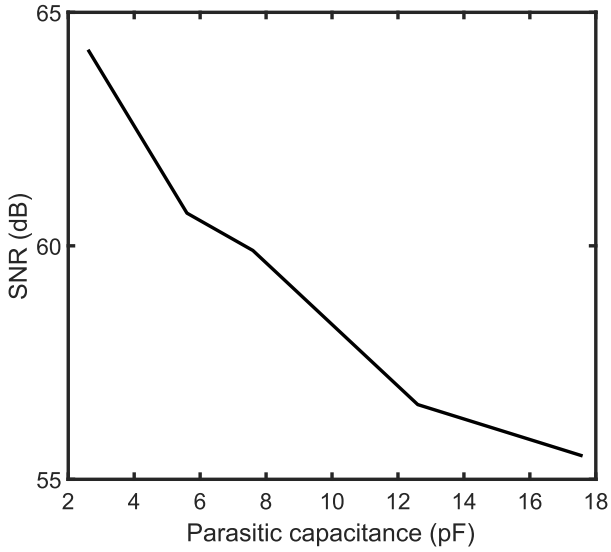


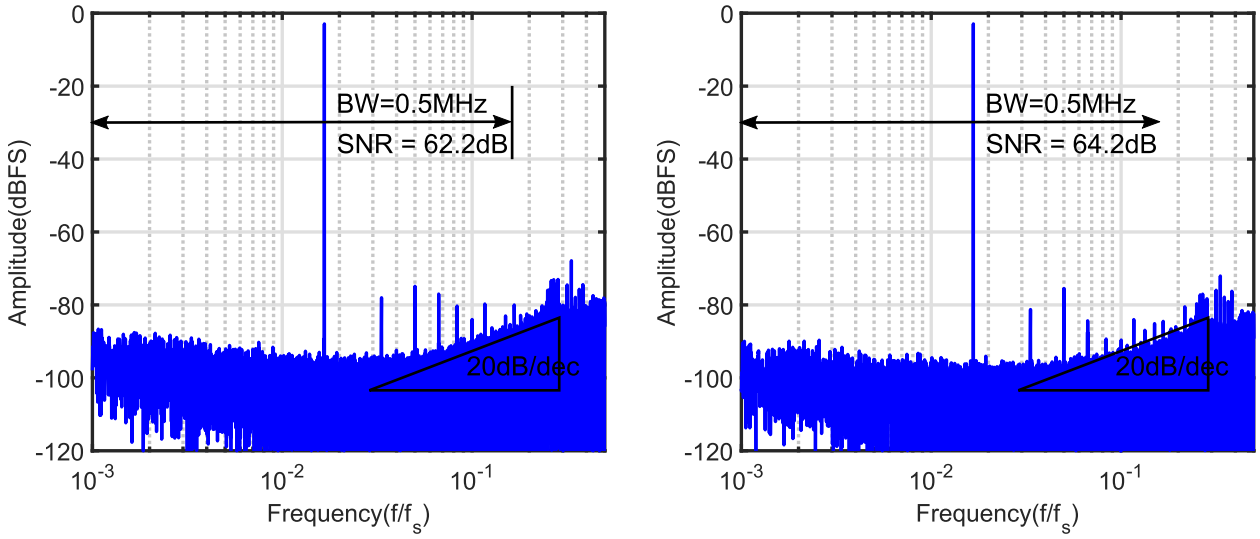
Fig. 10. Measured SNR versus parasitic capacitance (pF).

transition when its positive input is greater than $V_{\mathrm{dd}}/2$ and its positive output is less than $V_{\mathrm{dd}}/2$. This technique of phase quantization avoids nonuniform quantization, which can otherwise result in significant distortion [30]. The digitized phase is then differentiated to get the VCO output d_2.

3) Interstage Gain Extraction: The interstage gain extraction circuit consists of two averagers and a 1-to-2 DEMUX. Depending on the value of pseudorandom number generated by the PRNG, the VCO output d_2 is sent to one of the two averagers. The averagers are built using low-pass, first-order IIR filters, as shown in Fig. 6. The IIR filter output can be written as $y = \mu x/\{1-(1-\mu)z^{-1}\}$. The speed of convergence of the calibration algorithm depends on the IIR filter bandwidth μ. It can be seen from (6) that the dominant noise source is the quantization noise from the SAR stage, q_1. If the SAR resolution is increased by two times, its quantization noise power reduces by 4 and the IIR filter bandwidth can be increased by 4 resulting in four times faster calibration convergence. Thus, the 9-bit resolution of the SAR stage helps in achieving faster convergence of the calibration. This is also an important reason for choosing a 9-bit SAR over a 7- or 8-bit SAR.

III. Measurement Results

The proposed CDC is implemented in a 40-nm CMOS process. The chip photograph is shown in Fig. 7. The core circuit occupies an area of 0.033 mm^2 and the prototype area is limited by the number of pads. The prototype consumes 75 μW from 1-V supply while operating at 3 MS/s. At an OSR of 3, the equivalent measurement time is 1 μs and the total conversion energy is 75 pJ. The maximum value of C_{SENSE} that can be sensed by the CDC for $C_{\mathrm{OFF}} = 0$ is limited to 5 pF in the measurement. The capacitance sensing range can be extended beyond 5 pF by setting C_{OFF} to a nonzero value, such that it cancels the signal-independent base capacitance



(a) (b)

Fig. 11. Measured spectrum of the CDC with $M = 0$. (a) Without calibration. (b) With calibration.

in C_{SENSE}. As an example, the sensing range can be extended to $C_{\text{SENSE}} = 10$ pF by setting $C_{\text{OFF}} = 5$ pF.

Fig. 8 shows the power breakdown of the prototype for $C_{\text{SENSE}} = 5$ pF. Out of the total power consumption of 75 μW, the VCO consumes the highest power of 25 μW, which is 33% of the overall power. This power consumption is required to reduce VCO phase noise, which contributes to 40% of the CDC noise power; 32% of the CDC power is dissipated in switching of the SAR DAC and C_{SENSE}. No external reference voltages are used for the SAR DAC and sensing capacitor; instead, they are connected to the analog power supplies, which are generated using off-chip low-dropout voltage regulators. Digital logic, including SAR logic, clock generation, and VCO phase encoding, consumes 18 μW, which is 24% of the total power. The comparator consumes only 11% of the total power. The SAR+VCO architecture allows the use of a low-power comparator as its noise is canceled at the output. The proposed architecture does not use any OTA and is very scaling friendly. Thus, the power consumption of the CDC will reduce in more advanced CMOS processes. Technology scaling will also result in lower transistor delay, which will reduce VCO quantization noise.

Fig. 9 shows both theoretically calculated and measured SNR versus sensing capacitance at an OSR of 3. SNR is calculated using the formula $\text{SNR} = 20\log_{10}\left(\text{Range}/(8^{1/2})/\text{Resolution}\right)$ where capacitance resolution is obtained from the standard deviation of in-band noise. The theoretical value of standard deviation of in-band noise is calculated using the equations derived in Section II-C. For $C_{\text{OFF}} = 0$, the CDC supports an input range of 0–5 pF. Comparator offset prevented the CDC from achieving the full range of 6 pF. The capacitance sensing range is extended by using a nonzero C_{OFF}. SNR increases with C_{SENSE} till 5 pF. Beyond 5 pF, as C_{OFF} is combined with C_{SENSE}, charge sharing is greatly increased, which reduces the interstage gain and increases the noise contribution from the VCO. This leads to a decrease in SNR beyond $C_{\text{SENSE}} = 5$ pF. It should be noted here that for SNR calculations beyond $C_{\text{SENSE}} = 5$ pF, an effective full-scale capacitance range of $(C_{\text{SENSE}} - C_{\text{OFF}}) = 5$ pF is used. The theoretical values of SNR match quite well with measured values over the sweep of C_{SENSE}.

Fig. 10 shows the maximum SNR achieved by the CDC as the parasitic capacitance is varied. As expected, CDC SNR reduces as parasitic capacitance increases. The current prototype was designed to handle a parasitic capacitance of $1 \sim 3$ pF. However, the SAR stage can be easily modified to handle larger parasitic capacitances by adding an auxiliary capacitance array like in [34].

In the test mode ($M = 0$), a fixed ceramic capacitor C_{SENSE} of 5 pF is connected to the CDC and C_{OFF} is set to 0. A sine wave of 50 kHz is applied to V_{in} and the CDC output is sampled at 3 MHz. Fig. 11(a) shows the measured CDC output spectrum without any calibration. Background calibration improves the SNR by 2 dB and the corresponding output spectrum is shown in Fig. 11(b). The measured SFDR is 70.8 dB, which is limited not by the CDC chip but by nonlinearity in C_{SENSE} itself. No calibration is required for capacitor mismatches in the SAR DAC.

Fig. 12 shows the measured distribution of the VCO output after digital differentiation. The average of d_2 is 8.64 when $prbs = 1$ and 8.23 when $prbs = 0$. From this difference, we can extract $G_A^{'} = 0.41$. Fig. 13 shows the output digital code versus C_{SENSE} in the normal operating mode ($M = 1$). Fig. 14 shows SNR and figure of merit (FoM) versus OSR. The FoM is calculated as $\text{FoM} = \text{Energy}/2^{\text{resolution}}$. At low OSR, the overall noise is dominated by the first-order high-pass shaped VCO quantization noise. For every two times increase in OSR, noise power reduces by $\sqrt{8}$, which results in reduction in FoM by $\sqrt{2}$. Beyond a certain point, as OSR is further increased, thermal noise starts dominating the overall noise. For every two times increase in OSR, noise power reduces by $\sqrt{2}$, which results in increase in FoM by $\sqrt{2}$. For this

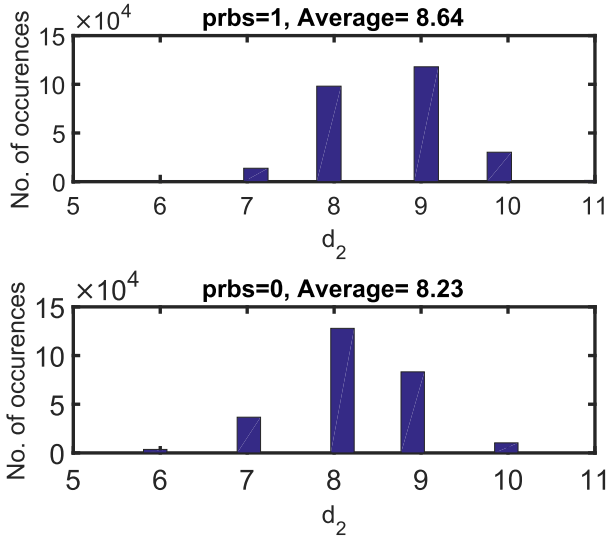


Fig. 12. Measured d_2 histogram for $prbs = 1$ and 0.

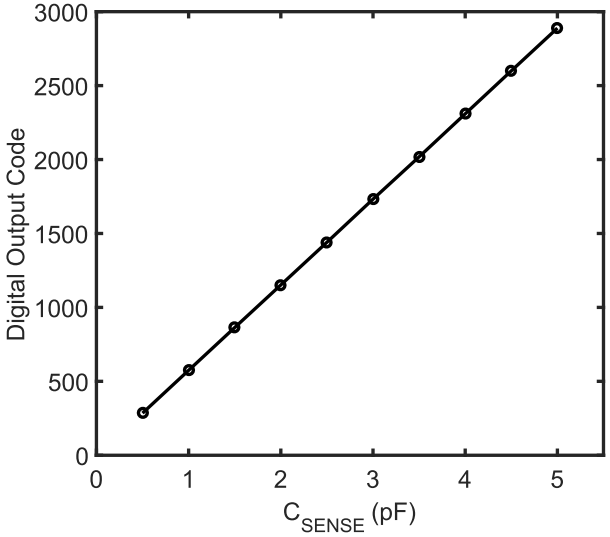


Fig. 13. Measured d_{out} versus C_{SENSE}.

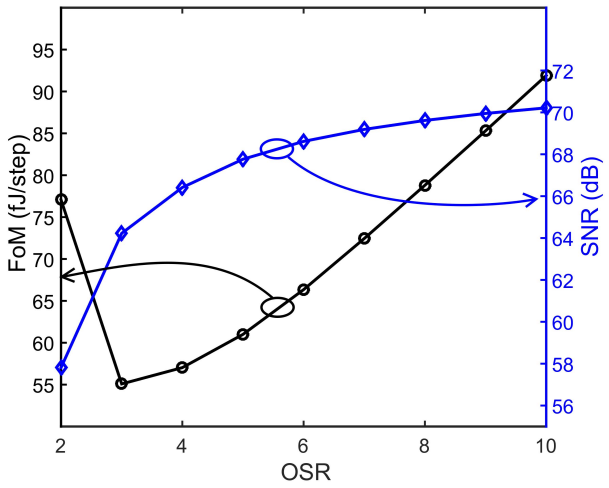
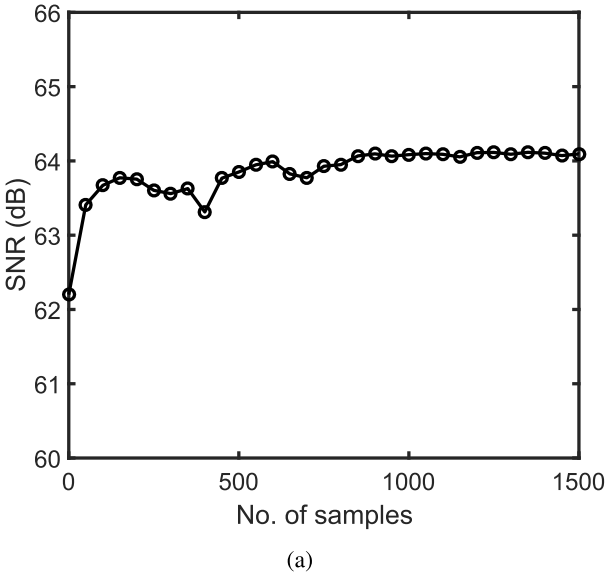


Fig. 14. FoM and SNR versus OSR.



(a)

Fig. 15. Measured calibration convergence speed.

prototype, the best FoM of 55 fJ/step is obtained at OSR of 3 with an SNR of 64.2 dB.

Fig. 15 shows the measured calibration convergence versus the number of samples. The 9-bit resolution from the SAR stage results in quick convergence and the prototype requires only 1000 samples to converge. The calibration algorithm runs in the background, while the CDC is operating in its normal mode ($M = 1$). The background calibration technique makes the proposed CDC suitable for applications which require continuous monitoring of capacitance, particularly in the domain of patient care or industrial applications. For applications in which the sensor has to work only intermittently, the proposed background calibration technique may not be suitable if PVT changes significantly between measurements. For such applications, foreground calibration of the interstage gain can be performed. By stopping the SAR stage completely and only switching the pseudorandom sequence, an estimate of the interstage gain be extracted from far fewer cycles as the only source of noise during the measurement will come from the VCO stage. The current CDC chip already has the required circuitry for the foreground calibration and only requires a switch to turn off the SAR stage.

The effectiveness of the background calibration in presence of supply voltage variation is shown in Fig. 16. As the supply voltage is varied from 0.9 to 1.1 V, the digital output code shows a maximum variation of four codes before calibration. The relative change in digital output code is calculated with respect to the digital output at 1 V. Calibration successfully removes the variation in digital output code as the supply voltage varies.

Table I compares the proposed CDC with the state-of-the-art CDCs. Combination of SAR + $\Delta\Sigma$ [19] achieves better energy efficiency than $\Delta\Sigma$-only CDCs. The SAR-CDC in [13] shows that the use of power efficient inverter-based amplifier

TABLE I
COMPARISON WITH PRIOR ART

	[2]	[20]	[4]	[13]	[19]	[27]	[26]	**This Work**
Process(nm)	180	350	160	180	180	40	130	**40**
Method	Dual-slope	ΔΣ	ΔΣ	SAR	SAR+ΔΣ	Delay Chain	Frequency	**SAR+VCO**
Input range (pF)	5.3-30.7	8.4-11.6	0.54-1.06	0-12.66	0-24	0.7-10000	6-6.3	**0-5**
Meas. time (μs)	6400	20	800	16	230	19	1000	**1**
Resolution (fF)	54.9	0.06	0.07	1.1	0.16	12.3	3.6	**1.1**
Energy (nJ)	0.704	298	8.24	0.12	7.75	0.035[3]	0.27	**0.075**[5]
SNR [1](dB)	44.2[4]	84.8	68.4	70.6	94.7	49.7[3]	29.4	**64.2**
FoM [2](fJ/conv-step)	5300[4]	21000	3800	35	175	140[3]	11000	**55**

[1] $\text{SNR} = 20\log_{10}\left(\frac{\text{Capacitance range}/2/\sqrt{2}}{\text{Capacitance resolution}}\right)$

[2] $\text{FoM} = \frac{\text{Energy}}{2^{(\text{SNR}-1.76)/6.02}}$

[3] Measured with 11.3pF

[4] Calculated with one subrange

[5] Energy consumed by off-chip voltage regulator ICs are not included

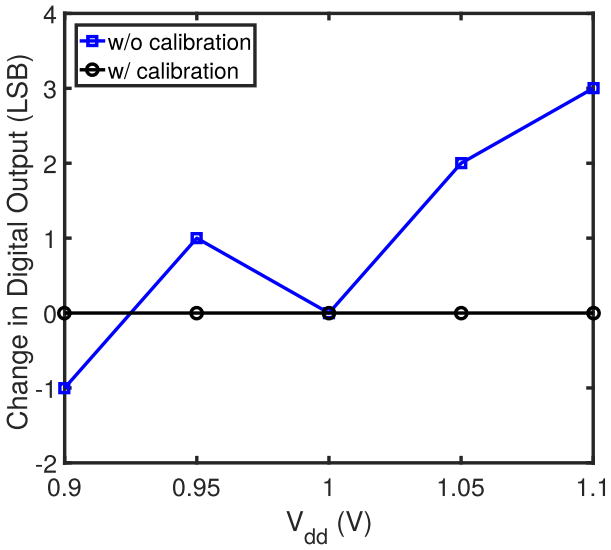


Fig. 16. Digital output code versus V_{dd} variation.

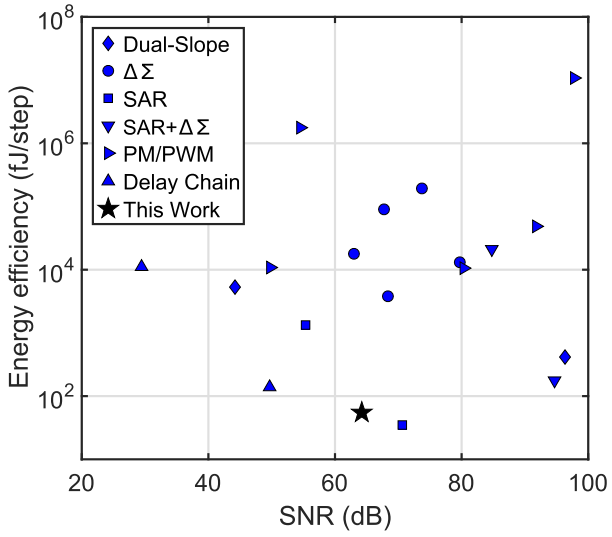


Fig. 17. Comparison of energy efficiency of different CDCs versus SNR.

can result in high energy efficiency. The proposed SAR+VCO architecture performs better than dual-slope and SAR+ ΔΣ architectures due to its highly digital nature and absence of power hungry OTAs. The proposed CDC prototype has the shortest measurement time compared with prior works, and energy of the prototype can be reduced further by trading off speed. Fig. 17 compares FoM versus SNR of the proposed architecture with different CDC architectures. It can be seen that the proposed architecture compares favorably with the state of the art and has the second highest energy efficiency after the SAR CDC in [13]. The CDC resolution can be increased by increasing the VCO resolution. The VCO resolution can be improved by lowering the sampling speed, which will increase the VCO's integration gain as well as reducing the CDC switching and digital power. As can be seen from (8), reducing sampling speed also reduces VCO's input-referred noise. However, a low sampling speed will increase the chance of VCO phase overflow. This can be addressed by using a counter to record the number of VCO phase overflows during any sampling period [32].

IV. CONCLUSION

A hybrid SAR-VCO-based ΔΣ CDC has been designed and implemented in a 40-nm CMOS process. The proposed CDC combines the merits of both SAR and ΔΣ to achieve high resolution with good energy efficiency while being highly digital in nature. A simple digital interstage gain extraction is incorporated into the CDC to track the VCO gain across PVT, while the CDC is operating in its normal mode. Measurement results show that the CDC has an SNR of 64.2 dB with an energy efficiency of 55 fJ/conversion-step.

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