A Low Frequency-Dependence, Energy-Efficient Switching Technique for Bottom-Plate Sampled SAR ADC

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Abstract— This paper shows frequency dependence of switching energy of bottom-plate sampled successive approximation register (SAR) analog-to-digital converters (ADC) and presents a technique that achieves 86% reduction in switching energy compared to the conventional SAR over a wide frequency range. The switching energy has been calculated by taking into account both the power drawn from reference as well as the power consumed by the switches themselves. The results have been verified through MATLAB and SPICE simulations.

I. INTRODUCTION

The low power consumption and highly digital nature of successive approximation register (SAR) analog-to-digital converter (ADC) makes it a very attractive option for future ADCs operating from a low supply voltage. A lot of research has been done on SAR ADCs in recent times [1]–[4]. Many of the research works focus on lowering the power of the SAR ADC to get to really low energy consumption per conversion step. For high resolution SAR ADCs, the capacitive digital-to-analog converter (DAC) can contribute a large fraction of the total ADC power. Hence, many research works aim to cut down the switching energy in the DAC. The split-capacitor technique of [5] achieves 37% saving in switching energy over the conventional switching technique. The technique in [6] combines the split-capacitor technique with an energy saving method to achieve 56% saving in switching energy. The monotonic switching scheme reported in [7] has an 81% reduction in switching energy. The V_{cm}-based switching techniques of [8], [9] can reduce the switching energy by 88% compared to a conventional SAR (for a single-ended implementation the energy savings in [9] is 93% but reduces to 88% for a differential configuration). The switching technique reported in [10] achieves 98% saving in switching energy.

The switching energy of a SAR ADC has two components: (a) energy drawn from the reference, E_{ref} and (b) energy spent in driving the DAC switches, E_{sw}. All the energy-efficient techniques reported in the literature refer only to the switching energy drawn from the voltage reference. This switching energy is frequency independent. However, E_{sw} has a strong frequency dependence, and as will be shown later, can easily dominate E_{ref} at medium-to-high sampling frequencies, specially for the energy saving switching techniques [7]–[9]. With the shrinking technology nodes, future SAR

ADCs will approach sampling rates of 100 MS/s and beyond, while still maintaining a high resolution. Hence, the frequency dependence of the switching energy cannot be ignored for the SAR ADCs of the future and energy saving techniques that can reduce both E_{ref} and E_{sw} will be of paramount importance.

An energy-efficient technique has been presented in [11] which reduces both E_{ref} and E_{sw}. The analysis presented in [11] is for top-plate sampled SAR ADCs. High linearity SAR ADCs invariably require bottom-plate sampling techniques and hence, in this work we will extend the technique of [11] to high resolution, bottom-plate sampled SAR ADCs. In order to reduce E_{ref}, the proposed technique reduces the capacitance in the DAC by 4X compared to the conventional switching technique. The proposed technique reduces E_{sw} by ensuring only one switching event per cycle, and allowing a full voltage swing of $(0, V_{ref})$ across the switches for all the comparison cycles except the last one. A full voltage swing allows the switches to have a smaller size and hence, an E_{sw} which is smaller than in the V_{cm}-based technique [8], [9] which employs reduced voltage swings of $(0, V_{cm})$ and (V_{cm}, V_{ref}). The reduction of capacitance in the proposed technique also helps lower its E_{sw} by cutting down the number of switches in the DAC. The proposed switching technique is presented and compared with the existing techniques in Section II and Section III brings up the conclusion.

II. PROPOSED SWITCHING TECHNIQUE

A. Capacitance reduction

The proposed technique for bottom-plate sampling is illustrated for a 3-bit SAR ADC in Fig. 1. The proposed technique can easily be generalized to a SAR ADC with arbitrary resolution. The analog supply voltage, V_{cc}, is used as the reference, V_{ref}. The last capacitor in the DAC is switched between (V_{cm}, V_{ref}) instead of $(0, V_{ref})$. This allows an additional comparison to be performed after the DAC has settled down, and the comparator's output can be appended to the DAC outputs to form the final digital output. It can be seen that for a 3-bit SAR, the proposed switching technique requires a total capacitance of only 4C compared to 16C capacitance in the conventional switching technique. Thus, the proposed technique achieves a 4X reduction in the DAC capacitance. It should be noted here that an accurate V_{cm} is not needed as
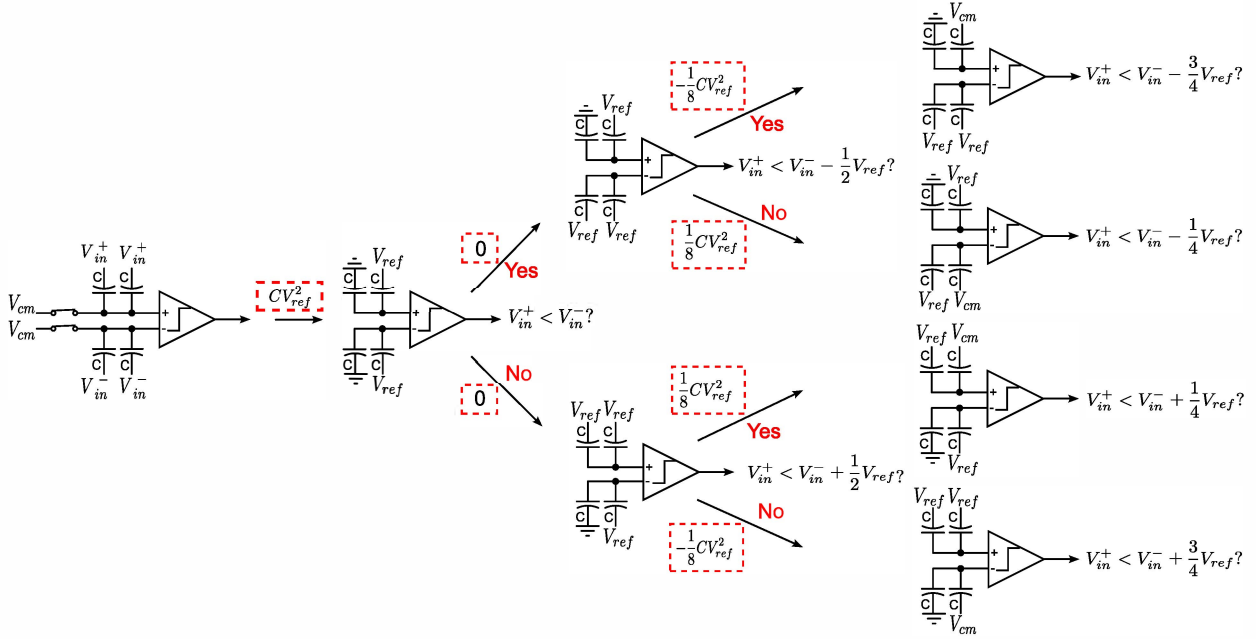
Fig. 1. Proposed switching technique illustrated for a 3-bit SAR ADC with bottom-plate sampling.

the reference level V_{cm} is used only for the last unit capacitor and any error in the value of V_{cm} does not degrade the ADC's resolution seriously. In addition, no energy is drawn from V_{cm} during the comparison cycles.

B. Zero switching energy in the second cycle

The concept of reducing the switching energy in the second cycle is introduced in Fig. 2. Fig. 2(a) indicates the simplified initial switching sequence proposed in this work, as shown in Fig. 1, while Fig. 2(b) shows the initial sequence from [7]. Applying charge conservation on Fig. 2(a), $V_y = V_x + V_{ref}/2$.
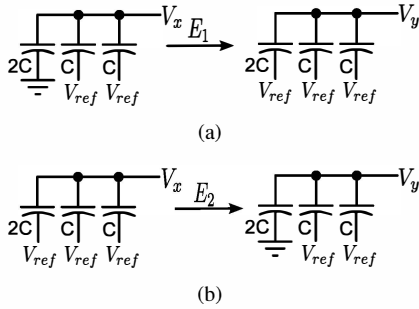

(a)

(b)

Fig. 2. Illustration of the idea behind energy saving.

The switching energy E_1 can be calculated as $E_1 = V_{ref} \cdot 2C\{V_{ref} + 2(V_x - V_y)\} = 0$. Thus, no energy is drawn from V_{ref}. However, if the sequence is reversed as is done in [7] (see Fig. 2(b)), applying charge conservation gives $V_y = V_x - V_{ref}/2$. Hence, the switching energy E_2 is given by $E_2 = V_{ref} \cdot 2C\{V_x - V_y\} = CV_{ref}^2 \neq 0$. Applying this concept also ensures that $E_{ref} = 0$ during the second cycle, as can be seen from Fig. 1. The 3-bit ADC is a special case of the proposed switching technique in that its average E_{ref} is zero. However, for SAR ADCs with resolution greater than 3 bits, the average E_{ref} is non-zero with the proposed switching technique.

C. Reduction of E_{sw}

The discussion on switching energy reduction has so far focused on reducing the frequency independent component E_{ref}. A considerable amount of energy is also spent on driving the switches in the DAC. The variation of the total switching energy, $E_{tot} = E_{ref} + E_{sw}$, with frequency for two different CMOS processes, 180nm and 65nm, and unit capacitor values, 2fF and 20fF, is shown in Fig. 3. The frequency dependence of the switching energy can be clearly seen in Fig. 3. The focus on this sub-section will be to show how E_{sw} affects the total switching energy, and how the proposed switching technique can achieve reduction in E_{sw}.

To study the effect of E_{sw}, a first-order, simplified model of the DAC was developed. Let the unit capacitor in the DAC be denoted by C_0, the resistance of the unit NMOS switch be R_0, and its gate capacitance be C_{r0}. It is assumed that the unit PMOS switch will be sized to have the same resistance as the unit NMOS switch. Let the i-th capacitor in the DAC be denoted by C_i. For an N-bit DAC, let us assume that the switches are all sized to have the same RC time constant, i.e, $R_i C_i = R_j C_j \ \forall i, j \in [0, N], \ i \neq j$, where R_i is the resistance of the i-th switch in the DAC. An estimate of R_i can be obtained from [11]

$$R_i = min\{0.8T_{\phi 1}/(\beta C_i), 0.8T_{DAC}/(\beta C_i)\} \quad (1)$$

where $T_{\phi 1}$ is the time over which the input is sampled, T_{DAC} is the DAC settling time given by $((T_s - T_{\phi 1})/N - T_{comp} - T_{logic})$, and β is the number of time constants required for the DAC to settle to N-bit accuracy. The sampling frequency is denoted by $1/T_s$.

The limits placed on R_i come from two different time constants: 1) the sampling time constant, $T_{\phi 1}/\beta$ and, 2) the DAC time constant, T_{DAC}/β. T_{comp} is the time required by the
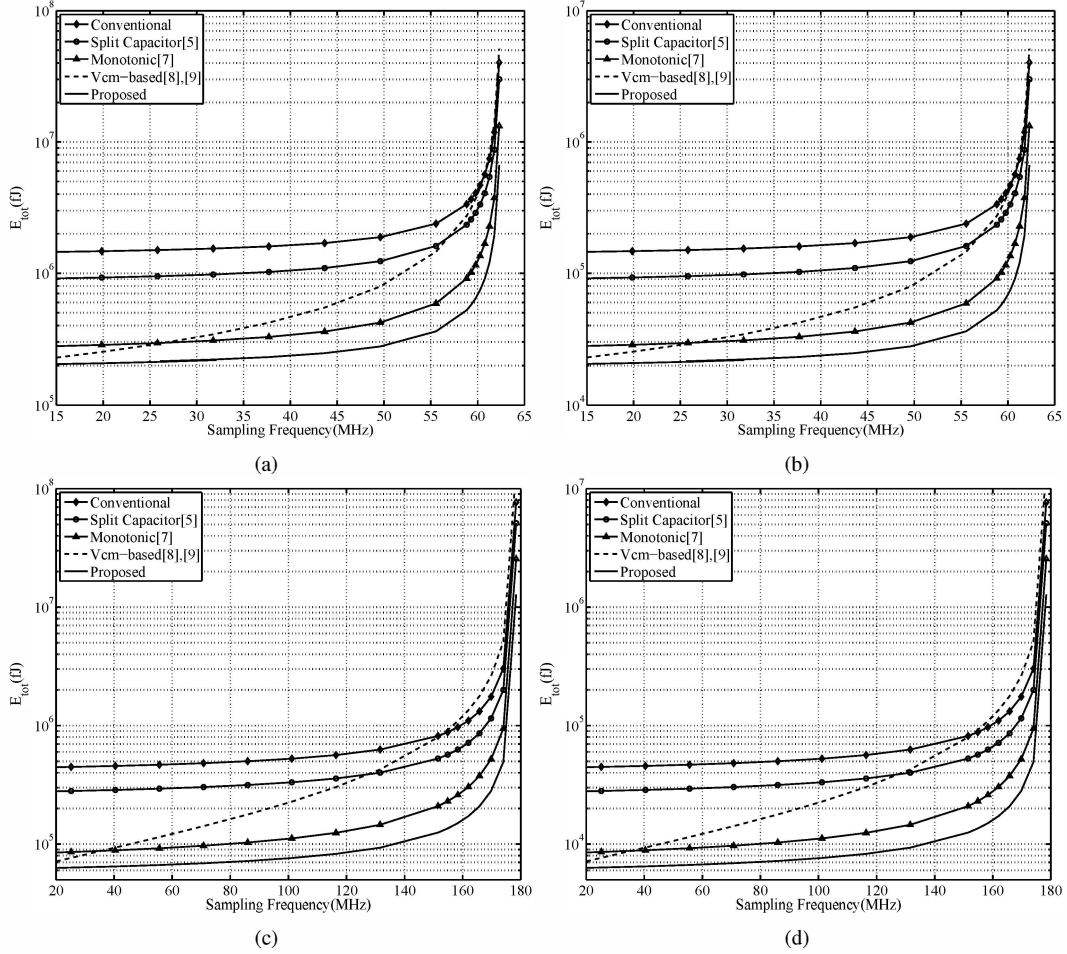
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Fig. 3. E_{tot} vs sampling frequency for {180nm, V_{ref}= 1.8V} (a) C_0 = 20fF, (b) C_0 = 2fF, and {65nm, V_{ref}=1V} (c) C_0 = 20fF, (d) C_0 = 2fF for a 14-bit bottom-plate sampling SAR ADC.

TABLE I

COMPARISON OF SWITCHING TECHNIQUES FOR $C_0 = 20fF$ AT 180NM FOR A 14-BIT BOTTOM-PLATE SAMPLING SAR ADC.

switching method	E_{ref}(pJ)	Low Freq.(15 MHz)		Medium Freq.(40 MHz)		High Freq.(60 MHz)	
		E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM
conventional	1415.50	34.80	88.50	184.60	97.70	1942.40	204.90
split-capacitor [5]	884.60	26.10	55.60	138.40	62.40	1456.60	142.90
monotonic [7]	265.42	11.59	16.91	61.53	19.96	647.46	55.72
V_{cm}-based [8], [9]	176.90	45.80	13.60	243.30	25.60	2560.40	167.10
this work	199.10	5.81	12.50	30.77	14.03	323.73	31.91

TABLE II

COMPARISON OF SWITCHING TECHNIQUES FOR $C_0 = 2fF$ AT 65NM FOR A 14-BIT BOTTOM-PLATE SAMPLING SAR ADC.

switching method	E_{ref}(pJ)	Low Freq.(20 MHz)		Medium Freq.(100 MHz)		High Freq.(160 MHz)	
		E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM
conventional	43.68	1.13	2.73	8.91	3.21	44.45	5.38
split-capacitor [5]	27.30	0.76	1.71	5.94	2.03	29.63	3.47
monotonic [7]	8.19	0.38	0.52	2.97	0.68	14.82	1.40
V_{cm}-based [8], [9]	5.46	2.19	0.47	17.35	1.39	86.62	5.62
this work	6.14	0.19	0.39	1.49	0.46	7.41	0.83

comparator to resolve its inputs, and T_{logic} is the delay of the digital control logic. The factor of 0.8 in (1) is used to account for the parasitic gate capacitance of the switches. As can be seen from (1), $T_{s,min}$ is given by $(N (T_{comp} + T_{logic}) + T_{\phi 1})$.

Once R_i is calculated, C_{ri} can be extracted from SPICE

simulation and is usually of the form α/R_i where α depends on the process parameters. At low sampling frequencies (high T_s), E_{sw} increases slowly due to the lower limit imposed on C_{ri} by the minimum capacitance available in the process. At high sampling frequencies (low T_s), E_{sw} is proportional

TABLE III

COMPARISON OF SWITCHING TECHNIQUES FOR $C_{tot} = 32.7pF$ AT 65NM FOR A 14-BIT BOTTOM-PLATE SAMPLING SAR ADC.

switching method	E_{ref}(pJ)	Low Freq.(20 MHz)		Medium Freq.(100 MHz)		High Freq.(160 MHz)	
		E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM	E_{sw}(pJ)	FoM
conventional	43.68	1.13	2.73	8.91	3.21	44.45	5.38
split-capacitor [5]	27.30	0.76	1.71	5.94	2.03	29.63	3.47
monotonic [7]	16.38	0.81	1.05	6.32	1.39	27.05	2.65
V_{cm}-based [8], [9]	10.92	5.02	0.97	39.38	3.07	168.55	10.95
this work	24.57	0.81	1.55	6.32	1.88	27.05	3.15

to $\alpha V_{cc}^2/T_{DAC}$. Since, T_{DAC} starts approaching zero at low T_s values, E_{sw} increases very quickly at high sampling frequencies [11].

As can be seen from Fig. 3, the conventional method and the split-capacitor scheme show a lesser increase in E_{tot} with frequency than the other schemes. This is because the conventional and the split-capacitor scheme have a much larger E_{ref} than the other switching techniques. The V_{cm}-based switching technique shows a much sharper increase in E_{tot} with frequency, compared to the other switching techniques. This is because it uses much wider switches as the gate-to-source voltage swing is only half of that of the other switching techniques which have a gate-to-source voltage swing of $(0, V_{ref})$. In addition, the V_{cm}-based technique has two transitions every switching cycle, compared to the monotonic switching technique [7] and the proposed technique which have only one transition every switching cycle. The proposed technique has the lowest E_{sw} among the existing switching techniques. The proposed technique has a 85.8% energy savings compared to the conventional method at 15 MHz and 84.4% energy savings at 60 MHz for the 180nm process node, and 20fF unit capacitor. Compared to the proposed technique, the monotonic switching technique and the V_{cm}-based technique have energy savings of 80.9% and 84.6% respectively at 15 MHz and 72.8% and 18.4% respectively at 60 MHz sampling frequency. As can be seen from Fig. 3, both E_{ref} and E_{sw} scale well with process node and capacitance.

To provide a better comparison of the different switching techniques across the process node and capacitance values, a figure-of-merit (FoM) has been defined as $FoM \equiv (E_{ref} + E_{sw})/2^N$. The results of the comparisons are shown in Tables I-II for a 14-bit bottom-plate sampled SAR ADC. As can be seen from Table II, the proposed technique has a very low FoM value of 0.83 fJ/conv. even at a high frequency of 160 MHz. Another useful comparison of the different switching techniques can be performed for the same C_{tot}, which will compare the different techniques for the same total kT/C noise. This comparison is important specially for high resolution ADCs whose noise maybe limited by kT/C noise. The comparison table for the different switching techniques with the same C_{tot} of 32.7 pF is shown in Table III. It can be seen that the V_{cm}-based technique has a much higher energy consumption than the conventional switching technique at high frequencies, while the monotonic switching technique of [7] has the best performance of all the switching techniques over the entire frequency range. The proposed technique has

a slightly higher E_{tot} than the monotonic technique due to larger E_{ref} of the proposed technique. However for the monotonic switching technique, the variation of the input common-mode voltage of the comparator is twice that of the proposed technique and the input common-mode voltage of the comparator eventually drifts to '0' for the monotonic switching technique [11]. The input common-mode voltage variation gives rise to dynamic offset for the comparator, and thus, the monotonic switching technique requires a more complicated comparator design than the proposed switching technique.

III. CONCLUSION

A high energy-efficiency, low frequency-dependence switching technique for bottom-plate sampling SAR ADCs has been presented in this paper. The frequency dependence of the existing switching techniques has been studied and compared with the proposed technique. It has been shown that the proposed switching technique maintains a better energy-efficiency than the existing switching techniques over the entire frequency range of operation.

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