Comparator Common-Mode Variation Effects Analysis and its Application in SAR ADCs

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***Abstract*—The effects of comparator input common-mode voltage V_{cm} are analyzed in this paper. The analysis clearly shows a trade-off in the choice of V_{cm} in terms of offset, noise, power and speed. Based on the analysis, an energy efficient SAR ADC switching technique is proposed with less V_{cm} variation and better linearity compared with the widely used monotonic switching technique. Both the simulation results and prototype measured results match with the analysis.**

I. Introduction

The strong-arm latch comparator is widely used in SAR ADCs. It serves as an interface between the analog and digital domains and is a key component in defining the resolution and speed of SAR ADCs. In strong-arm latch comparator, the gain during pre-amplification phase depends on its input common-mode voltage V_{cm} [1], [2]. This pre-amplification gain affects comparator input-referred offset, noise and resolve time. Thus, V_{cm} is a significant design factor for strong-arm latch comparator.

Another key component in SAR ADCs is capacitive DAC. The conventional DAC switching technique based on trial and error is not power efficient. Several low-power DAC switching techniques have been developed, among them the monotonic switching technique of [3] has attracted increasing attention. It achieves 81% reduction in DAC reference power, requires only one switching event every comparison cycle and reduces the total number of unit capacitors by a factor of 2. While its comparator input common-mode voltage V_{cm} has a large variation, which leads to reduced linearity. Thus, it is necessary to come up with an energy-efficient switching technique with less V_{cm} variation.

In this paper, the V_{cm} variation effects are analyzed. Based on the analysis, a prototype ADC with bidirectional single-side (BSS) switching technique is proposed that maintains all the aforementioned merits of the monotonic switching technique and solves the large V_{cm} variation issue. The BSS switching technique was originally reported in 2014 ESSCIRC conference [4]. However, due to the page limitation, the key design factor of V_{cm} variation reduction is not discussed thoroughly. The simulation shows a 7dB SNDR improvement is achieved with the BSS technique compared to the monotonic switching technique. In addition, the input referred noise of the prototype ADC is measured to further demonstrate the V_{cm} variation effects analysis.

II. Common-Mode Variation Effects Analysis

Fig. 1 and Fig. 2 show the strong-arm latch comparator and its typical transient behavior with a 1mV input differential

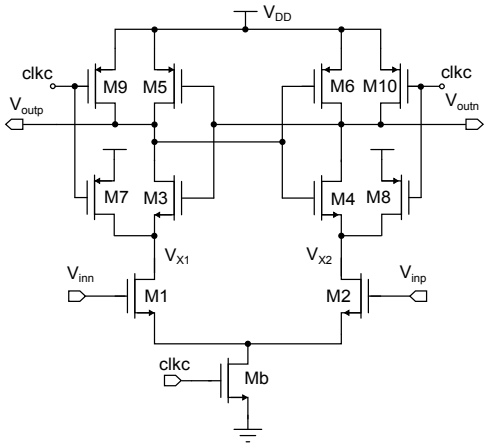

Fig. 1. Schematic of a strong-arm latch comparator.

voltage. When $clkc$ is low, the comparator is in reset with both $V_{X1,2}$ and $V_{outp,n}$ pulled to V_{DD}. When $clkc$ is high, the comparator is in evaluation mode. Here its operation can be divided into two phases, the pre-amplification phase and the latch regeneration phase as shown in Fig. 3, with the turn-on of the PMOS cross-coupled pair separating two phases. During the pre-amplification phase, the PMOS cross-coupled pair is in cut-off and the comparator works as a dynamic integrator. From differential-mode point of view, the comparator input voltage induces a differential drain current, which is integrated on the output capacitive load C_O and produces a differential output voltage V_{out} that grows linearly with time. From the common-mode point of view, $V_{X1,2}$ decrease after $clkc$ goes high. Once they reach $V_{DD} - V_{Tn3,4}$, M3 and M4 are turned on and $V_{outp,n}$ start to decrease. When $V_{outp,n}$ decrease to $V_{DD} - V_{Tp5,6}$, the PMOS crossed coupled pair is turned on and the comparator enters the latch phase. Since the PMOS crossed coupled pair is in positive feedback and provides exponentially growing gain, the PMOS pair dominates the behavior of the comparator in the latch phase, while other transistors can be considered to the first order as a current source before V_{out} grows very large that cuts off a transistor in the PMOS pair or the current source.

A critical parameter that links the two phases is the pre-amplifier gain G, defined as the differential voltage gain of the comparator at the end of the pre-amplification phase. It affects the comparator offset and noise. We can model the input referred offset of the pre-amplification phase as $V_{os,preamp}$, whose main contributor is $V_{Tn1,2}$ mismatch in the input pair. For the latch phase, we can model its offset referred to the

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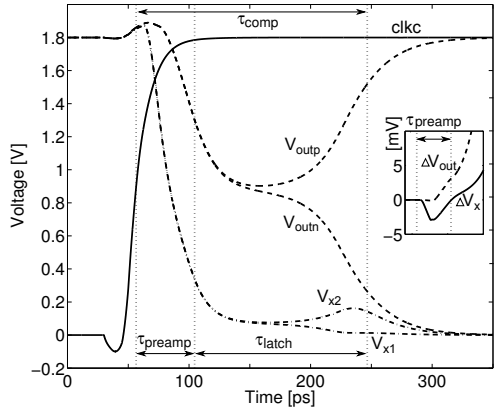

Fig. 2. Transient behavior of a strong-arm latch comparator.

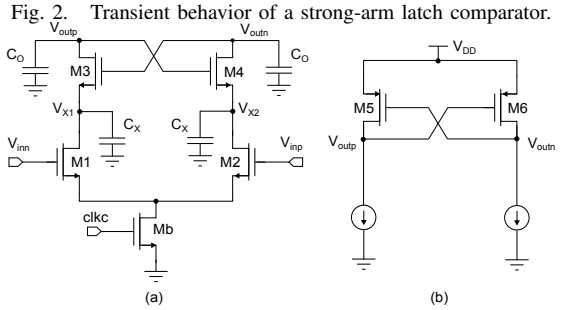

Fig. 3. Schematic for (a) pre-amplification phase (b) latch regeneration phase.

output nodes at the beginning of the latch generation phase as $V_{os,latch}$, whose main contributor is $V_{Tp5,6}$ mismatch in the PMOS cross coupled pair. As a result, the root-mean-square (rms) input referred offset of the entire comparator, V_{os}, is given by:

$$\sigma_{os} = \sqrt{\sigma^2_{os,preamp} + \frac{\sigma^2_{os,latch}}{G^2}} \tag{1}$$

Similarly, we have the expression for the comparator noise:

$$\sigma_n = \sqrt{\sigma^2_{n,preamp} + \frac{\sigma^2_{n,latch}}{G^2}} \tag{2}$$

From (1) and (2), we can see that the offset and noise depend strongly on G, and a large G is preferred as it attenuates the contribution from the latch phase. The value of G can be estimated to the first order in the following way. We first calculate the time duration τ_{preamp} of the pre-amplification phase by examining the common-mode voltage change. At the beginning of the pre-amplification phase, the common-mode voltages at $V_{outp,n}$ and $V_{X1,2}$ are both V_{DD}. By the end of the pre-amplification phase, the common-mode voltage at $V_{outp,n}$ and $V_{X1,2}$ are approximately $V_{DD} - V_{Tp5,6}$ and $V_{DD} - V_{Tp5,6} - V_{Tn3,4}$, respectively. For simplicity, assuming that the common-mode drain current of the comparator input pair I_D is unchanged during the integration, we have:

$$\tau_{preamp} \approx \frac{C_O V_{Tp5,6} + C_X(V_{Tp5,6} + V_{Tn3,4})}{I_D} \tag{3}$$

where C_X and C_O are the total capacitive load at $V_{X1,2}$ and $V_{outp,n}$ (see Fig. 3). Similarly, assuming g_m of the input pair is unchanged during the integration, the total amount of differential charge ΔQ produced by the input pair with small input voltage ΔV_{in} is:

$$\Delta Q = \Delta I \cdot \tau_{preamp} \approx g_m \Delta V_{in} \cdot \tau_{preamp} \tag{4}$$

By the end of the integration phase, the majority of the differential charge ΔQ is at the output nodes $V_{outp,n}$ (the amount of differential charge at $V_{X1,2}$ is very small as shown in Fig. 2), and thus, we can derive G:

$$\begin{aligned} G &\approx \frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{\Delta Q / C_O}{\Delta V_{in}} \\ &\approx \frac{g_m}{I_D}\left\{V_{Tp5,6} + \frac{C_X}{C_O}(V_{Tp5,6} + V_{Tp3,4})\right\} \end{aligned} \tag{5}$$

Since the comparator input common-mode V_{cm} determines g_m/I_D of the input transistor, it has a strong influence on G. To increase G and reduce offset and noise, we prefer a small V_{cm}. To verify the analysis above, SPICE simulation is performed in 0.18-μm CMOS process with $V_{DD} = 1.8V$. G is extracted by examining the voltage difference at $V_{outp,n}$ when the output common-mode drops to $V_{DD} - V_{Tp5,6}$. Fig. 4(a) shows that G depends strongly on V_{cm}. It decreases from 12.6 at $V_{cm} = 0.6V$ to 0.6 at $V_{cm} = 1.8V$. Also, g_m/I_D proportionally decreases as V_{cm} increases. These results match (5). σ_{os} and σ_n are extracted from Monte Carlo and transient noise simulations, respectively. Fig. 4(b) shows that they both increase with V_{cm} due to the reduction in G. Fig. 4(c) plots their square as a function of $1/G^2$. The close linear fitting with a fitting coefficient $r > 0.99$ clearly validates the models of (1) and (2).

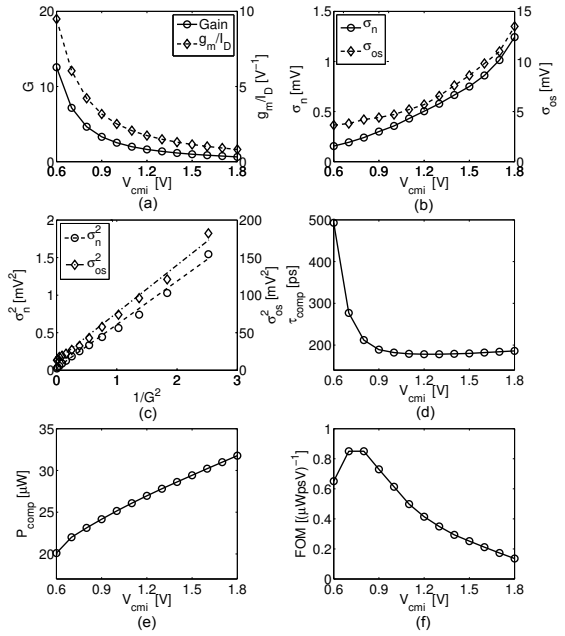

Fig. 4. Simulated comparator performance: (a) G and g_m/I_D; (b) noise and offset; (c) linear fitting for noise and offset with $1/G^2$; (d) resolve time; (e) power and (f) FOM_{comp}.

V_{cm} also strongly affects the comparator resolve time τ_{comp} defined here as the time it takes for the comparator output

differential voltage to reach $0.7V_{DD}$. Fig. 4(d) shows τ_{comp} as a function of V_{cm} for a fixed 1mV input. τ_{comp} decreases as V_{cm} increases, which can be explained by (3) as a larger I_D shortens the pre-amplification phase τ_{comp}. An interesting observation is that the minimum τ_{comp} is not obtained at $V_{cm} = V_{DD}$. The reason is that if V_{cm} is too large, the time duration of the latch regeneration phase is longer due to the reduction in G [1]. In addition, the comparator power P_{comp} depends mildly on V_{cm}, as shown in Fig. 4(e). The reason is that a large V_{cm} leads to increased short circuit current.

Overall, a small V_{cm} is preferred for small offset, low noise, and low power, but it leads to slow speed. This represents a trade-off in the choice of V_{cm}. To provide a holistic evaluation of the comparator performance, we can define a comparator figure-of-merit $FOM_{comp} = \frac{1}{\sigma_n \times \tau_{comp} \times P_{comp}}$, which is plotted in Fig. 4(f). Its optimum is at around $V_{cm} = 0.8V$, which is more than 6 times larger than that at $V_{cm} = 1.8V$.

III. Power Efficient Switching Technique With Less Common-Mode Variation

As discussed in Section I, the key limitation for monotonic switching is that its V_{cm} monotonically decreases from $V_{DD}/2$ to ground. Note that there exists a complementary version for the original monotonic switching by connecting all DAC capacitors initially to ground. This way, V_{cm} monotonically increases from $V_{DD}/2$ to V_{DD}, which permits the use of the strong-arm latch comparator with an NMOS input pair shown in Fig. 1. However, as shown in Fig. 4, having $V_{cm} = V_{DD}$ results in large comparator offset and noise. For the proposed BSS technique, V_{cm} first increases, then decreases, and finally converges to $V_{DD}/2$ for an 11-bit SAR ADC as reported in Fig. 2 in [4]. Compared to monotonic switching, the amount of V_{cm} variation is reduced by a factor of 2. Furthermore, because V_{cm} converges to $V_{DD}/2$, the comparator noise and offset are significantly reduced. To compare the ADC performance with monotonic up switching and the proposed switching technique, a behavioral model for an 11-bit SAR ADC is built in MATLAB using the strong-arm latch comparator parameters extracted via SPICE simulation (see Fig. 4). For simplicity, other components in the SAR ADC are assumed to be ideal.

In conventional switching technique, V_{cm} is fixed, and thus, the comparator offset is a constant and does not affect the ADC linearity. By contrast, in both monotonic switching and BSS schemes, V_{cm} changes every comparison cycle, which leads to varying comparator offset (see Fig. 4) and degrades the ADC linearity. To examine the influence of offset variation, we first perform 1000-time Monte Carlo simulations for the 11-bit ADC with V_{cm} dependent offset variation but no noise. The SNDR histograms are shown in Fig. 5. Since V_{cm} in monotonic switching changes from $V_{DD}/2$ to V_{DD}, it leads to large varying offset, which significantly degrades the ADC SNDR. For the proposed switching scheme, since its V_{cm} variation is only $V_{DD}/4$ and it starts from $V_{DD}/2$ and ends at $V_{DD}/2$, its SNDR is much higher. However, because V_{cm} still undergoes large changes in the first several MSB comparisons, there are still appreciable SNDR degradations in cases where the comparator offsets are large and have considerable variations.

To solve this problem, a small redundant capacitor can be added after the 6th MSB capacitor (see Fig. 4 in [4]), which corrects the errors due to offset variations in the first 6 comparisons. For the comparisons afterwards, the change in V_{cm} is within $V_{DD}/128$, and thus, the comparator offset variation is negligible and does not degrade SNDR. Fig. 8 shows the simulation results with redundancy added. The performance for the ADC with the proposed switching scheme is fully restored. The ADC performance for the monotonic switching is also improved, but there is still about 20% probability for having less than 67 dB SNDR. Although adding redundancy can effectively address the offset variation problem, it can't solve the SNDR loss due to increased comparator noise. For monotonic up switching, because V_{cm} converges to V_{DD}, its comparator noise is much larger than that for the proposed technique especially for the last several noisy sensitive LSB comparisons. This leads to SNDR degradation. Fig. 9 shows the simulated SNDR histograms with offset, noise, and redundancy. The average SNDR for monotonic switching is 60 dB, while that for the proposed switching is 67 dB. Note that this 7 dB SNDR improvement comes without any penalty in the comparator power.

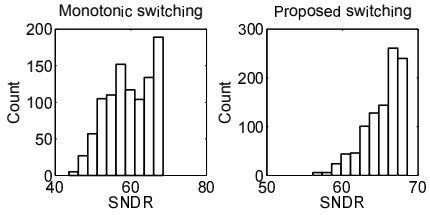

Fig. 5. Simulated SNDR with comparator offset variation.

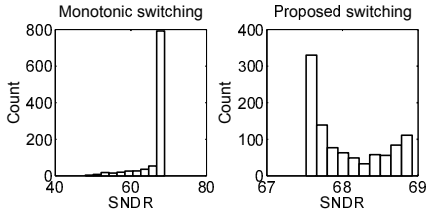

Fig. 6. Simulated SNDR with both comparator offset variation and a redundant capacitor after the 6th MSB capacitor.

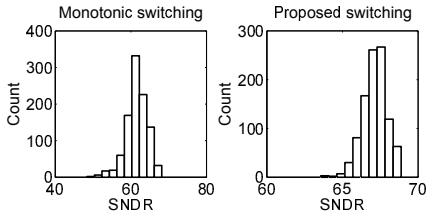

Fig. 7. Simulated SNDR with comparator offset variation, noise and a redundant capacitor after the 6th MSB capacitor.

The proposed switching technique can be generalized to allow the comparator common-mode voltage to converge to any desired voltage. It provides designers the freedom to

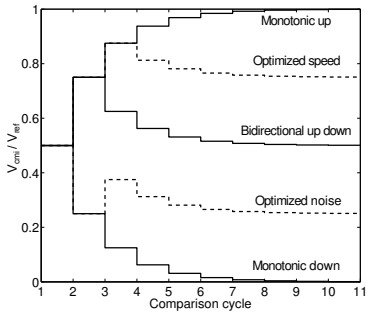

Fig. 8. V_{cm} variation for different switching techniques.

optimize the comparator for different design specifications. For example, for low-speed high-resolution applications, it is desirable to reduce V_{cm} to minimize the comparator noise (see Fig. 4). To this end, we can initialize the DAC array in such a way that the second MSB capacitor is connected to ground while all other capacitors are connected to V_{ref}. As a result, during DAC switching, V_{cm} first goes down, then goes up, and finally goes down to $0.25 \times 1.8 = 0.45V$ (see Fig. 8). In this configuration, the simulated comparator input referred noise is only 100 μV, which is 70% less than that for $V_{cm} = 0.9V$. For high-speed medium-resolution applications, it is preferred to place V_{cm} at higher voltages (see Fig. 4). This can be achieved by letting V_{cm} go up during the first two MSB comparisons and then go down, as shown in Fig. 8. This way, V_{cm} converges to $0.75V_{DD}$, leading to a 10ps shorter comparator resolve time. Note that the speed improvement by adjusting V_{cm} can be more significant in advanced technology nodes with low power supply voltage.

IV. Prototype Design And Measurements

The prototype SAR ADC with proposed BBS is fabricated in 0.18-μm CMOS process [see Fig. 9]. Its measured SNDR and SFDR are 63.4dB and 76.6dB, respectively, at the sampling rate of 1 MS/s under $V_{DD} = 1V$. The measured total ADC power is 24 μW with a figure-of-merit of 19.9 fJ/conversion-step [4].

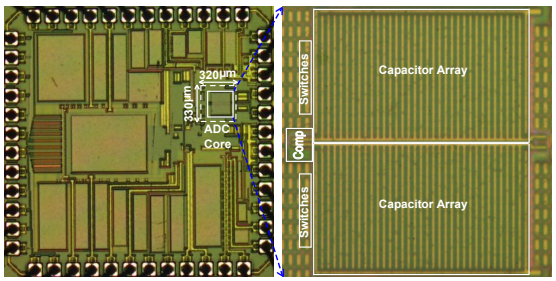

Fig. 9. Die micrograph and zoomed view.

Comparator noise plays a key role in the resolving accuracy in SAR ADCs [5]. To verify the analysis in Sec. II, we vary the comparator input common-mode voltage V_{cm} and measure ADC output D_{out} at $V_{in} = 0$V. The measured probability densities for D_{out} at $V_{DD} = 1$V with $V_{cm} = 0.4$V and $V_{cm} = 0.9$V are shown in Fig. 10 together with the fitted normal distributions. When $V_{cm} = 0.4$V, D_{out} is centered at code 1051 and spread over only 3 bins with a standard deviation of 0.36 LSB. By contrast, when V_{cm} is increased to 0.9V, D_{out} is centered at code 1049 and spread over 8 bins with a standard deviation of 0.70 LSB. The shift of D_{out} center indicates the comparator offset variation, which is due to V_{cm} induced preamplifier gain change as explained in Sec. II and Eq. (1). The increase in the ADC noise, which is dominated by the comparator, is also the result of preamplifier gain reduction as explained in Sec. II and Eq. (2). Fig. 11 shows the measured ADC rms noise with different V_{cm}. It clearly shows that a larger V_{cm} leads to increased comparator noise, which matches well with the analysis in Sec. II.

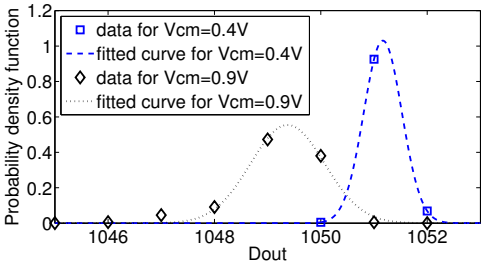

Fig. 10. Measured D_{out} distribution with $V_{cm} = 0.4V$ and $V_{cm} = 0.9V$.

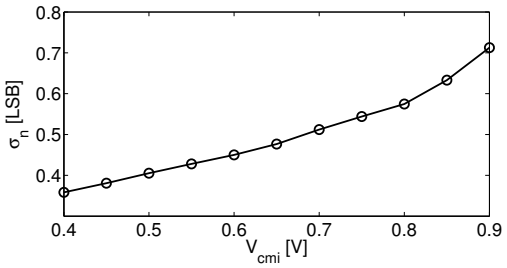

Fig. 11. Measured D_{out} standard deviation with different V_{cm} at $V_{in} = 0$V.

V. Conclusion

The effects of comparator input common-mode variation are analyzed. Based on the analysis, an energy efficient bidirectional single-side switching technique is proposed to reduce the common-mode voltage variation. The proposed switching technique is suitable for applications that require both low power and high resolution.

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