An Enhanced ISI Shaping Technique for Multi-bit $\Delta\Sigma$ DACs

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Abstract— This paper presents an improved ISI shaping technique for multi-bit $\Delta\Sigma$ DACs. Compared to the prior ISI shaping method (Lars Risbo et al, JSSC, 2011) that monitors only the up $(0 \rightarrow 1)$ transitions, the proposed technique makes use of both the up and down $(1 \rightarrow 0)$ transitions with negligible hardware cost. It provides a finer control of the transition activity, thereby improving the ISI shaping effect. In addition, due to the tight coupling between the ISI and mismatch shaping loops, the proposed technique also improves the mismatch shaping result. Simulation results show that it can reduce ISI induced distortions by 10 dB compared to the prior ISI shaping technique and 50 dB compared to DWA.

I. INTRODUCTION

Compared to a binary $\Delta\Sigma$ DAC, a multi-bit $\Delta\Sigma$ DAC has a higher signal-to-noise ratio (SNR) at a given over-sampling ratio (OSR) due to a more aggressive noise transfer function. The drawback for a multi-bit DAC is the nonlinearity caused by the element mismatches. The mismatch errors can be randomized by dynamic element matching (DEM) [1] or first-order shaped using data weighted averaging (DWA) [2], [3]. Recently, more advanced techniques have been developed that can achieve higher order mismatch shaping [4]-[7]. In addition to static mismatch, another major source of distortion in a continuoustime (CT) multi-bit $\Delta\Sigma$ DAC is the dynamic error due to inter-symbol interference (ISI). This ISI error represents the non-idealities during the transition of DAC elements and can be caused by clock skew, asymmetric on-and-off switching, and capacitive memory effects. Unlike the static mismatch error, the ISI error can be present even for a binary DAC. One common analog approach to mitigate the ISI error is to use the return-to-zero (RZ) arrangement [8]. However, this leads to a two times reduction in signal amplitude for the same power and also produces large discontinuities in the output waveform. Furthermore, it is much more sensitive to clock jitter compared to a non-return-to-zero (NRZ) DAC.

The ideal situation is to control the DAC element selection pattern in such a way that the ISI error is shaped, similar to the shaping of static mismatch errors by DEM techniques [1]–[7]. Unfortunately, many of the DEM techniques mentioned above exacerbate the ISI error. The reason is that the magnitude of the ISI error is proportional to the DAC switching activity. Most DEM techniques increase the DAC element transition rate in order to scramble more effectively the DAC element selection pattern techniques [1]–[7]. In particular, the popular DWA technique has the highest transition activity, as it always tries to turn off previously selected elements and turn on new elements that have not been selected before. This results in the largest ISI error for DWA technique.

To mitigate the ISI error, the key is to maintain the number of DAC element transitions at a constant value independent of the signal. This key observation was first used in the modified mismatch shaping (MMS) technique [9] to maintain a constant total number of up $(0 \rightarrow 1)$ and down $(1 \rightarrow 0)$ transitions of all DAC elements during every clock cycle. This turned a large portion of the ISI error into an offset. Despite its clear advancement from prior arts, the MMS technique has several limitations: 1) it assumes that the up and down transitions produce the same ISI error, which is rarely true in reality; 2) it cannot shape the ISI errors, leading to a relatively limited performance enhancement. The recent development of the ISI shaping technique of [10] represents a major step forward. It proves that the ISI error of each 1-bit unit DAC element can be written as a linear term plus a nonlinear term that only shows up during the up transition. It proposes to use a digital $\Delta\Sigma$ loop to keep the long-term average of the up transition rate constant, thus achieving high-pass shaping of the ISI error.

This paper presents an enhanced ISI shaping technique. It builds upon the technique of [10], but produces better ISI shaping results. The technique of [10] monitors only the up transition rate. By contrast, the proposed technique monitors both the up and down transition activities, and tries to keep their summation constant. In fact, the only difference is that the proposed technique uses an XOR gate to replace the AND gate used in [10]. As shown later, this simple modification can lead to as much as 10 dB reduction in distortion and inband noise caused by ISI. Note that the hardware complexity for the proposed technique is identical to that of [10]. This paper is organized as follows. Section II shows the ISI error model. Section III presents the proposed ISI shaping technique. Section IV discusses the simulation results. Finally, the conclusion is brought up in Section V.

II. ISI ERROR MODEL

Let us first examine the ISI error for a unit element DAC. Fig. 1(a) shows a 1-bit digital input s[n]. The ideal and actual DAC outputs are shown in Fig. 1(b) and (c). The ISI error pulse is plotted in Fig. 1(d). For an oversampling low-pass $\Delta\Sigma$ DAC, what is of interest is the in-band low-frequency component, which corresponds to the integral of the ISI error pulses. Depending on the transitions, they are denoted as e_{00} , e_{01} , e_{10} , and e_{11} , respectively. As shown in Fig. 1(e), we can derive an ISI error sequence $\{ISI[n]\}$, where ISI[n] represents the ISI error between s[n-1] and s[n]. It is easy to show that:

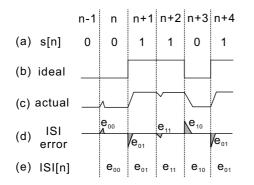


Fig. 1. (a) 1-bit digital sequence, (b) ideal DAC output, (c) DAC output with ISI error, (d) ISI error, and (e) ISI sequence.

$$ISI[n] = e_{00} + s[n-1](e_{10} - e_{00}) + s[n](e_{01} - e_{00}) + s[n-1]s[n](e_{11} + e_{00} - e_{01} - e_{10})$$
(1)

The first three terms of (1) represent a 2-tap FIR filtering of s[n], and thus, is linear. The last term is proportional to $\Gamma_{11}[n] \equiv s[n-1]s[n]$, and thus, is nonlinear. One straightforward idea to suppress the nonlinearity is to make $e_{11} + e_{00} - e_{01} - e_{10} = 0$. However, this is hard to achieve in reality due to parasitics and process variations. Another simple idea to remove the ISI induced distortion is to guarantee that there is no concatenated '1's in s[n], so that $\Gamma_{11}[n]$ always equals to '0'. This is essentially equivalent to the RZ scheme of [8], whose drawback has been stated in Section I.

Note that (1) can also be written in the following format:

$$ISI[n] = e_{00} + s[n-1](e_{10} - e_{00}) + s[n](e_{11} - e_{10}) -\Gamma_{01}[n](e_{00} + e_{11} - e_{01} - e_{10})$$
(2)

where $\Gamma_{01}[n] \equiv (1 - s[n - 1])s[n]$. (2) shows that the ISI nonlinearity can also be associated with only the up transition sequence $\Gamma_{01}[n]$. In fact, it is trivial to derive that the ISI nonlinearity can be solely associated with any one of the 4 transition sequences, $\Gamma_{11}[n]$, $\Gamma_{01}[n]$, $\Gamma_{10}[n] \equiv (1 - s[n - 1])s[n]$, or $\Gamma_{00}[n] \equiv (1 - s[n - 1])(1 - s[n])$.

The key idea of [10] is that if the long term average of $\Gamma_{01}[n]$ is kept as a constant independent of the signal s[n], the ISI induced nonlinearity can be significantly suppressed.

So far, the discussion has been focused on a single 1-bit unit DAC element. For a multi-bit DAC with M elements, the total ISI error sequence is given by:

$$ISI[n] = \sum_{i=1}^{M} w_i ISI_i[n]$$
(3)

where $ISI_i[n]$ denotes the ISI sequence and w_i represents the weight of the *i*-th unit DAC element. If every individual ISI sequence $ISI_i[n]$ is shaped, the total ISI error must be shaped regardless of weight differences. As an example, let us consider a 32-element DAC. The normalized spectra of $\Gamma_{01}[n]$ and s[n] for the 32-element DAC are shown in Fig. 2. It is clear that DWA provides good mismatch shaping, but has the highest transition rate and the largest ISI induced distortion [see Fig. 2(b)]. By contrast, although thermometer coding cannot shape the mismatch error, it has much smaller ISI induced distortion compared to DWA [see Fig. 2(a)]. The ISI shaping technique achieves both ISI shaping and mismatch shaping [see Fig. 2(c)]. Even though its mismatch noise floor is higher than that for DWA, the 2nd-order distortion due to ISI error is more than 30 dB lower, clearly demonstrating its effectiveness.

III. ENHANCED ISI SHAPING BY COUNTING BOTH UP AND DOWN TRANSITIONS

The ISI shaping technique of [10] counts only the up transition, and ignores the down transition. This is sufficient for the shaping of the ISI error, but is not optimum. This paper proposes an enhanced ISI shaping technique that is shown in Fig. 3. It uses an XOR gate to count both up and down transitions and keeps the total transition rate to be a constant c. The digital gain G adjusts the relative strength between the upper mismatch shaping loop and the lower ISI shaping loop. Its use will be explained later.

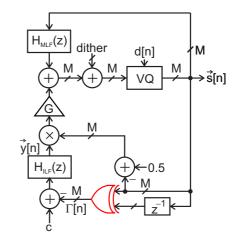
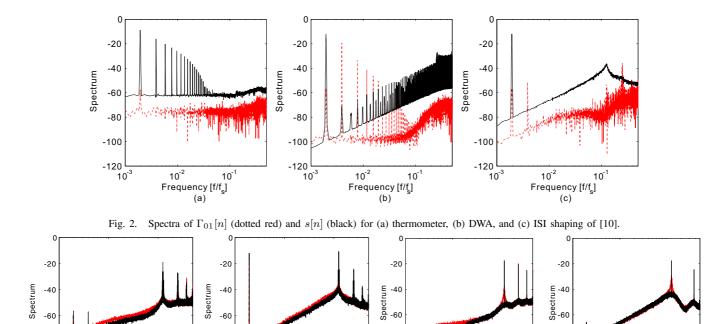
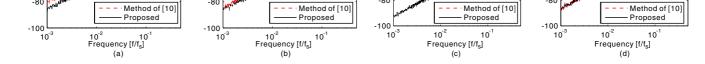


Fig. 3. Architecture for the proposed ISI shaping technique.

The rationale behind using both transitions is that they are closely linked to each other. There must be a down transition between two adjacent up transitions, and vice versa. Thus, a down transition can be viewed as an intermediate step before the next up transition, and used as a marker for a half up transition. This way, the resolution in the counting of the transition rate is doubled, leading to a better ISI shaping result. In fact, as shown later, it can also result in a better mismatch shaping due to the coupling between the two loops. Since the total up transition rate $\Gamma[n]$ has to be equal to the down transition rate, and $\Gamma_{01}[n] + \Gamma_{10}[n] = c$, it implies that $\Gamma_{01}[n] = \Gamma_{10}[n] = c/2$. This proves that the shaping of the total transition rate guarantees the shaping of individual up or down transition sequence and the ISI error.





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Comparison between spectra of (a) $\Gamma_{01}[n]$ and (b) s[n] for a large input at -3 dBFS; and (c) $\Gamma_{01}[n]$ and (d) s[n] for a small input at -60 dBFS. Fig. 4.

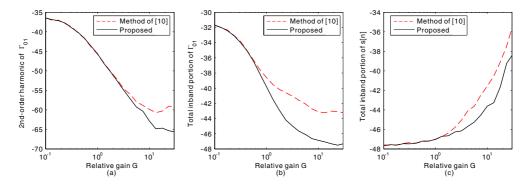


Fig. 5. Simulation results as a function of the relative gain.

IV. BEHAVIORAL SIMULATION RESULTS IN MATLAB

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A. 1st-order ISI and Mismatch Shaping

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For 1st-order ISI shaping and mismatch shaping, both the filters $H_{MLF}(z)$ and $H_{ILF}(z)$ are chosen to be $z^{-1}/(1-z^{-1})$. The simulated spectra for $\Gamma_{01}[n]$ and s[n] are shown in Fig. 4(a) and (b) respectively, for a 32-element $\Delta\Sigma$ DAC with a -3 dBFS input signal and G = 2. As expected, the ISI shaping spectrum using the proposed technique is 4 dB lower than that of [10]. Note that the mismatch shaping spectrum for the proposed technique is also 1 dB lower. Since the ISI loop has a higher resolution, it leads to a smaller swing at the output of $H_{ILF}(z)$, which results in less perturbation to the mismatch shaping loop and a better mismatch shaping result. Fig. 4(c) and (d) show the simulated result for the same DAC with a -60 dBFS input signal which show the difference in ISI shaping more clearly. At low frequency, the spectrum of $\Gamma_{01}[n]$ for the proposed technique is more than 20 dB lower than that of [10].

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Since the ISI shaping and mismatch shaping loops are coupled, it is meaningful to study the impact of the relative strength of the two loops on the shaping result by varying G. The result is shown in Fig. 5. It shows that as the ISI loop strength increases with G, both the 2nd-order distortion and total in-band component of $\Gamma_{01}[n]$ decrease [see Fig. 5(a) and (b)], leading to an improved ISI shaping result. However, the drawback is that the mismatch shaping result is worsened due to an increase in the total in-band component of s[n] [see Fig. 5(c)]. Thus, there is a clear trade-off between the ISI shaping effect and the mismatch shaping effect.

Note that the proposed technique always shows a better

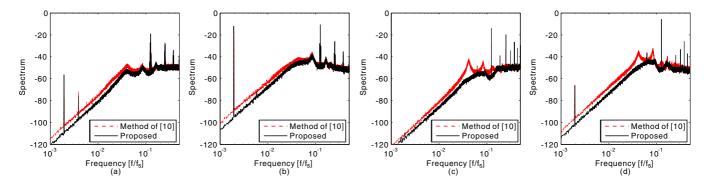


Fig. 6. Comparison between spectra of (a) $\Gamma_{01}[n]$ and (b) s[n] for a large input at -3 dBFS and, (c) $\Gamma_{01}[n]$ and (d) s[n] for a small input at -60 dBFS.

performance compared to that of [10], but the advantage becomes clearer at larger G. This is easy to understand. When G is small, the mismatch shaping loop dominates the overall loop behavior. Since both techniques use the same mismatch shaping loop, there is very small difference between them. By contrast, when G is large, the ISI shaping loop dominates over the mismatch shaping loop, and thus, there is a big difference in performance. At large G, the proposed technique can lower the ISI induced 2nd-order distortion by as much as 5 dB, which is significant especially given almost no additional hardware cost for the proposed technique.

B. 2nd-order ISI and Mismatch Shaping

The proposed technique can also provide 2nd-order ISI and mismatch shaping by using 2nd-order integrators in $H_{MLF}(z)$ and $H_{ILF}(z)$. Fig. 6(a) and (b) show the simulation results for the same $\Delta\Sigma$ DAC with a -3 dBFS input, G = 4, and $H_{MLF}(z) = H_{ILF}(z) = z^{-1}/(1-z^{-1})^2 +$ $4z^{-1}/(1-z^{-1})$. The 2nd-order shaping characteristic of 40 dB/dec is clearly seen. The proposed technique shows a 4 dB lower ISI-induced 2nd-order distortion and noise floor [see Fig. 6(a)] and 5 dB better mismatch shaping [see Fig. 6(b)] than [10]. Fig. 6(c) and (d) show the simulation result with a -60 dBFS input. Again, the proposed technique shows better performance in both ISI and mismatch shaping results than [10].

Fig. 7 shows the simulated DAC output spectra with G = 4. The ISI error and the mismatch error are assumed to be 0.3% and 1%, respectively. The THD for thermometer coding is -66 dB due to mismatch. When DWA is used, the THD does not improve; instead, it is worsened to -62 dB due to the substantial increase of the ISI error. The ISI shaping technique of [10] significantly improves the THD to -106 dB. The proposed technique shows the best THD of -111 dB, which clearly shows the advantage of the proposed technique.

V. CONCLUSION

This paper has presented an enhanced ISI shaping technique for high-precision $\Delta\Sigma$ DACs. It can significantly suppress the ISI induced distortions. As a pure digital technique, it is compatible with CMOS scaling, and can greatly lower the design complexity and precision requirements on the analog circuit and the clock distribution.

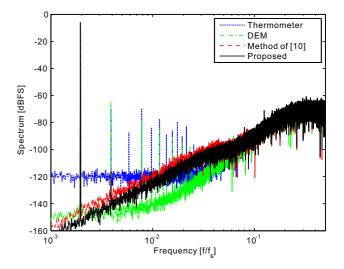


Fig. 7. DAC output spectrum.

REFERENCES

- R. J. Van De Plassche, "Dynamic element matching for high accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. sc-11, no. 6, pp. 795–800, Dec. 1976.
- [2] H. S. Jackson, "Circuit and method for cancelling nonlinearity error associated with component value mismatches in a data converter," U.S. Patent 5,221,926, Jun. 22, 1993.
- [3] R. T. Baird and T. S. Fiez, "Linearity enhancement of multi-bit ΣΔ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circ. Sys. II*, vol. 42, no. 12, pp. 753–762, Dec. 1995.
 [4] R. Schreier and B. Zhang, "Noise-shaped multibit D/A convertor em-
- [4] R. Schreier and B. Zhang, "Noise-shaped multibit D/A convertor employing unit elements," *Elec. Lett.*, vol. 31, no. 20, pp. 1712–1713, Sep. 1995.
- [5] R. K. Henderson and O. J. A. P. Nys, "Dynamic element matching techniques with arbitrary noise shaping functions," *Proc. IEEE International Symposium of Circuits and Systems*, May 1996, pp. 293–296.
- [6] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters", *IEEE Trans. Circ. and Sys. II*, vol. 44, pp. 808–817, Nov. 1997.
- [7] N. Sun, "High-order mismatch shaping in multi-bit $\Delta\Sigma$ DAC," *IEEE Trans. Circ. Sys. II*, vol. 58, no. 6, pp. 346–350, Jun. 2011.
- [8] K. Nguyen et al., "A 113 dB SNR oversampling Sigma-Delta DAC for CD/DVD application," *IEEE Trans. Consumer Electron*, vol. 44, no. 3, pp. 1019–1023, June 1998.
- [9] T. Shui et al., "Mismatch shaping for a current-mode multi-bit deltasigma DAC," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 331–338, Mar 1999.
- [10] L. Risbo et al., "Digital approaches to ISI-mitigation in high-resolution oversampled multi-level D/A converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2892–2903, Dec. 2011.
- [11] J. De Maeyer, P. Rombouts, and L. Weyten, "Addressing static and dynamic errors in unit element multibit DACs," *Elec. Lett.*, vol. 39, pp. 1038–1039, Jul. 2003.