Fractional-*N* PLL with multi-element fractional divider for noise reduction

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A novel technique to suppress quantisation noise in a ΔΣ fractional-*N* phase-locked loop (PLL) using a fine-resolution multi-element fractional divider is presented. The proposed technique suppresses noise uniformly over the entire frequency range. It is mostly digital and is applicable for both analogue and digital PLLs. The proposed technique with an eight-element fractional divider can suppress the quantisation noise by 18 dB compared with a conventional fractional-*N* PLL.

Introduction: Unlike integer-N phase-locked loops (PLLs), fractional-*N* PLLs allow synthesis of frequencies that are a fraction of the reference. Thus, it allows a higher reference frequency and a wider PLL bandwidth, which leads to faster settling time and stronger suppression of voltage controlled oscillator (VCO) noise. However, fractional-*N* PLL have an additional noise source in the form of quantisation error from ΔΣ modulator used to generate the fractional division ratio. For example, to implement a division ratio of 10.6, a conventional fractional-N PLL switches between integer division ratios of 10 and 11. It relies on the loop filter to suppress the quantisation noise. However, for a wide-band PLL, this quantisation noise can easily dominate the PLL phase noise [1] and cause large spurs.

There have been several techniques to address this issue. An analogue approach is to inject current into the charge pump to cancel out the quantisation noise. However, it requires a high-resolution DAC along with accurate gain and offset calibration techniques [2]. A multi-phase ring VCO can also be used to cancel the quantisation noise [3], but it requires complicated phase realignment technique. Another approach is to use a finite impulse response (FIR) filter at the ΔΣ modulator output [1]. Its merit is that it is mostly digital, but it is effective only at high frequencies. For a wide-band PLL, a large number of FIR filter taps are required to adequately suppress the quantisation noise.

This Letter presents a simple and mostly digital technique that significantly reduces the quantisation noise at all frequencies. Compared with the FIR filtering technique of [1], the proposed technique achieves a significant improvement in performance while incurring only a small increase in hardware complexity.

Proposed technique: The core idea of the proposed technique is to reduce the quantisation noise by increasing the ΔΣ modulator resolution. Again taking the division ratio of 10.6 as an example, if we can implement finer division ratios, such as 10.5 and 10.625, then we can just switch between these two division ratios. This way, our effective quantisation step is 1/8, and thus, the quantisation noise is 18 dB smaller than that of a conventional fractional-*N* PLL.

Now, the key question is how to implement an *instantaneous fractional* divider in hardware. Only one divider is not adequate as it can only count integer cycles, but we can arrange multiple of them running in parallel. For example, to implement the division ratio of 10.625, we can arrange 8 dividers, and choose 5 of them with the modulus of 11 and the remaining 3 of them with the modulus of 10. By combining these dividers' outputs, we effectively build a divider with a division ratio of 10.625. To get other fractional division ratios (e.g. 10.5), we can simply change the number of dividers with modulus 10 or 11. In a more general sense, to implement a division ratio of $N+k/M$, where N, k, and M are integers, we can arrange in total M dividers, and have k of them with modulus of $N+1$ and $M-k$ of them with modulus of N.

The circuit architecture implementing the proposed technique is shown in Fig. 1. As mentioned earlier, the proposed fractional divider consists of eight conventional multi-modulus dividers. They are controlled by the ΔΣ modulator to realise fractional division ratios. A key difference from a conventional fractional-*N* PLL is that the quantisation steps of the ΔΣ modulator are not integer value (e.g. 0 and 1) but fractional values (e.g. 1/8, 2/8,…, and 7/8) in the proposed technique. The decrease in the quantisation step size is the key to the noise reduction. In order to combine the outputs of the multi-element divider array, the phase-frequency detector (PFD) and the charge pump are also split into eight identical slices. This way, the eight divider outputs are effectively summed up in the charge domain. Note that each slice of the charge pump consumes only 1/8 of the original charge pump current, so that the total charge pump current remains the same as in the conventional fractional-*N* PLL. As a result, the PLL loop behaviour is unchanged.

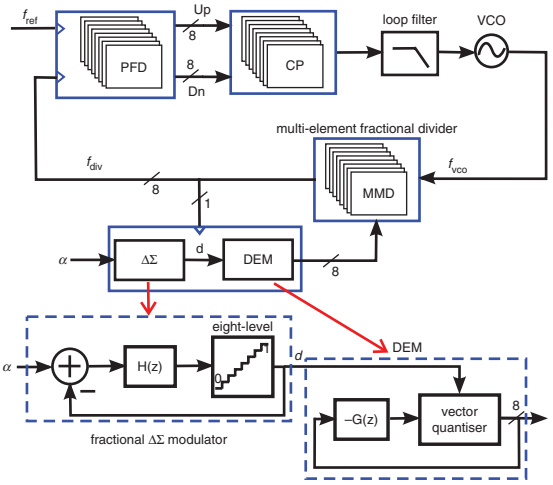

Fig. 1 *Architecture of proposed technique with an eight-element fractional divider*

To ensure that the PLL is locked, each divider slice has to maintain an average division ratio of $N+\alpha$, where N is integer part and α is the fractional part. This is done by inserting a dynamic element matching (DEM) block after the ΔΣ modulator. The DEM block scrambles the divider selection to ensure that average of the division ratio for each divider is identical. Note that the DEM also brings a key benefit in that the mismatch error among each charge-pump slice is greatly suppressed. This is similar to a multi-bit DAC where DEM can address the DAC element mismatch. A popular way to implement the DEM is to use a barrel shifter to high-pass shape the mismatch errors to the first order or to use a vector quantiser to shape the mismatch errors to higher orders [4].

Fig. 2 compares the phase noise for a classic fractional-*N* PLL, a PLL with an eight-tap FIR filter [1], and the proposed technique with an eight-element fractional divider, using a linear phase-domain PLL model. The fractional-*N* PLL is designed to have a third-order loop filter, a closed-loop bandwidth of 1 MHz, and a reference frequency of 20 MHz. It can be seen from Fig. 2 that the FIR filter only suppresses the quantisation noise beyond 1 MHz. By contrast, the proposed technique suppresses the quantisation noise by 18 dB over the entire frequency range and substantially outperforms the FIR filtering technique of [1].

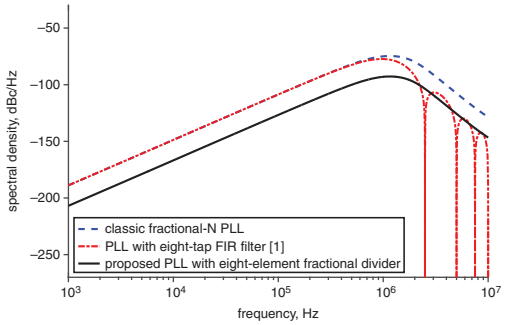

Fig. 2 *Fractional-N PLL phase noise with different techniques*

Another important advantage of the proposed technique is that the ripple in the VCO control voltage is much smaller than that in a conventional fractional-*N* PLL. This is because the quantisation error has been greatly reduced. This can greatly relax the linearity requirement for the charge pump and the VCO, leading to significantly reduced quantisation noise folding effect and spur.

The hardware cost for the proposed technique is the fine-resolution quantiser in the ΔΣ modulator, the DEM block, and multiple copies of the divider and PFD. The increased hardware is *entirely digital* and entails very low cost in terms of design effort as well as area and

power especially for designs in advanced technology. Compared with the FIR-filtering technique of [1], the only changes in hardware are the DEM block and the quantiser.

Simulation results: To verify the proposed technique, a type-II, third-order ΔΣ fractional-*N* PLL is implemented in Simulink. The reference frequency is 20 MHz and the PLL bandwidth is 1 MHz. A third-order ΔΣ modulator was used to generate a division ratio of 10.57. For simplicity, quantisation noise from the ΔΣ modulator is the only source of noise in the simulations. The VCO frequency is down-converted to 20 MHz and the output spectra for different techniques are plotted in Fig. 3. As can be seen from Fig. 3*a*, the conventional fractional-*N* PLL has large quantisation noise and appreciable spur. The FIR filtering technique can suppress the quantisation noise but only at high frequencies [see Fig. 3*b*]. By contrast, the proposed technique with eight-element divider suppresses noise across all frequencies by 18 dB, which matches the analysis using linear model (see Fig. 2). To further validate the proposed technique in the presence of device mismatches, a 3σ mismatch of 15% is added to the charge pump slices. The simulation result of Fig. 3*d* shows no noticeable degradation, which is enabled by the DEM block. The simulated root mean square jitters for the conventional fractional-*N* PLL, the FIR filtering technique, our proposed technique with and without mismatches, are 188, 126, 25, and 23 ps, respectively. This again shows that our proposed technique can reduce jitter by eight times. Note that the phase noise and jitter can be further reduced by increasing the number of slices and the fractional divider resolution. The trade-off is hardware complexity.

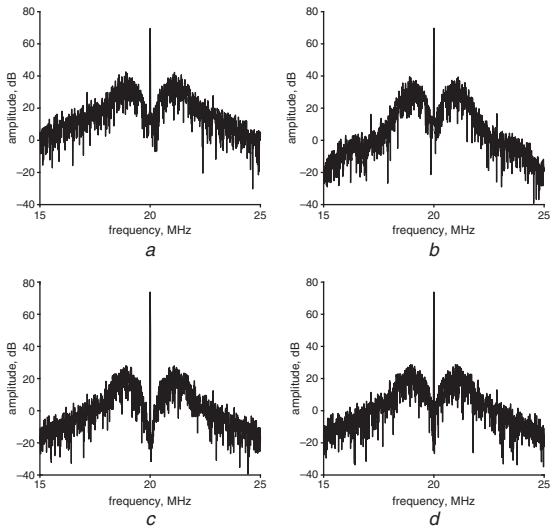

Fig. 3 *VCO output spectrum for*

a Conventional fractional-*N* PLL
b PLL with eight-tap FIR filtering [1]
c Proposed technique with eight-element fractional divider
d Proposed technique with 3σ mismatch of 15%

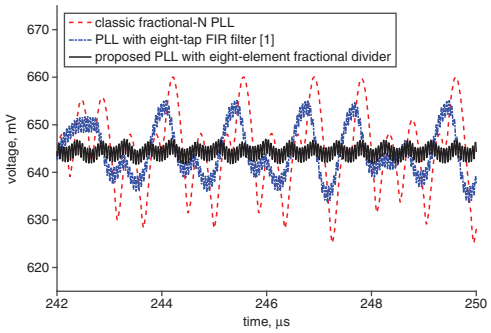

Fig. 4 *VCO control voltage transient at lock*

Fig. 4 shows the VCO control voltage at lock for three different cases: the conventional fractional-*N* PLL, the FIR filtering technique, and our proposed technique. As expected, the ripple of the proposed technique is only 1/8 of the conventional PLL, and is also significantly smaller than that of the FIR filtering technique.

Conclusion: A mostly digital technique has been presented to suppress ΔΣ quantisation noise in a wide-band fractional-*N* PLLs. It is based on the use of a fine-resolution *fractional divider*. The proposed technique has a low hardware cost due to its mostly digital nature especially in advanced CMOS processes. It can be applied to both analogue and digital fractional-*N* PLLs.

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One or more of the Figures in this Letter are available in colour online.

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