A 55fJ/conv-step Hybrid SAR-VCO $\Delta\Sigma$ Capacitance-to-Digital Converter in 40nm CMOS

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***Abstract*— A highly digital, two-stage capacitance-to-digital converter (CDC) is presented in this work. The CDC works by sampling a reference voltage on the sensing capacitor and then quantizing the charge stored in it by a 9-bit SAR ADC. The residue is fed to a ring VCO and quantized in time domain. The outputs from the two stages are combined to produce a quantized output with first-order noise shaping. A digital background calibration technique is used to track the VCO's gain across PVT. A prototype CDC in 40nm CMOS process achieves 64.2 dB SNR and an FoM of 55fJ/conversion-step while operating from a 1V supply and using a sampling frequency of 3MHz.**

I. Introduction

Capacitive sensors can measure a variety of physical quantities, such as pressure [1], position, proximity [2] and humidity [3]. They are widely used in biomedical sensing applications [4], [5] and wireless sensor nodes. These applications require high resolution and low-energy capacitance-to-digital converters (CDCs). Most CDCs work by sampling a reference voltage on the sensing capacitor and then using a high resolution analog-to-digital converter (ADC) to quantize the charge. The quantized charge is proportional to the value of the sensing capacitor. Hence, it seems intuitive that simply using an ADC with good energy efficiency will result in a CDC with good energy efficiency. Thus, a successive approximation register (SAR) ADC should be a good candidate for a CDC. However, charge sharing between the sensing capacitor and the capacitive DAC lowers the voltage swing at the comparator input forcing the comparator to burn more power to resolve its input with high accuracy. This results in low energy efficiency for a SAR based high resolution CDC. To address charge sharing between the sensing capacitor and the SAR DAC, [6] uses an operational transconductance amplifier (OTA) to perform an active charge transfer. While this technique solves the issue of reduced swing at the comparator input, the energy efficiency is still low due to the power hungry OTA.

Switched capacitor $\Delta\Sigma$ CDCs are suitable for high resolution CDCs but have low energy efficiency. This is because a $\Delta\Sigma$ CDC requires large oversampling ratio (OSR) to achieve high resolution. Thus, the CDC has to charge/discharge the large sensing capacitor many times to produce the digitized output which lowers its energy efficiency [2]. A recent work [7] combines a $\Delta\Sigma$ ADC with 9-bit SAR, but it uses OTAs which are power hungry. To reduce power and obviate the need for OTAs, a delay chain based CDC was developed in [8], but its resolution is limited and is not suitable for sensing small capacitors despite its wide sensing range.

This paper presents an energy-efficient 2-stage $\Delta\Sigma$ CDC that combines a SAR and a ring voltage-controlled oscillator (VCO). The SAR performs a 9-bit coarse quantization, and the residue is sent to the VCO for fine quantization. VCO is effective at quantizing small voltages in the time domain. Moreover, it provides an intrinsic first-order noise shaping, which increases resolution of the CDC. The combination of SAR with VCO addresses the challenges faced by stand-alone SAR and $\Delta\Sigma$ CDCs, namely (1) reduced swing at comparator input for SAR CDC, and (2) high OSR requirement for $\Delta\Sigma$ CDC. The VCO can absorb quantization errors in the SAR and thus, relaxes the precision requirement for the SAR comparator and permits the use of a small dynamic comparator for power saving. The 9-bit SAR greatly reduces requirements on the VCO linearity and allows the use of low OSR. In addition, the proposed $\Delta\Sigma$ CDC is highly digital, scaling friendly, and OTA-free.

The paper is organized as follows: the proposed CDC design is presented in Section II, the measurements results are presented in Section III and the conclusion is brought up in Section IV.

II. Proposed CDC Design

The proposed CDC along with its timing diagram is shown in Fig. 1. The CDC digitizes the sensing capacitor C_{SENSE} in a single-ended fashion. During the sampling phase ϕ_1, V_{cc} is sampled across C_{SENSE} and C_{REF}, as well as the 9-bit capacitive DAC (C_{DAC}), are reset. At the end of ϕ_1, C_{SENSE} is switched to Gnd, C_{REF} is switched to V_{cc} and the top-plate of C_{DAC} is left open. As a result, a net charge proportional to $(C_{SENSE} - C_{REF})$ is transferred onto C_{DAC}. During ϕ_2, this charge is quantized by the 9-bit SAR ADC. The size of unit capacitor in the DAC is 12fF. Hence, the DAC can sense a maximum capacitance difference $(C_{SENSE} - C_{REF})$ of 6pF. There is no redundancy in the DAC because the second stage VCO can absorb quantization error. The range of capacitance C_{SENSE} which can be sensed by the CDC is extended by C_{REF}.

After the SAR stage finishes quantization, the residue voltage V_{res} is directly available at the comparator input. The residue is sent to the VCO during the phase ϕ_3. The VCO performs a phase domain integration of V_{res} and its output d_2 is obtained by sampling the phase and performing a first-order digital differentiation $(1 - z^{-1})$ on it. The VCO consists of a 7-stage current-starved inverter chain. At any

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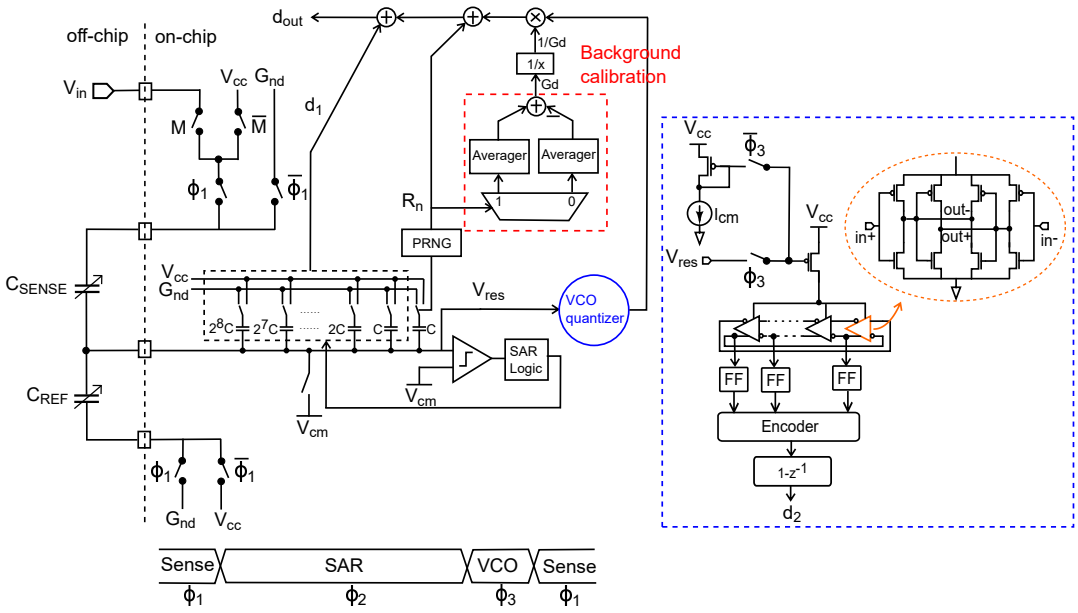

Fig. 1. Circuit diagram showing the proposed CDC.

given time, only one of the VCO stages is in a state of either a positive or a negative transition. Thus, for a 7-stage VCO, the instantaneous phase can be quantized into 14 levels between $(0, 2\pi)$ corresponding to 7 positive transitions and 7 negative transitions. The VCO gain is chosen carefully to ensure that the VCO phase does not overflow during a sampling period. PMOS tail current is chosen over NMOS to reduce flicker noise. Each VCO cell is made pseudo-differential to improve power supply rejection. During ϕ_1 and ϕ_2, the VCO is not switched off as charge leakage will introduce error in the phase value held by the VCO and degrade the CDC linearity. Instead, the VCO is controlled by a small current source I_{cm} which keeps the VCO running at a low frequency. To facilitate the testing of the CDC, we provide two operation modes controlled by M. When M=1, the CDC is in the normal operation mode. When M=0, the CDC is in test mode and C_{SENSE} samples an external voltage V_{in}. This allows the full-range testing of CDC using a fixed C_{SENSE} and variable V_{in}.

The final CDC output d_{out} is obtained by combining the first-stage SAR output d_1 and the second-stage VCO output d_2. To ensure high linearity, d_2 needs to be scaled with an appropriate digital gain G_D that matches the analog interstage gain G_A. This is a challenge for the proposed CDC because G_A depends on the VCO tuning gain which is PVT sensitive. To address this issue, a digital background calibration technique is used. A pseudo-random number generator (PRNG) is built on-chip using a 20-stage linear feedback shift register (LFSR). Its output R_n controls an LSB capacitor in C_{DAC}. When $R_n = 0$, the LSB capacitor is always connected to Gnd. When $R_n = 1$, the LSB capacitor is switched to V_{cc} by the end of ϕ_2. As a result, V_{res} increases, resulting in a larger d_2 compared to when $R_n = 0$. Since the amount of shift in d_2 corresponds to an LSB change in d_1, it exactly reflects the interstage gain G_A. As a result, we can extract G_A from the difference between the d_2 averages for $R_n = 1$ and $R_n = 0$. This can be implemented easily in the hardware by passing d_2 through a 1-to-2 DEMUX followed by two averaging blocks and a subtractor. This calibration technique operates in the background without disturbing the normal operation of the CDC.

Fig. 2 shows the signal flow diagram of the proposed CDC. The factor G reflects the voltage attenuation at the comparator input node due to charge sharing between C_{SENSE}, C_{REF}, C_{DAC}, and the parasitic capacitance C_{par}. G is given by $\{C_{DAC}/(C_{DAC} + C_{SENSE} + C_{REF} + C_{par})\}$. K_{VCO} is the VCO tuning gain. d_2 is scaled by the digital gain G_D and then combined with d_1.

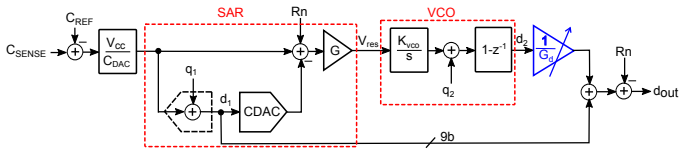

Fig. 2. Block diagram of the proposed CDC architecture.

Based on Fig. 2, it is easy to derive that

$$d_{out} = \frac{(C_{SENSE} - C_{REF})V_{cc}}{C_{DAC}} + q_1\left(1 - \frac{G_A}{G_D}\right) + \frac{q_2(1 - z^{-1})}{G_D} - R_n\left(1 - \frac{G_A}{G_D}\right) \quad (1)$$

where G_A is the analog interstage gain given by GK_{VCO}. If $G_A = G_D$, the SAR quantization noise q_1 as well as R_n is cancelled at the output. The final quantization noise at d_{out} comes solely from the VCO stage and is first-order shaped. Any mismatch between G_A and G_D will result in q_1 and R_n leaking to the output, thus significantly increasing the in-band

noise floor. To ensure $G_A = G_D$, we digitally adjust G_D to match G_A. More specifically, we set

$$G_D = \overline{d_2(R_n = 1)} - \overline{d_2(R_n = 0)}$$

where d_2 is given by $d_2 = -q_1 G_A + q_2(1 - z^{-1}) + G_A R_n$. Note that only the last term in d_2 depend on R_n. The first two terms in d_2 do not depend on R_n, and thus, are canceled in the subtraction between d_2 for $R_n = 1$ and $R_n = 0$.

III. Measurement Results

The proposed CDC is implemented in 40nm CMOS process. The prototype consumes 75μW from 1V supply while operating at 3MS/s. At OSR=3, the equivalent measurement time is 1μs. and the total conversion energy is 75pJ. Fig. 3 shows the measured SNR versus sensing capacitance at an OSR of 3. For C_{REF} = 0, the CDC supports an input range of 0-5pF. The capacitance sensing range is extended by using a nonzero C_{REF}. SNR increases with C_{SENSE} till 5pF. Beyond 5pF, as the sensing capacitance is together with C_{REF}, SNR is reduced due to increased charge sharing.

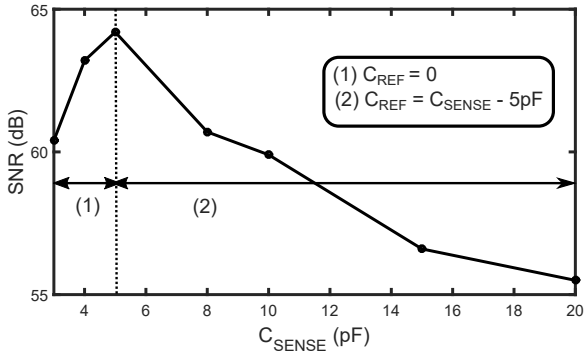

Fig. 3. Measured SNR versus C_{SENSE}.

In the test mode (M=0), a fixed capacitor C_{SENSE} of 5pF is connected to the CDC and C_{REF} is set to 0. A sine wave of 50KHz is applied to V_{in} and the CDC output is sampled at 3MHz. Fig. 4 shows the measured CDC output spectra. Background calibration improves the SNR by 2 dB. The measured SFDR is 70.8 dB which is limited not by the CDC chip but the sensor capacitor itself.

Fig. 5 shows the output digital code versus C_{SENSE}. The errorbars on the transfer curve represents 1σ of the noise. It can be seen from Fig. 5 that the CDC has excellent linearity.

Fig. 6 shows the measured distribution of the VCO output d_2. The average of d_2 is 8.64 when $R_n = 1$ and 8.23 when $R_n = 0$. From this difference, we can extract $G_A = 0.41$. Fig. 7 shows SNR and FoM versus OSR. The best FoM of 55fJ/step is obtained at OSR of 3 with an SNR of 64.2 dB. Fig. 8 shows the die photo.

Table I compares the proposed CDC with the state-of-the-art. It can be seen that the proposed CDC has the best figure-of-merit and improves the energy efficiency by more than 2X compared to prior work. It can be seen that OTA-based $\Delta\Sigma$ CDC does not achieve a good energy efficiency. SAR based CDC improves the energy efficiency compared to

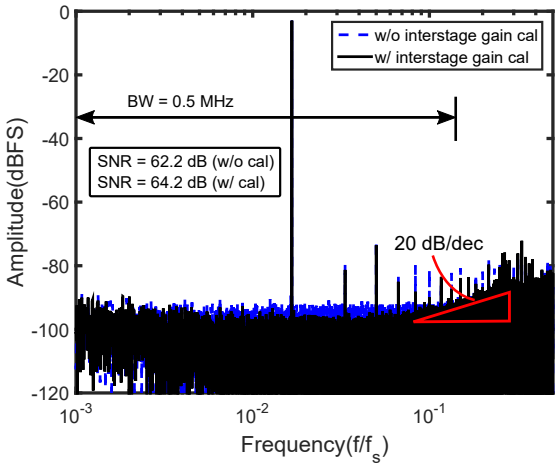

Fig. 4. Measured spectrum of the CDC with M=0.

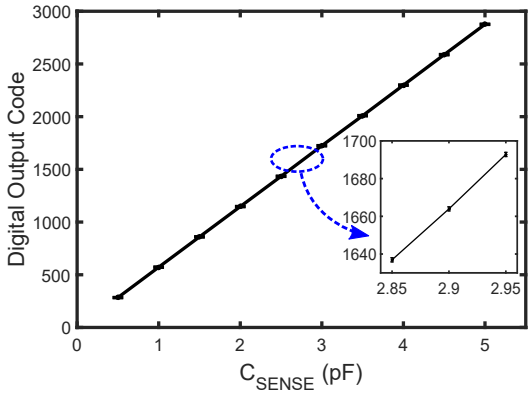

Fig. 5. Measured d_{out} versus C_{SENSE}.

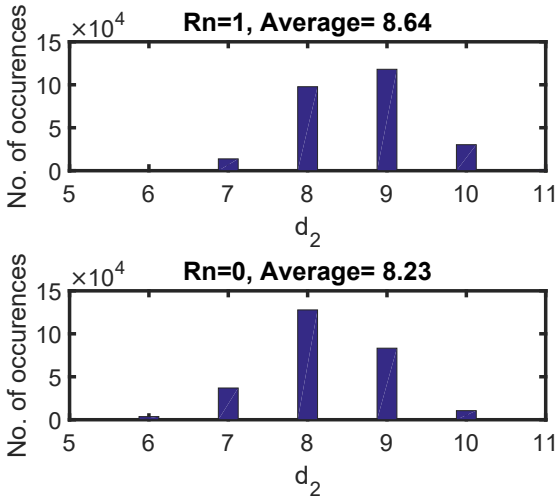

Fig. 6. Measured d_2 histogram for $R_n = 1$ and 0.

$\Delta\Sigma$ CDC. Combination of SAR+$\Delta\Sigma$ achieves better energy efficiency than both SAR-only and $\Delta\Sigma$-only CDCs. The proposed SAR+VCO architecture performs better than dual-slope and SAR+$\Delta\Sigma$ architectures due to its highly digital nature and absence of power hungry OTAs. The proposed CDC prototype has the shortest measurement time compared to prior

TABLE I

COMPARISON WITH PRIOR ART.

	[1]	[2]	[3]	[6]	[7]	[8]	[9]	**This Work**
Process(nm)	180	350	160	180	180	40	130	**40**
Method	Dual-slope	$\Delta\Sigma$	$\Delta\Sigma$	SAR	SAR+$\Delta\Sigma$	Delay Chain	Frequency	**SAR+VCO**
Input range (pF)	5.3-30.7	8.4-11.6	0.54-1.06	2.5-75.3	0-24	0.7-10000	6-6.3	**0-5**
Meas. time (μs)	6400	20	800	4000	230	19	1000	**1**
Resolution (fF)	54.9	0.06	0.07	6	0.16	12.3	3.6	**1.1**
Energy (nJ)	0.704	298	8.24	0.64	7.75	0.035	0.27	**0.075**
SNR [1](dB)	44.2 [3]	84.8	68.4	55.4	94.7	49.7	29.4	**64.2**
FoM [2](fJ/conv-step)	5300 [3]	21000	3800	1330	175	140	11000	**55**

[1] $\text{SNR} = 20\log\left(\frac{\text{Capacitance range}/2/\sqrt{2}}{\text{Capacitance resolution}}\right)$

[2] $\text{FoM} = \frac{\text{Energy}}{2^{(\text{SNR}-1.76)/6.02}}$

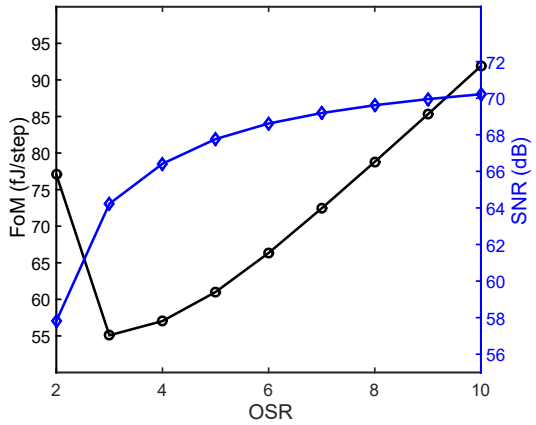

Fig. 7. FoM and SNR versus OSR.

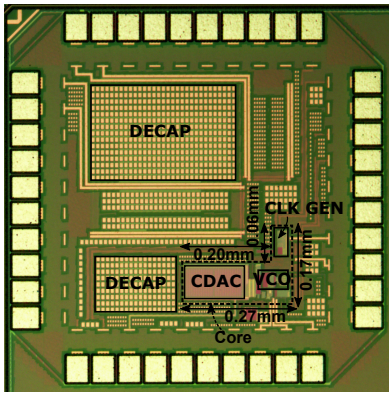

Fig. 8. Die photo.

works, and energy of the prototype can be reduced further by trading off speed.

IV. CONCLUSION

A hybrid SAR-VCO based $\Delta\Sigma$ CDC has been presented in this paper. The proposed architecture combines the merits of both SAR and $\Delta\Sigma$ to achieve high resolution with good energy efficiency while being highly digital in nature. A prototype implemented in 40nm CMOS process has an SNR of 64.2 dB with an energy efficiency of 55 fJ/conversion-step which is 2.5 times better than the state-of-the-art.

ACKNOWLEDGEMENT

The authors would like to thank TSMC shuttle program for chip fabrication. This work was supported in part by NSF grants 1254459, 1509767 and 1527320.

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