A 24-μW 11-bit 1-MS/s SAR ADC With a Bidirectional Single-side Switching Technique

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Abstract—This paper presents a low-power SAR ADC with a bidirectional single-side (BSS) switching technique. It reduces the DAC reference power and the total number of unit capacitors by 86% and 75% respectively, compared to the conventional SAR switching technique. It also minimizes the DAC switch driving power as it has only 1 single-side switching event every comparison cycle. Unlike the existing monotonic switching technique that also has only 1 switching event, the comparator input common-mode voltage for the proposed technique does not converge to ground but to V_{cm}, and thus, obviates the need for a specially designed comparator. To further reduce power, a segmented common-centroid capacitor layout is developed to ensure good matching accuracy. An 11-bit prototype ADC fabricated in 0.18-μm 1P6M CMOS technology achieves an ENOB of 10.3 bits and an SFDR of 77 dB. Operating at 1 MS/s, it consumes only 24 μW from a 1V power supply, leading to a FOM of 19.9 fJ/conv-step.

I. INTRODUCTION

SAR ADC becomes more popular recently as it is low power and scaling friendly. It consists of a capacitive DAC, a comparator, and a SAR logic block. The DAC can contribute a large portion of the total ADC power especially at high resolution with large capacitors. Several techniques have been developed to reduce the DAC power, including the split capacitor technique [1], the V_{cm}-based switching technique [2], and the monotonic switching technique [3]. The V_{cm}-based technique can substantially reduce the DAC reference power, but it requires additional switches to pass V_{cm}. Due to the reduced overdrive voltage, these switches need to be big, leading to increased area and DAC switch driving power [4]. The monotonic switching technique of [3] has attracted increasing attention as it reduces both the DAC reference power and the switch driving power. It does not need extra switches. Moreover, it has only 1 switching event at only one side of the differential DAC array during every comparison cycle. Thus, its switching activity is only about 33% of the conventional switching technique and 50% of the V_{cm}-based technique. In addition, it can cut down the total number of unit capacitors by half. Nevertheless, it has one key limitation. Its comparator input common-mode voltage has a large variation and eventually converges to ground. As a result, the ADC linearity is degraded and the comparator needs to be specially designed, which results in a larger comparator power and increased design complexity.

This paper presents a bidirectional single-side (BSS) switching technique. It maintains all aforementioned merits of the monotonic switching technique and solves its issue of large common-mode variation. Instead of switching DAC capacitors from V_{ref} to ground monotonically as in [3], the proposed technique first switches the MSB capacitor from ground to V_{ref}, and then, switches other capacitors from V_{ref} to ground. As a result, the range of comparator input common-mode variation is reduced by half. More importantly, the common-mode voltage converges to V_{cm} instead of ground. As a result, the proposed technique obviates the need for a special comparator. Furthermore, the proposed technique uses (V_{ref}, V_{cm}) as two reference voltages at the LSB capacitor instead of (V_{ref}, ground). Thus, an extra bit can be obtained via an additional comparison. Consequently, for the same ADC resolution, the proposed technique reduces the total number of unit capacitors by 2 times compared to the monotonic switching technique and 4 times compared to the conventional switching technique. Overall, the proposed technique can achieve 86% reduction in the DAC reference power with bottom-plate sampling. Although bottom-plate sampling is less power efficient, it is favorable for high resolution as it removes the input dependent charge injection.

An 11-bit prototype ADC using the proposed switching technique is implemented in 0.18-μm CMOS process. It achieves 10.3-bit ENOB at 1 MS/s and consumes 24 μW power, which leads to a FOM of 19.9 fJ/conv-step. To ensure good capacitor matching, a segmented common-centroid layout with surrounding dummy capacitors is developed. Having a total capacitor size of only 1.04 pF (unit MIM capacitor of 2 fF and an equivalent LSB capacitor size of 0.5 fF), the ADC achieves 77 dB SFDR without any calibration.

The paper is organized as follows. Sec. II describes the proposed bidirectional single-side switching technique. Sec. III presents the detailed circuit implementation. Sec. IV shows the measured results. The conclusion is drawn in Sec. V.

II. PROPOSED BIDIRECTIONAL SINGLE-SIDE SWITCHING

Fig. 1 (a) and (b) show a 3-bit SAR ADC example with the monotonic switching technique and the proposed BSS switching technique. The proposed technique works as follows. The analog input is sampled on the capacitors' bottom plates to ensure high linearity. After sampling, the left-hand-side MSB capacitor is initialized to ground, while the right-hand-side LSB capacitor is connected to V_{ref}. When the first comparison is done, one of MSB capacitors is switched up from ground to V_{ref}. Following the second comparison, one of the LSB capacitors is switched from V_{ref} to V_{cm}, and an additional
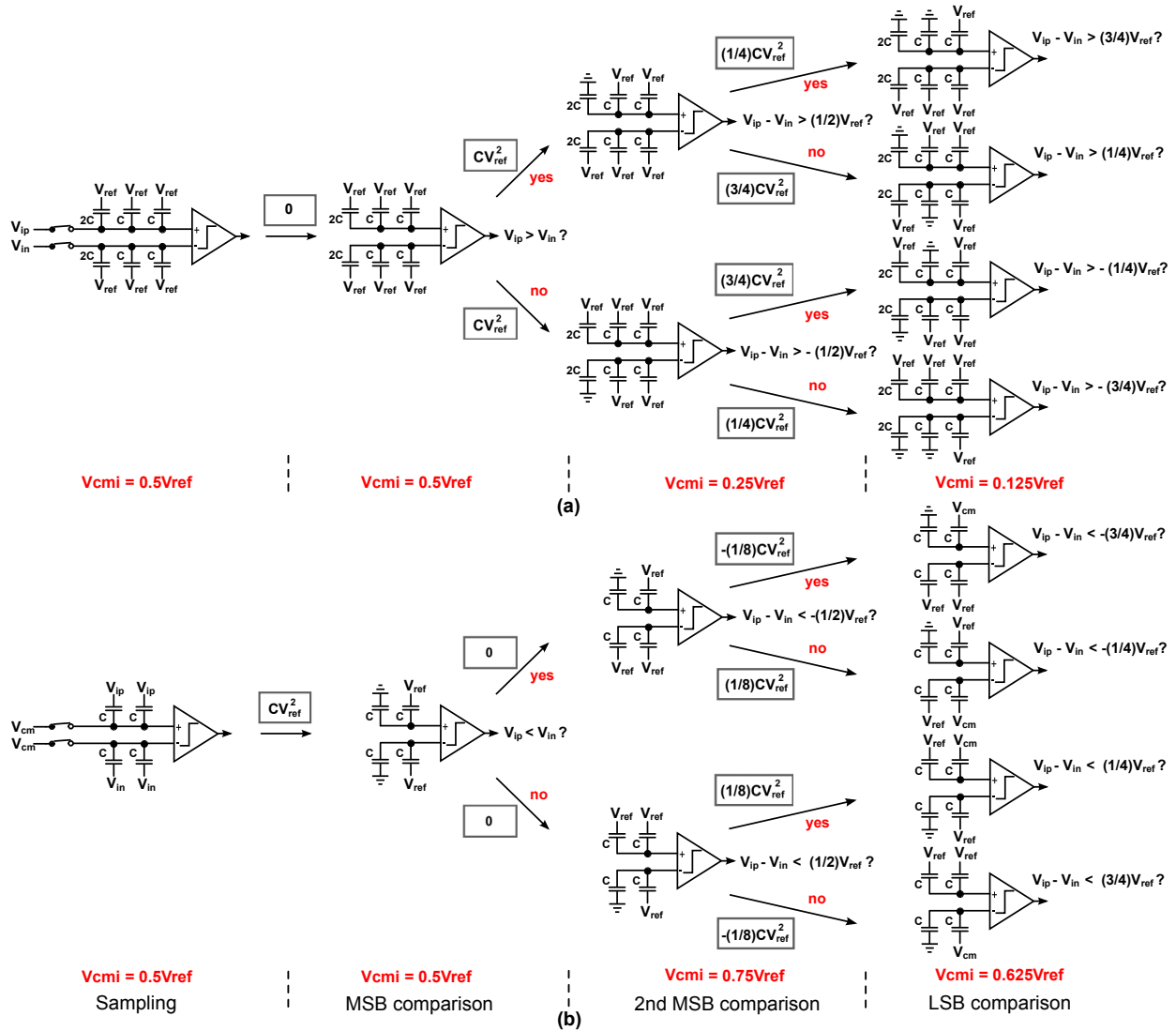
Fig. 1. (a) Monotonic switching procedure [3]; (b) Proposed bidirectional single-side switching procedure.

third comparison is launched. This operation scheme can be easily generalized to more number of bits. An interesting note is that the average power drawn from V_{cm} during the LSB comparison is 0. The reason is that for 50% of time it sends power to the DAC while it receives power from the DAC for the other 50% of time. Although V_{cm} is used as a reference voltage in the LSB comparison, it does not need to be accurate. Simulation confirms that 5% deviation in V_{cm} only causes an INL/DNL error of 0.05 LSB. In our design, the same V_{cm} is shared for both the sampling phase and LSB comparison phase.

For a 3-bit SAR ADC, the proposed technique requires a total capacitance of only $4C$. By contrast, the conventional switching technique requires in total $16C$ (the monotonic switching requires $8C$). Thus, for a fixed unit capacitor size, the proposed technique can reduce the total DAC capacitance by 4 times, leading to reduced chip area and power. Or, for a fixed total DAC capacitance, the proposed technique allows a 4 times bigger unit capacitor, which allows better matching

and simplifies the layout design.

As shown in Fig. 1, the monotonic switching technique consumes an average DAC reference energy of $1.5CV_{ref}^2$ for a 3-bit SAR ADC, while that for the proposed technique is only CV_{ref}^2. For an 11-bit SAR ADC, the conventional switching technique consumes $2729CV_{ref}^2$, while the monotonic switching technique consumes $512CV_{ref}^2$, which amounts to 81% power reduction. The proposed technique consumes only $384CV_{ref}^2$, which provides 86% power reduction even with the less power efficient bottom-plate sampling structure.

Fig. 1 also shows the behavior of the comparator input common-mode voltage V_{cmi} for a 3-bit SAR ADC using the monotonic switching and the proposed switching techniques. For an 11-bit SAR ADC, V_{cmi} for the monotonic switching technique eventually goes to ground, as shown in Fig. 2. Such large common-mode variation leads to linearity degradation and necessitates a specially designed comparator [3]. By contrast, the proposed bidirectional switching technique reduces the range of the common-mode variation by half. Moreover,
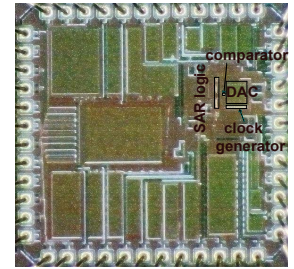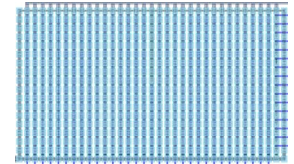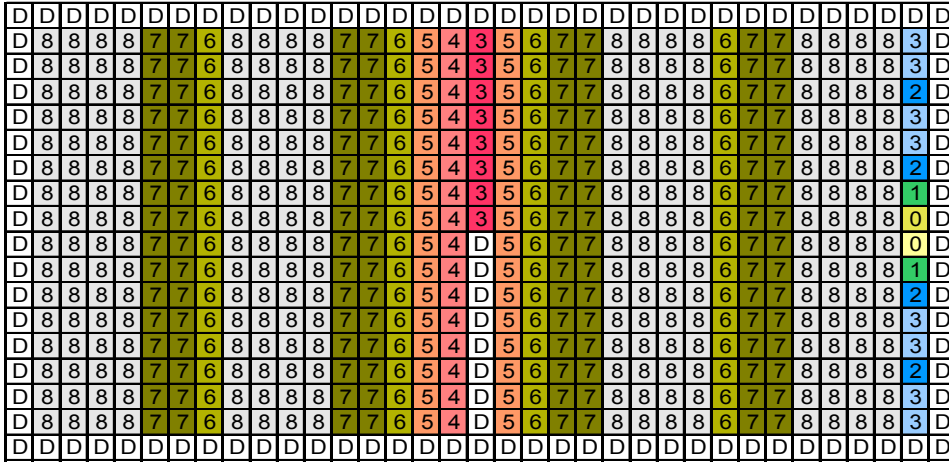
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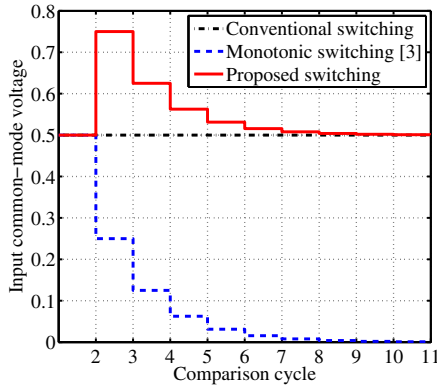Fig. 3. (a) DAC floorplan; (b) DAC layout; (c) chip die.

Fig. 2. Comparator input common-mode variation ($V_{ref} = 1$).

its V_{cmi} converges to V_{cm}, and thus, it obviates the need for a special comparator. For the last several comparisons where high accuracy is required, V_{cmi} stays very close to V_{cm} and its variations exponentially decreases. Thus, the linearity degradation is avoided.
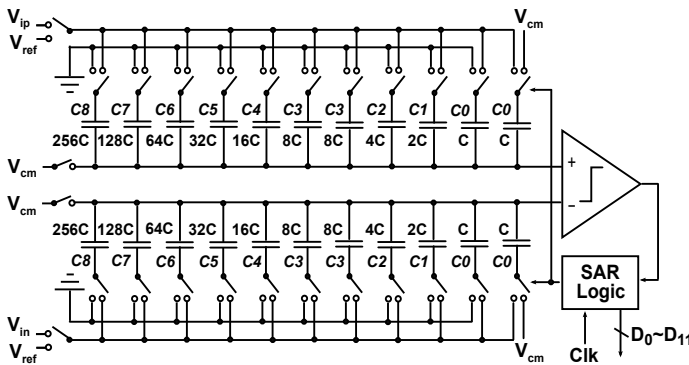
III. CIRCUIT IMPLEMENTATION

Fig. 4. Proposed SAR ADC architecture.

Fig. 4 shows a differential 11-bit SAR ADC using the proposed switching technique. A standard dynamic comparator without the preamplifier is used in this design, which is the same as the dynamic latch shown in [2]. The simulated input-referred noise is 300μV. Unlike [3], no special comparator design is needed, which further reduces the power and design complexity. With the bottom-plate sampling structure, the sampling switches are implemented by transmission gates instead of bootstrapped switches in [3] for power saving. The SAR logic, which is built by shift register, realizes the proposed switching technique.

The capacitive DAC is implemented with binary-weighted capacitors. The unit capacitor size is limited by the thermal noise and matching requirement. This design uses a 2 fF MIM capacitor as the unit capacitor C, which is the minimum MIM capacitor provided in the 0.18-μm CMOS technology. A redundant capacitor $C_3=8C$ is provided to recover possible errors during the first several conversions with large common-mode variations. The total capacitance is $520C$, which is 4 times smaller than the conventional switching technique that requires in total $2048C$ for the same 11-bit resolution.

Since the unit capacitor is only 2 fF, the routing parasitic capacitors have a considerable influence on the capacitor matching accuracy. Although several digital calibration techniques have been developed to calibrate the capacitor mismatch [5], [6], they increase the design complexity and digital power consumption. In this design, a segmented common-centroid technique is used to minimize the capacitor mismatch due to the parasitic capacitors of routing wires. Fig. 3(a) shows the DAC layout floorplan. Each cell means a unit capacitor and the digit indicates the corresponding capacitor. The capacitors are separated into two groups $\{C_8, C_7, ..., C_3\}$ and $\{C_3, C_2, ..., C_0\}$ and each group is placed based on common-centroid rule. Dummy cells, represented as D in the floorplan, are placed for better matching. They are connected to ground to ensure the same parasitic capacitance. The highest metal $M6$ is used for connections of the capacitors' top plates while a lower metal $M2$ is used to connect the bottom plates. By doing this, the parasitic capacitors between two routing wires are minimized. Fig. 3(b) shows the final layout. Post-layout

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simulation shows that the DAC with the proposed layout achieves an INL of ±0.5 LSB and an SFDR of 77.4 dB.

IV. MEASURED RESULTS

The prototype SAR ADC is fabricated in 0.18-μm CMOS process and occupies an active area of 0.1mm^2 [see Fig. 3(c)], which is dominated by the DAC. The power supply is 1V. Fig. 5 shows the measured DNL and INL, which are $+0.53/-0.85$ LSB and $+0.68/-0.91$ LSB, respectively. The major INL jumps occur at first and second MSB transitions.
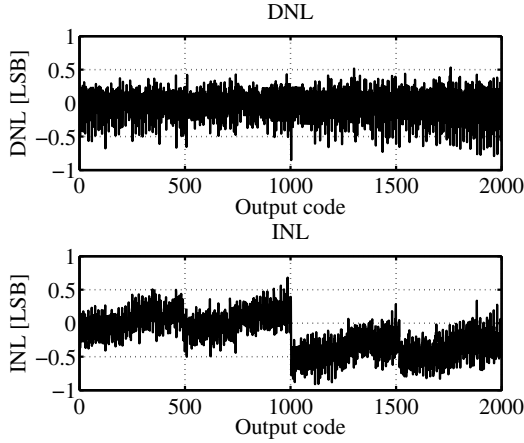

Fig. 5. Measured DNL and INL.

Fig. 6 shows spectrum with a full-scale input at 500 kHz and a sampling rate of 1.05 MS/s. The measured SNDR and SFDR are 63.4 dB and 76.6 dB, respectively. The ENOB is 10.3-bit. Fig. 7 shows the SNDR and SFDR with varying input amplitudes. To evaluate the influence of process variation, we randomly picked and tested 3 other chips. The peak SNDRs are consistently at 63 dB.
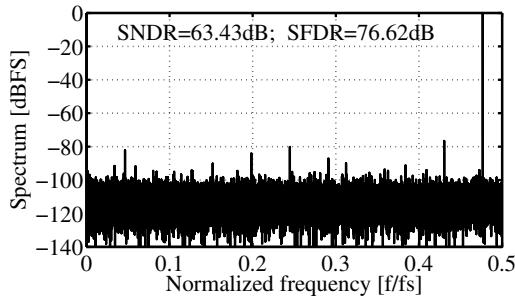

Fig. 6. Measured 65536-point FFT spectrum.

The measured total power consumption is 24.0 μW at 1 MS/s. The DAC, the comparator, and the SAR logic, consume 5.8 μW, 8 μW, and 10.2 μW, respectively. The DAC power accounts for 24% of the total power. This compares favorably to other works with the conventional switching technique, such as [7] whose DAC power is 62% of the total power. The prototype ADC achieves a figure of merit (FOM) of 19.9 fJ/conv-step. Table I compares the performance of the proposed ADC with other recent work using similar processes and voltage supplies.
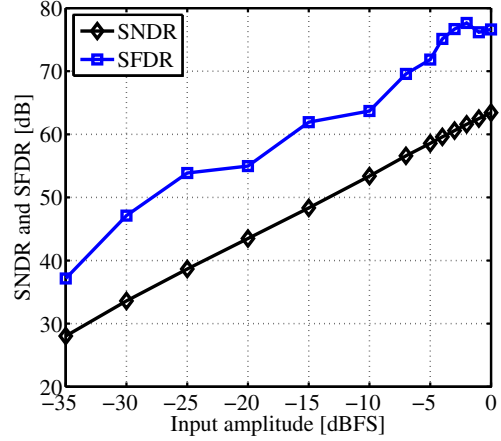

Fig. 7. Measured SNDR and SFDR vs. input amplitude.

TABLE I
PERFORMANCE COMPARISON.

	[3]	[5]	[8]	**This work**
Process [nm]	130	65	180	**180**
Supply Voltage [V]	1.2	1.2	0.9	**1.0**
Sampling Rate [MS/s]	50	50	1	**1**
Resolution [bit]	10	12	10	**11**
Total capacitance [pF]	2.5	1.6	–	**1.04**
ENOB [bit]	9.18	10.9	8.38	**10.3**
Power [μW]	826	2090	7.16	**24.0**
FOM [fJ/conv-step]	29	21.9	21.6	**19.9**

V. CONCLUSION

This paper presented an 11-bit SAR ADC with a novel bidirectional single-side switching technique. It maintains the merits of the monotonic switching technique, and addresses its limitation of large comparator input common-mode voltage deviation. It can reduce the total capacitor size and DAC reference power by 75% and 86%, respectively. It adopts bottom-plate sampling and is suitable for applications that desire both low power and high resolution.

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