A Hybrid SAR-VCO $\Delta\Sigma$ ADC with First-Order Noise Shaping

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***Abstract*—A scaling-friendly, hybrid, two-stage $\Delta\Sigma$ ADC with a 5-bit SAR as first stage and a VCO as second stage is presented in this work. Since the VCO can provide fine quantization for small signals in the time-domain, it is used to directly quantize the SAR residue without OTA-based residue amplification. Also, having a small input swing obviates the need for VCO non-linearity calibration. The VCO phase overflow problem is solved by using a counter to record the number of overflows, thus allowing a variable sampling rate. Since the VCO phase and counter are never reset, the VCO's first-order noise-shaping capability is retained. A prototype ADC in an 180 nm process achieves 73 dB SNDR over 2.2 MHz bandwidth and consumes 5 mW from a 1.8V supply while sampling at 35 MHz.**

***Index Terms*—analog to digital converters (ADC), voltage controlled oscillator (VCO), two stage ADC, successive approximation register (SAR), noise shaping**

I. Introduction

VCO-based ADCs are gaining in popularity and have received a lot of attention from the research community [1]–[6]. This is because VCO-based ADCs lend themselves easily to technology scaling. VCO-based ADCs quantize in the time-domain which is very suitable for advanced technologies in which gate delay is reduced. Reduction in gate delay results in finer quantization step, and hence, increased resolution for VCO-based ADCs. However, VCO-based ADCs suffer from inherent non-linearity which limit the ADC dynamic range.

Researchers have proposed multiple approaches to address this issue. Digital calibration has been used to solve this problem in [1]. The digital calibration used in [1] is complicated, requires accurate replica matching and the input-swing is still limited to reduce higher-order distortion. Another approach is to put the VCO inside a closed loop with a linear gain before the VCO [2]. The distortion of the VCO is reduced by the gain block. A two-stage ADC with a VCO-based second stage is put inside a high gain loop in [3]. The gain block/loop filter is implemented through an OTA. However, an OTA is not scaling-friendly and designing a high-gain OTA in an advanced CMOS process with low supply voltage and low transistor gain will consume a large power and area.

A third approach has been to linearize the VCO in an open-loop configuration without digital calibration. A high linearity delay cell design has been used to address the non-linearity issue in [4]. The approach in [5] has been to convert the analog input to a two-level signal by using a naturally sampled pulse width modulator and switching the VCO between two frequencies. By switching the VCO between only two points on its tuning curve, the non-linearity problem is eliminated. However, [5] still uses OTAs to implement the pulse width modulator. Yet another approach is to use a two-stage ADC with a VCO-based second stage as in [6], where a 5-bit flash ADC has been used as the first stage to reduce the swing of the second-stage. However, it still requires an OTA for residue amplification.

In this work, we propose a novel two-stage architecture which combines a low-resolution SAR ADC with a VCO. The SAR ADC has a very good power efficiency at low resolution, while the VCO is more suitable for quantizing low-swing signals. Thus, combining a SAR ADC with a VCO can reap the benefits of both the ADCs and the overall architecture is very scaling friendly. To the best of the authors' knowledge, this architecture has not been reported in literature. The proposed ADC does not require any OTA and can handle the full input swing without requiring any non-linearity calibration for the VCO. The SAR performs a 5-bit coarse quantization of the input, and the residue is directly fed to the VCO for finer quantization. Since, the VCO sees only the low-swing residue from the SAR stage, which is 1/32 of the input swing, the non-linearity is significantly reduced and no non-linearity calibration is needed for the VCO. The proposed technique has several merits over the technique of [6]. SAR is more power efficient than flash, especially for resolutions ≥ 5 bits. Also, the proposed ADC uses the VCO as an integrator rather than a quantizer as in [6]. The counter used to record the VCO output is reset every cycle in [6], while the counter is always kept running in the proposed technique. This allows the proposed technique to exploit first-order shaping of the quantization noise, which is an important advantage of the proposed technique over [6]. Thus the proposed ADC can also be viewed as a 0-1 MASH $\Delta\Sigma$ ADC.

The paper is organized as follows: the proposed ADC design is presented in Section II, the measured results of the prototype are presented in Section III and the conclusion is brought up in Section IV.

II. Proposed ADC Design

The proposed ADC and its timing diagram is shown in Fig. 1. The first-stage is a 5-bit SAR which performs a coarse quantization of the input signal. Once the SAR finishes comparison, the conversion residue is available at the comparator input. Since the VCO can do fine quantization for small signals in the time domain, the residue is directly transferred to the VCO

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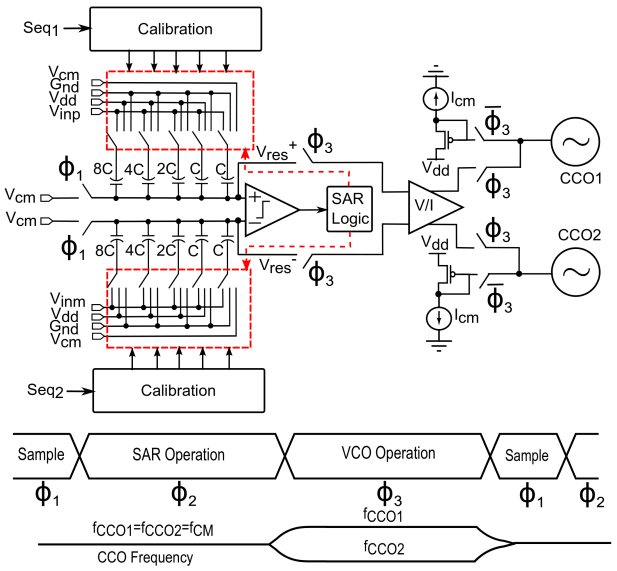


Fig. 1. Proposed hybrid $\Delta\Sigma$ ADC architecture.

without the need of any OTA-based residue amplification. The absence of OTA makes the design more scaling friendly and reduces the ADC power consumption. The clocks required for the 3 phases (ϕ_1, ϕ_2, ϕ_3) are generated synchronously from a master clock. 3 cycles of the master clock are used for sampling the input and 5 cycles of the master clock are allotted for SAR and VCO operation each.

A. SAR ADC

The SAR used in the proposed technique adopts the novel low-power switching technique of [7] in which only one-side of the differential DAC array needs to be switched every cycle. The proposed technique is illustrated in Fig. 2 with a 2-bit example. Switching the LSB capacitor between $(0, V_{cm})$ instead of $(0, V_{dd})$ allows the proposed technique to generate a zero-mean residue for the 2-bit ADC with only 4C capacitance. If a zero-mean residue is not required, the proposed technique can give 3-bit resolution with the same 4C capacitance [7]. In contrast, a 2-bit conventional SAR requires 8C capacitance for nonzero-mean residue and 16C capacitance if a zero-mean residue is required which is more desirable for a two-stage architecture due to lower swing at second-stage input. Thus, the proposed switching technique achieves 4X capacitance reduction compared to the conventional technique and this holds true for an ADC with any resolution. For a 5-bit SAR, the simulated saving in switching energy of the proposed technique is 86% when compared to the conventional SAR.

It should be noted here that any error in the value of V_{cm} has the same effect as mismatch in the LSB capacitor and can be calibrated. Bottom-plate switching is used to ensure linearity of the ADC. The SAR ADC uses a strong-arm latch based comparator without any pre-amplifier. The simulated 3σ offset of the comparator is 15 mV.

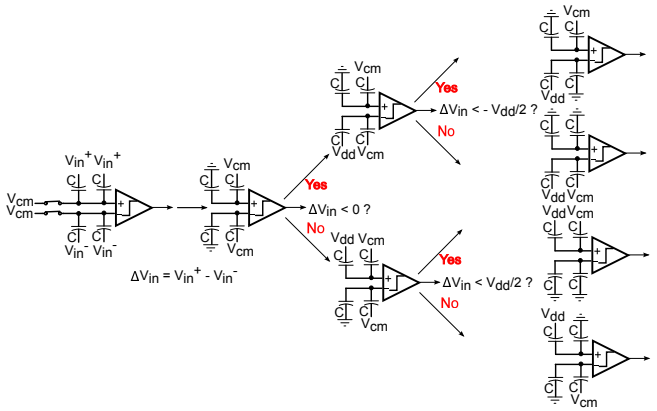


Fig. 2. Switching technique used in SAR ADC shown with a 2-bit example.

B. VCO stage

The VCO consists of a source-degenerated V/I converter and two 7-stage, differential current-controlled oscillators (CCOs) as shown in Fig. 3. The V/I converter has a simulated linearity of 9-bit. The delay cells use weak cross-coupled inverters and are buffered before they are sampled by comparator-based flip-flops. The buffers isolate the delay cells from the kickback noise of the comparators. The use of two CCOs cancel out any major second-order distortion. The CCO phase is obtained by sampling the outputs of all 7 stages and subsequently encoding them to produce a 4 bit output. A 6-bit counter is used to record how many times the phase overflows over one sampling period [8]. The final CCO output is the counter output plus 14 times the phase encoder output.

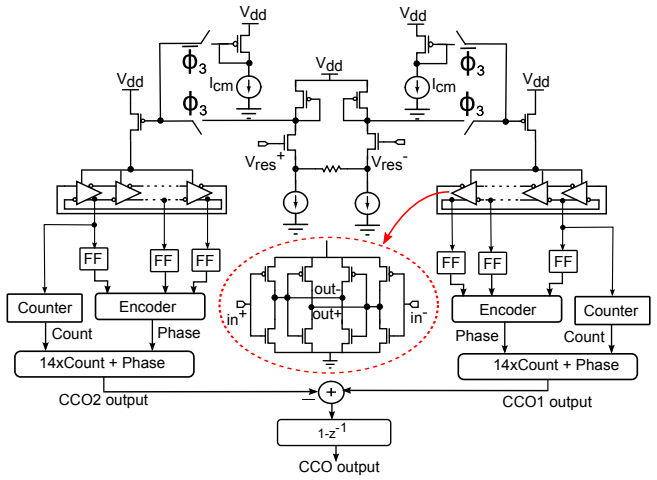


Fig. 3. VCO schematic.

The number of bits available from the VCO stage is given by $n_{vco} = \log_2(2N_{stage} \cdot K_{vco}\Delta v_{in}T_{vco})$ where N_{stage} is the number of VCO stages, K_{vco} is the VCO gain in Hz/V, Δv_{in} is the VCO input swing and T_{vco} is the time-period over which the VCO acts as an integrator (ϕ_3 in Fig. 1). The VCO linearity requirement is relaxed as the VCO input swing is reduced by 32 by the 5-bit SAR front-end. The use

of a counter to keep a record of the phase overflow increases the VCO dynamic range by a factor of 2^M, where M is the number of bits in the counter. This effectively decouples the ADC sampling frequency from both the VCO tuning gain and the VCO center frequency and allows variable ADC sampling rates. For a 6-bit counter, the minimum ADC sampling rate is given by $f_s \geq (5/13)\left(K_{vco}\Delta v_{in}/2^6\right) \approx 1$ MHz, where the factor (5/13) comes from the fact that the VCO integrates for 5 cycles out of 13 (phase ϕ_3). Reducing the sampling rate allows the VCO to integrate for a longer time and thus more bits can be obtained from the second stage which improves the SQNR of the ADC. Thus, the proposed ADC can have a higher resolution by reducing the sampling rate. This is in contrast to typical $\Delta\Sigma$ converters where reducing the sampling rate does not increase the resolution.

To reduce the VCO phase noise, the delay cells use only a PMOS tail current source as shown in Fig. 3. This is because the $1/f$ noise corner for PMOS is much lower than NMOS in 180 nm technology. During the ADC sampling operation (ϕ_1) and SAR operation (ϕ_2) (see Fig. 1), the CCOs are not reset but switched to the same fixed current source; the counter is also kept running. Thus, the VCO is used as a phase integrator and the first-order noise shaping capability is retained.

C. ADC model

The block-level model of the proposed ADC is shown in Fig. 4. In the model, q_1 represents the quantization error of the first stage, δ represents the error due to capacitor mismatches, V_{os} represents the input-referred offset of the comparator, and q_2 represents the quantization error of the VCO stage. The effect of non-zero comparator input capacitance C_{in} and parasitic capacitance C_{par} is captured by the term $G \equiv C_{tot}/\left(C_{tot} + C_{par} + C_{in}\right)$ where C_{tot} is the total capacitance of the DAC. The input swing of the comparator is scaled by the factor G.

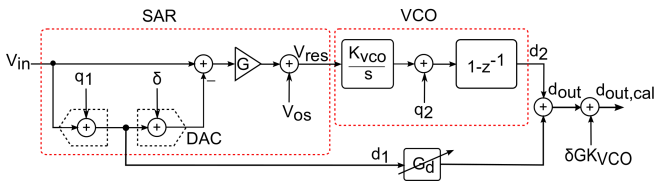


Fig. 4. Model of the proposed ADC.

The overall ADC output is given by

$$\begin{aligned} d_{out} = \; & G_d V_{in} + (G_d - GK_{vco})\, q_1 - \delta G K_{vco} \\ & + K_{vco} V_{os} + (1 - z^{-1}) q_2 \end{aligned} \tag{1}$$

where G_d is the digital interstage gain factor.

It can be seen from (1) that the quantization error from the first-stage will not show up in the overall output if $G_d = GK_{vco}$, i.e, if the digital interstage gain G_d matches the analog interstage gain GK_{vco}. Thus, the only quantization noise in the overall output is the quantization noise of the second stage which is first-order shaped. To ensure linearity, it is important to calibrate DAC capacitor mismatch δ. To this end, a digital calibration technique similar to [9] is employed. A calibration block (see Fig. 1) configures the SAR capacitor array and uses the VCO to measure capacitor mismatches and GK_{vco}. Then G_d is adjusted to match the extracted GK_{vco} and δ is compensated via a digital adder.

D. SNR analysis

The sampling noise is given by $\sqrt{2kT/C_{tot}} = 226\mu V_{rms}$. The input-referred thermal noise of the VCO is given by

$$\overline{v_{vco,in}} = \sqrt{2}\left(\frac{\sqrt{2D_1\left(T_s - T_{vco}\right) + 2D_2 T_{vco}}}{2\pi K_{vco} T_{vco}}\right) \cdot \frac{1}{G}$$

where D_1 is the phase diffusion constant [10] of the VCO during ϕ_1 and ϕ_2 phases, and, D_2 is the phase diffusion constant of the VCO when it is integrating (ϕ_3 phase).

The phase diffusion constant D is evaluated from the value of phase noise $\mathcal{L}(\Delta\omega)$ at an offset of $\Delta\omega$ as $D = \{\mathcal{L}(\Delta\omega) \cdot (\Delta\omega)^2\}/2$. $\mathcal{L}(\Delta\omega)$ at 1 MHz offset during ϕ_1 and ϕ_2 phases is -73.6 dBc/Hz and $\mathcal{L}(\Delta\omega)$ at 1 MHz offset during ϕ_3 phase is -69.2 dBc/Hz. For T_s = 28.6 ns, T_{vco} = 11 ns, K_{vco} = 3.6 GHz/V, and G = 0.8, the input-referred VCO noise, $\overline{v_{vco,in}}$ can be calculated to be $203\mu V_{rms}$.

The input-referred thermal noise of the V/I stage for this design is $283\mu V_{rms}$. Thus, the overall input-referred thermal noise is $414\mu V_{rms}$. For an OSR of 8, the in-band input-referred thermal noise is $146\mu V_{rms}$. Thus, for an input swing of $3.2V_{p-p}$, the thermal noise limited SNR is 77.7 dB.

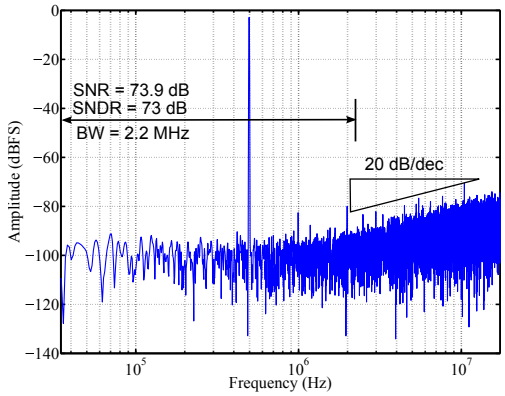
In order to calculate the quantization noise of the ADC, we need to calculate the number of bits available from both the stages. The first-stage has 5 bits, and the number of bits available from the VCO stage, n_{vco}, is given by $\log_2\left(2N_{stage} \cdot K_{vco}\Delta v_{in} T_{vco}\right) = 4.6$. For an OSR of 8, the SQNR is given by $\{6(5+4.6) + 1.76 + 30\log_{10}(8) - 5.2\} = 81.2$ dB. Thus, the overall SNR is 75.6 dB.

III. Measurement Results

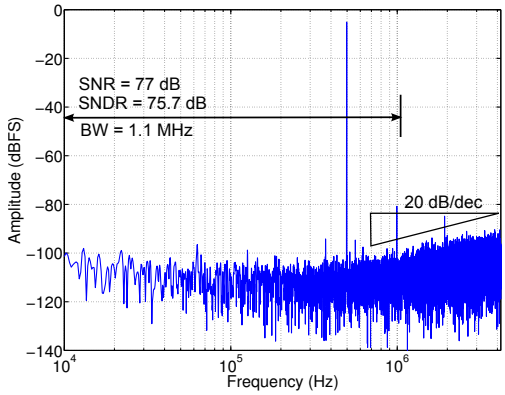
A prototype ADC was designed in 180nm CMOS process. Fig. 5 shows the spectrum of the measured output for two different sampling frequencies of 35 MHz and 8.4 MHz respectively. The input frequency is 497 kHz and the input swing is $3.2V_{p-p}$. The first-order noise shaping can be clearly seen at both the sampling frequencies. The SNDR is 73 dB with an input bandwidth of 2.2 MHz and OSR of 8. The SNDR is 75.7 dB at an OSR of 4 if the sampling frequency is lowered to 8.4 MHz. The CCO center frequency is 487 MHz. The ADC sampling rate is variable. As long as the sampling rate is greater than 1 MHz, there is no phase overflow issue.

The measured SNDR versus amplitude is shown in Fig. 6. It can be seen from Fig. 6 that digital calibration improves the SNDR by about 13 dB.

The prototype consumes 5 mW from a 1.8V supply. The V/I consumes 0.3 mW, while the remaining 4.7 mW goes to the SAR, CCO and counter which are mostly digital and whose power is limited by the 180 nm technology. The die photograph is shown in Fig. 7. The active area is 0.4 mm^2.



(a)



(b)

Fig. 5. 32768-pt windowed FFT of the measured ADC output for (a) f_s = 35 MHz and (b) f_s = 8.4 MHz with $V_{in} = 3.2V_{p-p}$ and f_{in} = 497 KHz.

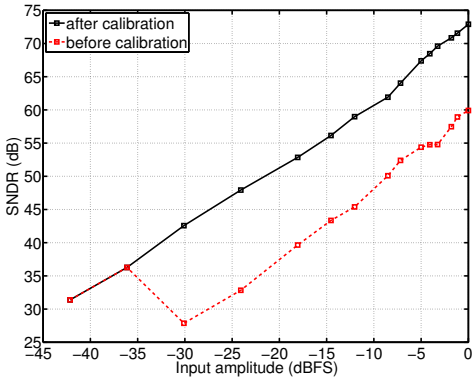


Fig. 6. Measured SNDR vs input amplitude (the departure between the two curves starts when SAR output starts changing).

A comparison of this work with previously reported state-of-the-art VCO-based ADCs with similar resolution and similar bandwidth is summarized in Table I. It can be seen that the proposed ADC has achieved competitive performance. The power-efficiency can be improved dramatically in an advanced technology as the current prototype's power consumption comes almost entirely from digital blocks.

IV. Conclusion

A novel VCO-based, hybrid $\Delta\Sigma$ architecture has been presented in this paper. The proposed ADC is highly digital in nature and uses no OTA. A prototype has been implemented in 180 nm technology and shows good performance when compared with existing VCO-based ADCs. The scaling-friendly nature of the proposed ADC makes it a very good candidate for advanced technology nodes.

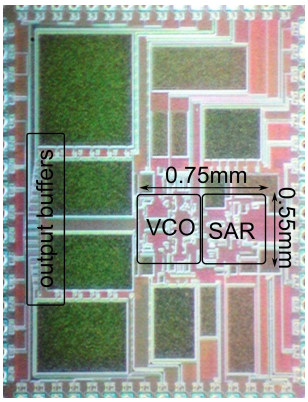


Fig. 7. Die photograph.

TABLE I
Comparison with prior art.

	[1]	[2]	[4]	[5]	**This work**		
Process(nm)	65	130	180	90	**180**		
Area(mm^2)	0.07	0.42	–	0.1	**0.4**		
F_s(MHz)	500	950	128	640	**35**	**35**	**8.4**
BW(MHz)	3.9	10	2	8	**3.5**	**2.2**	**1.1**
OSR	64	47.5	32	40	**5**	**8**	**4**
SNDR(dB)	71	72.4	63.5	59.1	**70**	**73**	**75.7**
Power(mW)	8	40	6	4.3	**5**	**5**	**4.1**
FoM(fJ/step)	344	587	1243	366	**272**	**303**	**382**

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