A 10.5-b ENOB 645nW 100kS/s SAR ADC with Statistical Estimation Based Noise Reduction

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***Abstract*—This paper presents a power-efficient SNR enhancement technique for SAR ADCs. By accurately estimating the conversion residue, it can suppress both comparator noise and quantization error. Thus, it allows the use of a noisy low-power comparator and a relatively low resolution DAC to achieve high resolution. The proposed technique has low hardware complexity, requiring no change to the standard ADC operation except for repeating the LSB comparisons. A prototype ADC is designed in 65nm CMOS. Its SNR is improved by 7dB with the proposed technique. Overall, it achieves 10.5-b ENOB while operating at 100kS/s and consuming 645nW from a 0.7V power supply.**

I. Introduction

Low resolution (ENOB $<$ 10b) SAR ADC can achieve high power efficiency [1]–[3]. However, it is hard to maintain such high efficiency when extending ENOB beyond 10 bits. The reason is that high-resolution ADCs are thermal noise limited, and every 1-bit reduction in thermal noise typically requires 4 times the analog power, which represents a steep tradeoff and leads to a worsened figure-of-merit (FOM). The noise in a high-resolution SAR ADC is usually dominated by the comparator [3]. Several techniques have been developed to reduce the comparator noise without significantly increasing its power. The technique of [4] arranges two comparators where a low power coarse comparator is used for the MSB bits and a high power fine comparator is used for the last two LSB comparisons. It requires the offsets of two comparators to be tightly matched, which is nontrivial at high resolution even with calibration. The data driven noise reduction technique of [3] fires one comparator multiple times when the comparator input is small and the final decision is made via majority voting. This technique requires a carefully tuned metastability detector, resulting in increased design complexity. Yet another technique combines redundancy with averaging [5]. Its merit is that it can also correct DAC settling errors, but it requires more number of comparison cycles and additional DAC control logic. Besides, as will be shown in details later, the SNR improvement using simple averaging is limited.

This paper presents a novel statistical estimation based noise reduction technique. The key idea is if we can estimate the conversion error of an ADC, we can remove it to achieve higher resolution. For a SAR ADC, the conversion error is directly available at the comparator input. Although a noisy 1-bit comparator cannot produce an accurate estimation for its input if used only once, we can repeat the comparison for multiple times and improve the estimation accuracy by examining the probability of the comparator output being '1' or '0'. The estimation of a signal out of noisy environment through multiple trials is a classic *statistical estimation problem* [6]. In this work, an optimal Bayes estimator is developed to achieve the lowest estimation error. To the authors' best knowledge, this is the first time that formal statistical estimation theory is introduced to the ADC field.

Compared to existing comparator noise reduction techniques mentioned earlier, the merits of the proposed technique are as follows. First, it is simple. It does not require an additional comparator with matched offset [4], an accurately tuned metastability detector [3], or extra DAC control logic [5]. In fact, it does not need any change to standard SAR ADC operation except for repeating the LSB comparison for multiple times. The digital estimation can also be easily implemented using a pre-computed look-up table. Furthermore, the proposed technique can suppress not only comparator noise but also quantization error, which is impossible with prior techniques [3]–[5]. Thus, it relaxes the DAC resolution requirement, which simplifies the DAC design. In addition, the proposed technique is more efficient than [3] from the information usage point of view. It makes use of all statistics, while [3] only uses the information whether the number of '1' is more than that of '0'. Last but not least, its estimation accuracy is much higher than basic averaging as in [5].

A prototype ADC is implemented in 65nm CMOS. Using the proposed technique, the measured SNR is improved by 7dB, which matches well with the theoretical prediction. Overall, the ADC achieves an ENOB of 10.5-bit at 100kS/s while consuming only 645nW power from a 0.7V supply.

The paper is organized as follows. Sec. II describes the proposed noise reduction technique. Sec. III presents the circuit implementation. Sec. IV shows the measured results. The conclusion is drawn in Sec. V.

II. Proposed Statistical Estimation Based Noise Reduction Technique

For a SAR ADC, the relationship between V_{in} and D_{out} can be written as:

$$D_{out} = V_{in} + n_s + x \tag{1}$$

where n_s denotes the sampling kT/C noise which is directly added to the input and x represents the conversion residue due to both quantization error and comparator noise. If the comparator is noise free, x is simply the quantization error bounded by $\pm 1/2$ LSB. However, in the presence of large

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comparator noise, x is Gaussian distributed with standard deviation close to the comparator noise. The noise of a SAR ADC is typically dominated not by n_s but by x [3]. To reduce x, the conventional approach is to use a low noise comparator and a high-resolution DAC; however, it requires large power and area.

This paper proposes a simple and power efficient way to reduce noise. The idea is that if we can develop an accurate estimator for x, denoted as $\hat{x}$, we can increase the ADC resolution by subtracting $\hat{x}$ from D_{out} as:

$$D^*_{out} = D_{out} - \hat{x} = D_{out} = V_{in} + n_s + (x - \hat{x}) \quad (2)$$

which shows that the resolution of D^*_{out} is only limited by n_s and the estimation error. It can even surpass the limit set by the quantization error if $\hat{x}$ is very close to x.

Now the key question to answer is how to estimate x. One important property for SAR ADC is that its conversion residue x is readily available at the comparator input after the LSB comparison. Thus, we can directly use the comparator to estimate x. This may sound strange because the comparator can only provide binary decision and its output is error-prone due to noise. How can we use it to accurately estimate an analog quantity x? Certainly 1-time comparison is inadequate, but we can repeat the LSB comparison for a total of N times and estimate x by examining the number of '1's, denoted as k. For example, if $k = N$, we know that x is a large positive value; if $k = 0$, x is most likely a large negative value; and if $k = N/2$, x is highly probable to be close to 0.

It turns out that the estimation of an unknown variable out of noisy experiments is a *classic statistical estimation problem*; thus, we can directly borrow the concepts and theories from statistics for our problem. There are many ways to form $\hat{x}$. The simplest way is to use the basic averaging like in [5] and set $\hat{x} = (2k - N)/N$. Nevertheless, this scheme has large estimation error. It can be proved that the best estimator for our problem with the smallest error is Bayes estimator [6] defined as:

$$\hat{x}_{BE}(k) = E(x|k) = \int_{-\infty}^{+\infty} x g(x|k) dx \quad (3)$$

where $g(x|k)$ is the posterior probability density function:

$$g(x|k) = \frac{P(k|x)g(x)}{\int_{-\infty}^{+\infty} P(k|x)g(x)dx} \quad (4)$$

where $P(k|x)$ is the probability of k conditioning on x, and $g(x)$ is the prior distribution of x. Eq. (3) and (4) are computationally intensive. Fortunately, we only need to solve $\hat{x}_{BE}$ once and store the results in a look-up table. This way, once we know k, $\hat{x}_{BE}$ can be directly obtained from the table. Fig. 1 shows $\hat{x}_{BE}$ for $N = 17$, which is used in the prototype ADC. To calculate $\hat{x}_{BE}$, we need to know the comparator noise σ. It can be measured from the standard deviation of D_{out} by setting $V_{in} = 0$. It can also be extracted from SPICE simulation.

As in any noise reduction scheme, there is always an extra cost of power. For the proposed technique, the total

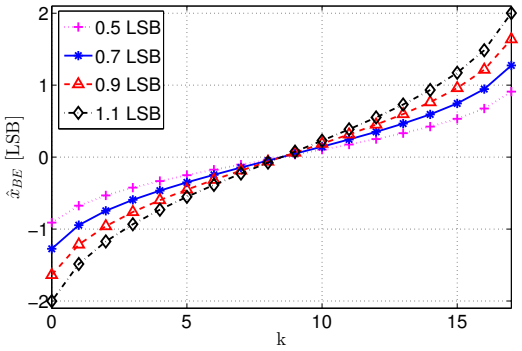

Fig. 1. $\hat{x}_{BE}(k)$ for different comparator noise σ.

power of the comparator increases due to extra number of LSB comparisons. In the prototype 11-bit ADC, to reduce its total noise by 7 dB, the LSB comparison needs to be fired 17 times, which results in an increase of total comparator power by $(11 + 17)/11 \approx 2.5$ times. By contrast, to obtain the same amount of noise reduction for the same 11-bit ADC, if we choose the brute-force way to reduce comparator noise by increasing its size and power, we need to increase the comparator power by 21 times (see Sec. IV). Thus, the proposed technique is much more power efficient. The tradeoff for the proposed technique is reduced conversion rate due to increased number of LSB comparisons. Thus, it is mostly suitable for low-to-medium speed applications.

III. Circuit Implementation

Fig. 2 shows the SAR ADC architecture with the proposed noise reduction technique. The only changes to the standard SAR operations are: 1) the clock generator is modified to repeat the LSB comparison for 17 times; and 2) a 5-bit counter is used to count the number of '1's to obtain k.

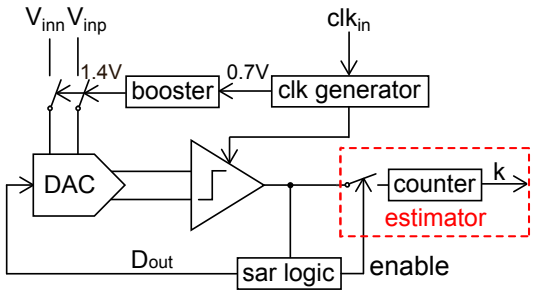

Fig. 2. Proposed SAR ADC architecture.

A. Capacitive DAC

The DAC is implemented with binary-weighted capacitors. The unit capacitor C_U is minimized to save power. Considering the noise and matching requirement, this design chooses $C_U = 2$ fF, which is the smallest MOM capacitor provided in the PDK. A bidirectional single-side (BSS) switching technique is adopted to further reduce the DAC reference power by 86% compared to the conventional switching scheme [7].

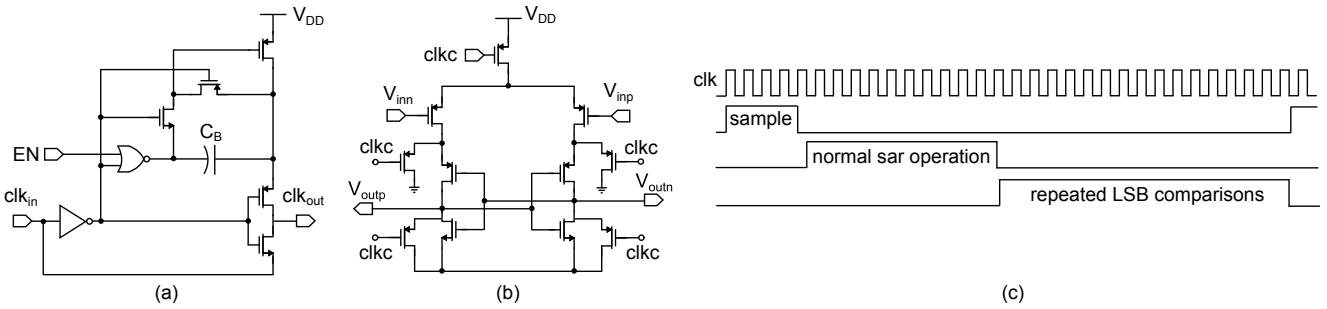

Fig. 3. (a) clock booster; (b) comparator; and (c) timing diagram.

BSS reduces the number of unit capacitors by 4 times, leading to a small capacitor array of {256, 128, 64, 32, 16, 16, 8, 4, 2, 1, 1}C_U for an 11-bit ADC. The redundant capacitor $16C_U$ is provided to recover possible errors during the first several MSB comparisons with large comparator input common-mode variation [7]. The differential sampling kT/C noise is 88μV.

B. Input sampling circuit

To ensure good sampling linearity, bottom-plate sampling is used. In addition, a clock booster shown in Fig. 3(a) is employed to double the sampling clock voltage from 0.7V to 1.4V. As a result, simple small NMOS transistors can be used to sample V_{in} instead of an array of bootstrapped switches or large CMOS switches to reduce the design complexity and switch driving power.

C. Dynamic latch comparator with noise reduction technique

Fig. 3(b) shows the dynamic comparator. It uses a PMOS input pair to minimize the flicker noise and substrate coupling. Thanks to the proposed noise reduction technique, the comparator thermal noise requirement is relaxed, leading to substantially reduced comparator power. In this design, the simulated overall input referred comparator rms noise is 490μV or 0.72 LSB.

D. Clock generation and SAR logic

The ADC timing diagram is shown in Fig. 3(c). It uses a synchronous clocking scheme. The frequency of the master clock is 32 times faster than the sampling rate. The first 4 clock cycles are used for input sampling to ensure high sampling accuracy; the subsequent 11 cycles are used for normal SAR operation; and the final 17 cycles are used for repeated LSB comparisons. This clock allocation scheme can be easily implemented using a ripple counter based clock divider and several AND gates.

The SAR logic is built by standard shift registers. When the normal SAR operation finishes and the last shift register makes transition, a counter is enabled as shown in Fig. 2. It records the number of '1's during the LSB comparisons and obtains k for statistical estimation.

IV. Measured Results

The prototype ADC in 65nm CMOS occupies an active area of 0.03 mm^2 dominated by the DAC (see Fig. 4).

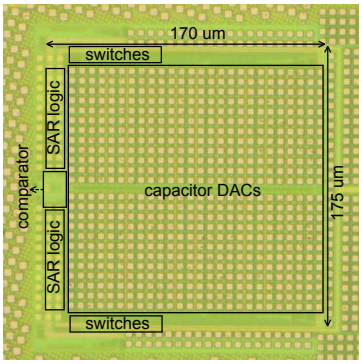

Fig. 4. Die micrograph.

The measured INL is $+1.57/-1.23$ LSB and is shown in Fig. 5. There exists a 1-LSB systematic mismatch between the 6 MSB capacitors and the 6 LSB capacitors, which arises from the unmatched surrounding environment due to the segmented layout strategy [7] and inaccurate parasitic extraction. A simple foreground calibration is performed and the appreciable periodic transition pattern disappears after calibration.

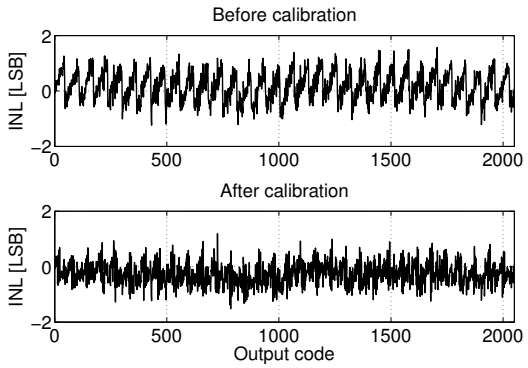

Fig. 5. Measured INL before and after capacitor calibration.

To verify the proposed noise reduction technique, we first measure the ADC noise (e.g., the variation of D_{out}) at $V_{in} = 0$. The measured probability densities for D_{out} before and after noise reduction are shown in Fig. 6 together with fitted normal distributions. Before noise reduction, the standard deviation of D_{out} is 0.73 LSB. It indicates the comparator input referred noise is about 500μV, which is in agreement with SPICE

simulation. After noise reduction, the standard deviation of D_{out} is reduced by 7 dB to 0.33 LSB, which matches well with the estimation theory. Note that if the conventional design approach is used, the comparator noise needs to be reduced to 0.16 LSB in order for the total ADC noise to be 0.33 LSB, which also includes the 0.29 LSB quantization error. This means that the total comparator power needs to be increased by 21 times. By contrast, in our proposed noise reduction technique, the total comparator power is only increased by 2.5 times, which firmly proves its power efficiency.

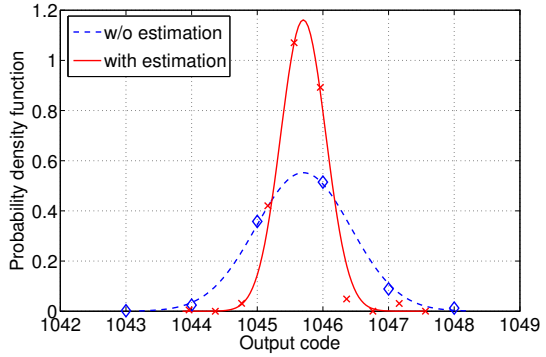

Fig. 6. D_{out} distribution with and w/o estimation at $V_{in} = 0$.

Fig. 7 shows the measured spectrum for a 96kHz full-scale input sampled at 100kS/s. The reason for not choosing a low frequency input is our low-distortion band-pass filter has a cut-off frequency at 90kHz. The measured SNDR and SNR are 59.4 and 59.7 dB, respectively. After applying the proposed noise reduction technique, the SNDR and SNR are improved to 64.5 dB and 65 dB, respectively. The corresponding ENOB is 10.5-bit.

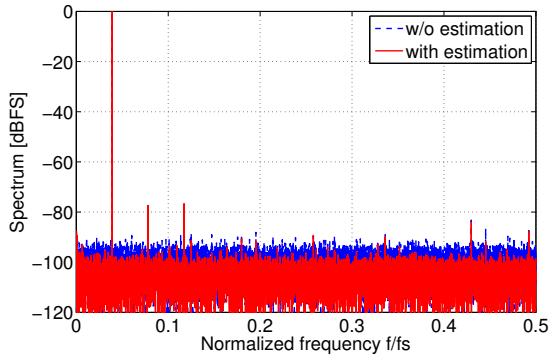

Fig. 7. Measured ADC output spectra with 2^{14} points.

Fig. 8 shows the SNR with varying input amplitudes. The SNR improvement using simple averaging based estimator $\hat{x}_{avg}$ is limited to only 2.2 dB. By contrast, using the Bayes estimator $\hat{x}_{BE}$, the SNR can be improved by 7 dB. When the input is very large, the SNR improvement decreases slightly to 5.3 dB, which is caused by the unwanted coupling from the input to the reference lines, discovered during measurements. However, such SNR loss can be recovered by optimizing layout to reduce the coupling.

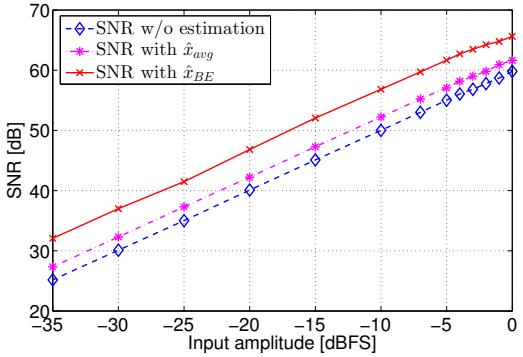

Fig. 8. Measured SNR versus input amplitudes.

The ADC consumes 645nW from a 0.7V power supply. The comparator, DAC, clock generator, and SAR logic consume 70nW, 102nW, 193nW and 280nW, respectively. With the noise reduction technique, the comparator power accounts for only 10% of the total power at the ENOB of 10.5-bit. The digital power, including both clock generator and SAR logic, dominates the overall ADC power. It can be substantially reduced via further thorough optimization and/or going to a more advanced technology node, without affecting SNR. The measured figure-of-merit (FOM) for the prototype ADC is 4.5 fJ/conversion-step. As shown in Table I, the performance of the proposal ADC is comparable to the state-of-the-art works.

TABLE I
PERFORMANCE COMPARISON.

	[1]	[2]	[3]	This work
Process [nm]	90	65	65	65
Supply Voltage [V]	0.35	0.8	0.6	0.7
Sampling Rate [kS/s]	100	32	40	100
Resolution [bit]	10	12	12	11
ENOB [bit]	9.05	11	10.1	10.5
Power [nW]	170	310	97	645
FOM [fJ/conv-step]	3.2	4.8	2.2	4.5

V. CONCLUSION

This paper presented a novel noise reduction technique for SAR ADC based on statistical estimation. It is simple to use and power efficient. It is suitable for applications that require low-power high-resolution ADCs.

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