

CarbonSet: A Dataset to Analyze Trends and Benchmark the Sustainability of CPUs and GPUs

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ABSTRACT

Over the years, the chip industry has consistently developed high-performance processors to address the increasing demands across diverse applications. However, the rapid expansion of chip production has significantly increased carbon emissions, raising critical concerns about environmental sustainability. While researchers have previously modeled the carbon footprint (CFP) at both system and processor levels, a holistic analysis of sustainability trends encompassing the entire chip lifecycle remains lacking. This paper presents CarbonSet, a comprehensive dataset integrating sustainability and performance metrics for CPUs and GPUs over the past decade. CarbonSet aims to benchmark and assess the design of next-generation processors. Leveraging this dataset, we conducted detailed analysis of flagship processors' sustainability trends over the last decade. This paper further highlights that modern processors are not yet sustainably designed, with total carbon emissions increasing more than 50× in the past three years due to the surging demand driven by the AI boom. Power efficiency remains a significant concern, while advanced process nodes pose new challenges requiring to effectively amortize the dramatically increased manufacturing carbon emissions.

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1 INTRODUCTION

The information and communication technology (ICT) sector contributes 2.1%–3.9% of global greenhouse gas emissions with emissions projected to rise [11]. Emissions mainly arise from chip manufacturing, design, and packaging (embodied carbon) and energy consumption of daily operation (operational carbon). Designing

more sustainable processors for both manufacturing and daily use is vital. Recent works include tools for modeling system-level embodied CFP [10] and further chip-level modeling for general processors and reconfigurable systems [4, 23]. Some studies also propose new sustainability-focused metrics for architecture design space exploration [22, 26]. Historical insights of trend analysis and projections of processor metrics have long been integral to the computing industry. For example, Moore's Law—central to driving semiconductor innovation for over 50 years—was understood by curating and analyzing data from numerous chips [14]. Similarly, analyzing trends in CFPs of modern processors (CPUs and GPUs) can raise awareness of their environmental impact, identify areas for intervention, and guide the design of sustainable chips.

1.1 Goals

This paper seeks to create actionable insights into processor sustainability while enabling benchmarking of existing processors based on their CFP. We aim to raise semiconductor community awareness about the growing sustainability challenges computing technologies pose. We curate a dataset of CPUs and GPUs over the last decade, analyzing their CFP across lifecycle stages for both datacenter and desktop series. We aim to answer the following key research questions:

- How has the CFP of flagship GPUs and CPUs evolved?
- Does the increased performance of chips justify higher CFP?
- For flagship processors, which type of CFP dominates? [1, 3]
- Has the AI boom impacted the CFP of processors?
- Is the chip price (\$) a reliable proxy for its Embodied CFP?
- What processor lifetimes effectively amortize Embodied CFP?
- Are chiplet-based processors always more sustainable than monolithic processors?

Answers to these questions help identify key trends and sustainability challenges and also enable more environmentally conscious decision-making in chip design, manufacturing, and lifecycle management.

1.2 Overview of Our Contributions

Figure 1 shows an overview of CarbonSet, including data for desktop and datacenter CPUs and GPUs across multiple metrics - *design metrics* (chip area, technology node, transistors, TDP), *performance metrics* (throughput, OpenCL [8], Passmark [20]), and *sustainability*

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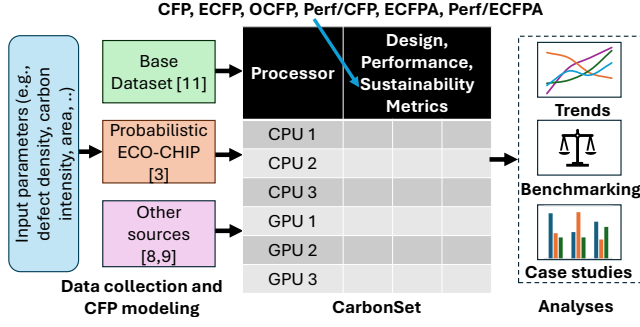


Figure 1: CarbonSet contains sustainability-related metrics for multiple CPUs and GPUs derived from probabilistic carbon modeling.

metrics (Embodied CFP, Operation CFP, total CFP). It also offers composite metrics like Performance per CFP and ECFP per unit area (ECFPA) for further tradeoff-based trend analysis.

Estimating CFP across a processor’s lifecycle is challenging due to uncertainties in parameters such as manufacturing defect density, energy source carbon intensity, utilization patterns, and lifetimes. CarbonSet addresses this issue by extending the ECO-CHIP framework [23] to generate ranges of CFP values instead of a single CFP value. This range of CFP values are evaluated using several probabilistic modeled parameters, which are derived from real-world data and have more practical significance.

From our analysis, we find that flagship GPUs and CPUs are still far away from achieving sustainable design. Although operational CFP (OCFP) still dominates throughout the lifecycle, the proportion of embodied CFP (ECFP) is also increasing due to the advancement of the process nodes. Moreover, in our estimation, given the performance per unit CFP increased by over 100× in some cases, the dramatically increased chip shipments, driven by the AI boom, have eventually led to 50× more total CFP.

To the best of our knowledge, CarbonSet is the first work for processor sustainability evaluation, containing more than 1000 processors, out of which 45% are GPUs and 55% are CPUs. This includes monolithic GPUs, monolithic CPUs, and recent chiplet-based CPUs as well. By leveraging CarbonSet, a Moore’s law-like trend analysis is performed to understand how processor sustainability has evolved, which could also be used for ‘pathfinding’ studies for future architecture design. With more detailed processor specifications and modeling, CarbonSet could also serve as an industry processor sustainability evaluation norm. Our contributions in this work include the following:

- **Comprehensive dataset curation:** We curate a dataset of CPUs and GPUs across desktop and datacenters from multiple vendors, spanning the last decade. This dataset includes detailed design, performance, and sustainability metrics. CFP is evaluated across all stages of the processor lifecycle - design, manufacturing, use, and end-of-life. The complete dataset is available at [16].
- **Probabilistic CFP modeling:** We extend ECO-CHIP to generate ranges of CFP values for each processor based on probabilistic modeled key parameters, including defect density, carbon intensity, energy per area and gas per area. This mitigates the challenges arising from the uncertainties across a processor’s

lifecycle, resulting in practical ranges of CFP values instead of specific values, which are difficult to validate.

- **Sustainability analysis:** We track the sustainability trends of flagship processors, by examining metrics such as ECFP, OCFP, performance per CFP, and ECFP per area. Such an analysis needs significant effort in selecting the most representative flagship processors across generations while ensuring the availability of sufficient performance benchmark data for each selected one.
- **In-depth case studies:** We also conduct several case studies to address the aforementioned research questions to better understand how external factors affect processor sustainability such as the impact of processor lifetime on ECFP amortization, the increasing shipment demands driven by the AI boom, increased manufacturing costs due to advanced process nodes, and the sustainability evaluation of contemporary chiplet architectures.

2 RELATED WORK

Datasets: Researchers have analyzed processor design trends using area, power and performance metrics. For example, [24] reviewed processor design trends over the last two decades discussing the major driving factors of performance increases. Existing datasets, however, do not provide sustainability data for the various processors, which precludes the analysis of trends and the benchmarking of processors from a sustainability standpoint.

Carbon modeling: Driven by the rapidly growing carbon emissions due to the increased number of large-scale datacenters [11, 12, 27], researchers have proposed various CFP modeling frameworks. These range from general first-order estimation [6] to comprehensive system-level modeling (ACT) [10] and support for heterogeneous integration (chiplet-based) chips (ECO-CHIP) [23]. Inspired by [2], We updated ECO-CHIP to generate probabilistic modeled CFP data and then use it to complete CarbonSet.

Metrics: Chip designers and architectures have used traditional metrics such as chip area, frequency, power, performance-per-watt, and area-delay-product to benchmark chips across generations. However, such metrics fail to capture sustainability-related trade-offs. While ECFP and OCFP quantify carbon emissions, new metrics like CDP (Carbon Delay Product), CEP (Carbon Energy Product) [10], performance per unit CFP (Perf-SI), and CFP per billion transistors [22] offer improved tradeoff evaluation. Our dataset includes metrics like CFP, ECFP, OCFP, performance per CFP, embodied CFP per area (ECFPA), and performance per ECFPA.

3 MODELING AND DATASET CONTENTS

3.1 Carbon Footprint Modeling

Prior carbon modeling: In our dataset, CFP is used as the primary metric to estimate the sustainability of a chip. We use ECO-CHIP [23] to evaluate the CFP in all stages of the chip lifecycle, design, manufacturing, use, and end of life. As modeled in ECO-CHIP, total CFP is the sum of ECFP and OCFP. ECFP includes the CFP spent during chip design, manufacturing and packaging. The manufacturing CFP depends on yield and the CFP per unit area (CFPA) of the manufacturing process. Yield is influenced by die area and can be calculated using the equation:

$$Y = \left(1 + \frac{A_{\text{die}} \times D_0}{\alpha}\right)^{-\alpha} \quad (1)$$

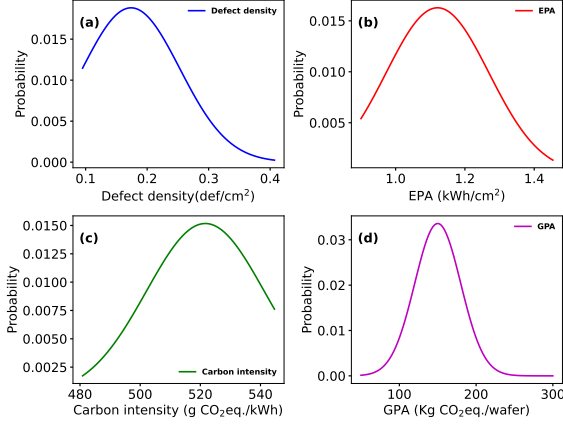


Figure 2: Distributions for (a) Defect density(10nm) [15] (b) Energy-Per-unit Area(EPA)(10nm) [25] (c) Carbon intensity [19] (d) Gas-Per-unit Area(GPA) [17]

where A_{die} is die area, α is the clustering parameter, and D_0 is defect density of current process node, and CFPA is given by [10, 23]:

$$CFPA = \frac{(C_{mfg, src} \times EPA + C_{gas} + C_{material})}{Y} \quad (2)$$

where $C_{mfg, src}$ is the carbon intensity, and it mainly depends on the source of energy for fabrication, EPA is the energy consumed per unit area (kWh per cm^2), C_{gas} is a function of gas per unit area (GPA) emissions usually expressed in kgs of CO_2eq per cm^2 , and $C_{material}$ is the emission from procuring materials expressed in kgs of CO_2eq per cm^2 , and Y is the yield given in Eq. 1.

OCFP is modeled as the carbon intensity of the energy source times the energy spent during operation. The latter is determined by using the TDP and the lifetime scaled by the time during which the chip is in idle state (idle time).

Probabilistic carbon modeling: CFP values are difficult to validate due to the inherent uncertainties of the chip’s lifecycle analysis. Therefore, inspired by [2], we enhance ECO-CHIP to produce a range of CFP values by modeling multiple input parameters as probability distributions. The resultant CFP distribution now represents the viable range of the chip’s CFP values instead of a single value.

Figure. 2 illustrates the probability density function of four input parameters: defect density, EPA, carbon intensity, and GPA. Defect density, EPA, and carbon intensity are modeled using Kernel Density Estimation (KDE), while GPA follows a Gaussian distribution. The distributions of defect density and EPA are derived from 10nm TSMC reports [15, 25]. Carbon intensity is modeled by analyzing global trends over the past 24 years from [19]. The GPA is sourced from IMEC [17], which examines variations in greenhouse gas emissions at fabrication facilities. For OCFP model, a fixed three-year lifetime with 60% idle time is assumed.

Using enhanced ECO-CHIP, we perform Monte Carlo simulations with 10,000 samples per input parameter to model CFP variability across processors. Figure 3 presents the resulting CFP distributions for the A100-SXM and Xeon Platinum 8380. By incorporating parameter uncertainty, ECO-CHIP supports what-if analyses for carbon-aware design decisions. Overlapping distribution regions indicate that the Xeon is not consistently more sustainable than

the A100. For consistency, we use the mean CFP from the 10,000 simulations as the final value for each processor.

3.2 Dataset Contents

CarbonSet builds on a dataset of over 1,000 CPUs and GPUs from vendors such as Intel, NVIDIA, and AMD, covering both datacenter and desktop series. While the base dataset supports trend analysis using conventional metrics, CarbonSet adds a probabilistic model that estimates a CFP range for each processor, using the mean as a representative value. It includes 30 chiplet-based CPUs, assuming equal die area distribution and a uniform process node. Users can modify these assumptions as more vendor architectural details become available.

Due to the complicated system/software configurations, it is difficult to establish a single-chip performance benchmark applicable to both desktop and datacenter CPUs. *SPEC* [21] is a widely accepted CPU performance benchmark; however, comparing scores from different *SPEC* versions (e.g., *SPEC-2017* and *SPEC-2006*) is not valid as each *SPEC* version uses distinct evaluation suites. Therefore, for CPU benchmarking, we use the highest single-chip scores from *Geekbench* for desktops and *Passmark* for datacenter series, respectively [8, 20].

For GPUs, the performance metrics listed in the vendor specifications are rarely achieved in practice. Also, due to varying precision support and the introduction of Tensor Cores, comparing peak metrics across generations is unreliable (e.g., comparing Float16 performance of the A100 with Float32 performance of the P100). Hence, we use the *OpenCL score* from GeekBench as a performance metric of all GPUs [8]. To evaluate performance-sustainability tradeoffs, we include data for the following metrics inspired by [22]:

- **Performance per unit CFP:** This metric measures the performance gain per unit of CFP, which is an overall evaluation factor of the balance between sustainability and performance comprising both the embodied and operational CFP.
- **Embodied CFP per area (ECFPA):** ECFPA assesses the CO_2 density per unit chip area, which is related to the chip manufacturing process node. Generally, an advanced process node has a higher CO_2 emission due to complex lithography processes and lower yields. However, this factor can also be significantly influenced by chip architecture; for example, chiplet-based designs may reduce the overall ECFPA[23]. An architecture with a complicated design process may also increase the design carbon. This metric, therefore, assesses the chip’s sustainability and scalability in the design and manufacturing stages.
- **Performance per ECFPA:** This metric assesses performance gain relative to ECFP and helps to evaluate the performance scalability of the die area for mass production. A chip with high ECFPA but only marginal performance is unlikely to meet sustainability standards. Ideal processors balance low ECFPA with high performance to meet demands sustainably.

4 DATA ANALYSIS AND TRENDS

To showcase the trends in CFP, NVIDIA GPUs and Intel CPUs are selected for their leading roles in datacenter and desktop series, which also offer extensive documentation and architectural specifications. Since most hardware vendors diversify product lines

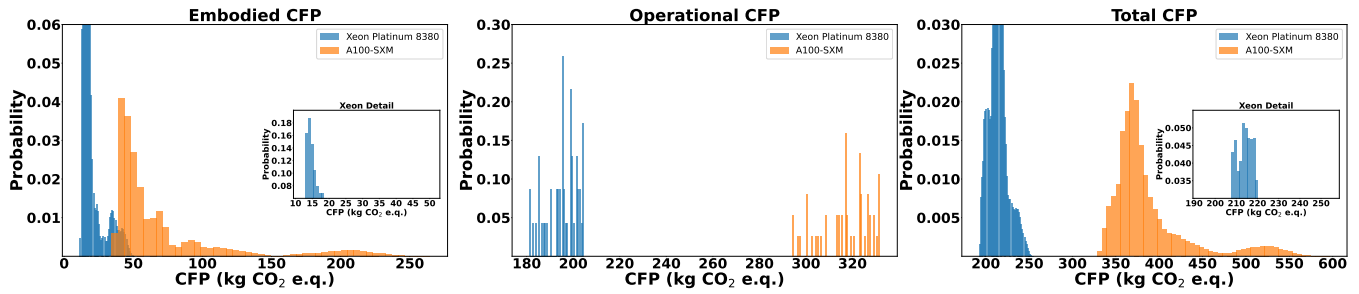


Figure 3: CFP distributions for two flagship processors from our dataset obtained from enhanced ECO-CHIP, by varying defect density, EPA, GPA, carbon intensity, lifetime, and idle time.

by binning and only flagship chips with the largest die and highest TDP are the most complete designs, our dataset only selects those most representative flagship models across both desktop and datacenter series.

4.1 Sustainability Trends in GPUs

The left two plots in Figure. 4 show various design and sustainability metrics for flagship desktop and datacenter GPUs from NVIDIA in the last decade, respectively. Both the datacenter and desktop GPU series exhibit an increasing trend in single-chip total CFP and OCFP, consistently constituting its majority.

In the desktop series, the die area shows significant fluctuations, particularly at the 14nm node from 2016 to 2018, indicating continuous optimization of architecture design during this period. In contrast, datacenter GPUs have consistently increased area over generations. While the die area may fluctuate significantly within the same process node, the total CFP remains stable. For example, in 14nm, TITAN V has significantly increased die size but has a similar CFP to the previous 2 generations. Also, P100 incurs significantly larger CFP but a slightly varied die area. This shows that the ECFP led by the process node and die area contributes much less CFP than OCFP which is dominated by the chip TDP.

The right two plots in Figure. 4 show various performance and sustainability-related metrics for flagship desktop and datacenter GPUs from NVIDIA in the last decade, respectively. The performance metrics are described in Section 3.2. While overall GPU performance continues to improve, the architectural trade-offs and priorities across generations differ significantly when evaluated through a combined perspective of sustainability metrics. Specifically in the desktop series, comparing to TITAN V, TITAN RTX has a similar performance and a significantly smaller ECFPA. However, this does not result in an expected improvement in Performance/CFP nor Performance/ECFPA. This implies that, while a chip’s (e.g., TITAN RTX’s) architecture is optimized for large-scale manufacturing and incurs less ECFP, it may incur much higher OCFP and fail to achieve a greater performance-sustainability balance than previous generations (e.g., TITAN V). Still in the desktop series, the performance/CFP continues to drop after 2018, even with a node advanced from 14nm to 10nm; this highlights that the performance improvements in recent desktop GPUs are being achieved at the expense of increased CFP.

Compared to desktop GPUs, datacenter series appear even more extreme in the pursuit of performance, with models A100-SXM and V100-SXM achieving significantly higher performance with a

boom of CFP, specifically the dropping Performance/CFP and Performance/Embodied CFPA. Although A100 achieves a performance boost of less than 2× compared to V100, it comes at the cost of a dramatically increased ECFPA (over 4×). In contrast, V100 demonstrates significantly lower ECFPA with moderate performance. As a result, V100 achieves around 2× performance/CFP than A100.

In summary, GPUs generally prioritize performance over sustainability, with datacenter GPUs being particularly extreme. Moreover, the comparison of TITAN V and TITAN RTX shows that the OCFP may be one of the major setbacks preventing achieving a better performance-sustainability balance.

4.2 Sustainability Trends in CPUs

The two plots on the left in Figure. 5 show various metrics related to performance and sustainability for Intel’s flagship desktop and datacenter CPUs in the last decade, respectively. OCFP consistently dominates the overall CFP in both series while the proportion of ECFP has a steady growing trend in datacenter CPUs. All CPUs show similar trends in process node evolution, transitioning from 22nm to 14nm, and eventually to 10nm. In desktop CPUs, each process node shrink leads to a significant reduction in die area and an increase in total CFP. Additionally, the die area gradually increases within the same process node, while total CFP slightly fluctuates. In contrast, the chip area of datacenter CPUs increases steadily with a slight dip at the end. Both series demonstrate a reduction in total CFP within the same process node, regardless of changes in chip area, shown by Core i7-6950X and Xeon Platinum 8280 at 14nm. This proves that while a CPU’s total CFP decrease is primarily driven by process node shrinkage, the iterative architectural optimizations within the same process node can effectively enhance processor sustainability.

The right two plots in Figure 5 show various performance and sustainability metrics for Intel flagship CPUs in the last decade, respectively. Overall, the trend for datacenter CPUs is smoother evidencing a more consistent architectural design philosophy. In contrast, desktop CPUs follow greater variability in processor architecture exploration within the same process node leading to violent fluctuations. Specifically, within 14nm process node, Core i7-6960X has both higher performance and ECFPA than Core i7-8700X but leads to a lower Performance/CFP. This demonstrates that architectural design has a great impact on the performance-sustainability tradeoff and it is feasible to design a processor with high performance and low CFP. Subsequently, from 14nm process node all the way to 10nm, Intel kept the performance/ECFPA, performance/CFP

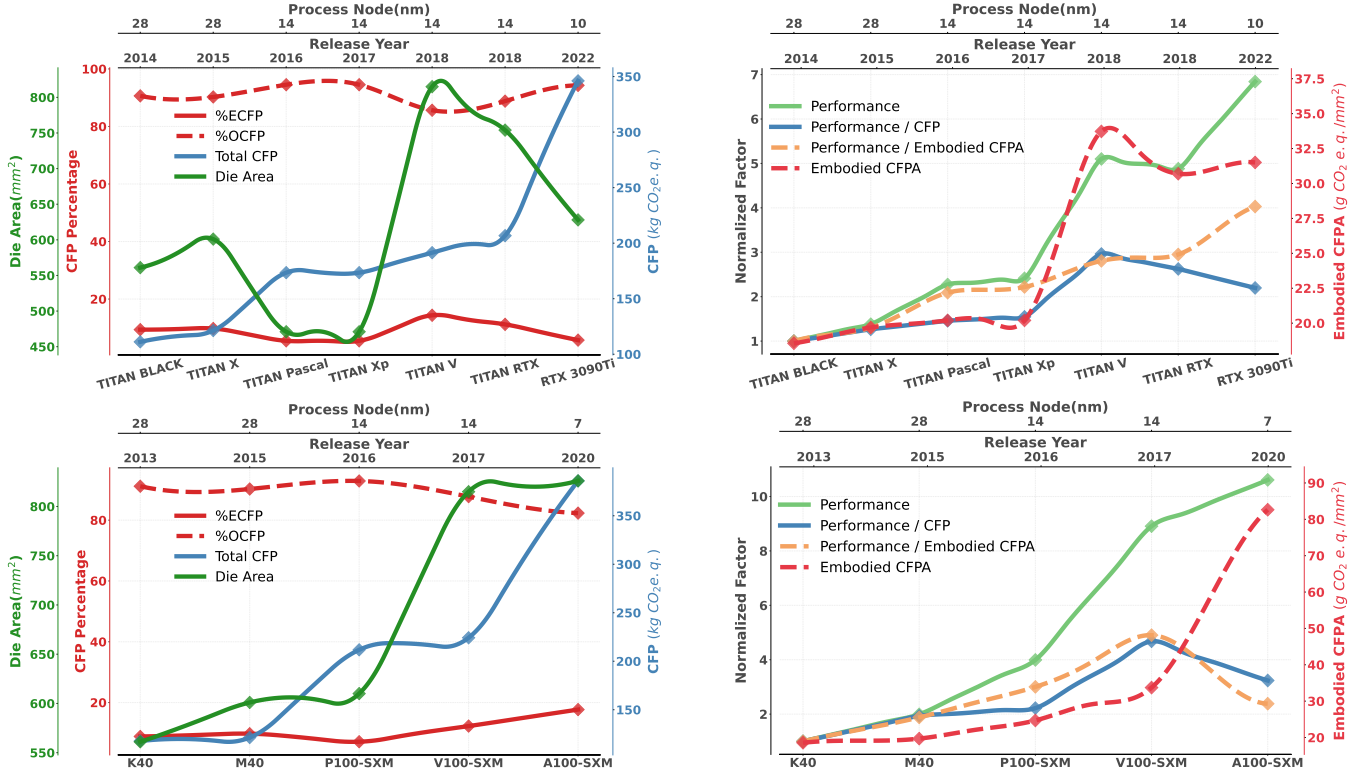


Figure 4: Sustainability trends in flagship desktop (top) and datacenter (bottom) GPUs from NVIDIA

steadily increased, despite the rise in both ECFP and ECFPA, which aligns with the idea of sustainable design.

An opposite trend is observed in datacenter CPUs, where overall performance continues to increase steadily without achieving a good sustainability-performance balance. As process nodes advance, the performance gains do not convert into better sustainability. Both Performance/ECFPA and Performance/CFP show little improvement failing to keep pace with absolute performance. Especially, performance gained a boost at 10nm, but Performance/ECFP and Performance/ECFPA have limited increases. Generally, for datacenter CPUs, the increase in absolute performance is usually accompanied by a significant rise in TDP. Although the share of OCFP is decreasing, the aggressive power consumption continues to limit datacenter processors' sustainability.

4.3 How has the AI boom impacted CFP?

With the surging demand for high-performance GPUs in data centers due to rapidly expanding AI models, estimating datacenter GPU CFP growth provides insights into the impact of this AI boom. To this end, we first estimate the GPU shipments using NVIDIA's Datacenter Business Group annual financial reports [5]. We assume that the group's revenue comes solely from the latest flagship GPU sales with a 75% profit margin while being sold at the highest price. Additionally, we use the peak performance from datasheets as the performance estimator, since there is no publicly available single-chip AI benchmarking across generations of GPUs (e.g. MLPerf [18] scores are unavailable for older GPUs like the P100, and scores are for large multi-GPU systems). Since datacenter GPUs are usually sold as multi-GPU systems the actual single chip price is lower than

the released price, meaning the true number of GPU shipments is likely much larger, making this a conservative estimation.

Fig.6 shows that although performance efficiency (TFLOPS/CFP) has improved dramatically, reaching 120X of the 2016 baseline, the total CFP per chip has not increased significantly.

The addition of domain-specific accelerator blocks and features (e.g., Tensor Cores in V100, structured sparsity and reduced precisions in A100, and transformer engine in H100) improved performance significantly at a minor increase in per-chip CFP, indicating a good sustainability trend. Except for a slight decline in 2020, GPU shipments have increased annually, driven in part by the recent surge in training and deployment of LLMs. This sharp increase has led to an explosive rise in overall CO_2 emissions, now exceeding 50X of the 2016 baseline. This is a call for the community to design efficient chips and algorithms to stem the increase in CFP to keep the AI revolution healthy and green.¹

4.4 Is manufacturing cost (\$) a proxy for ECFP?

With the growing importance of measuring and reducing carbon emissions, prior work has proposed using cost as a proxy for carbon emissions. E.g., models like EIO-LCA [13] estimate carbon emissions based on the economic cost of electronics, generally converting component costs into carbon emissions. Using our dataset, we analyze the validity of this consideration. Figure 7 illustrates the variation in manufacturing cost along with ECFP. The divergence

¹The 5nm process node of H100 is actually not modeled in ECO-CHIP, but scaled based on existing process node metrics.

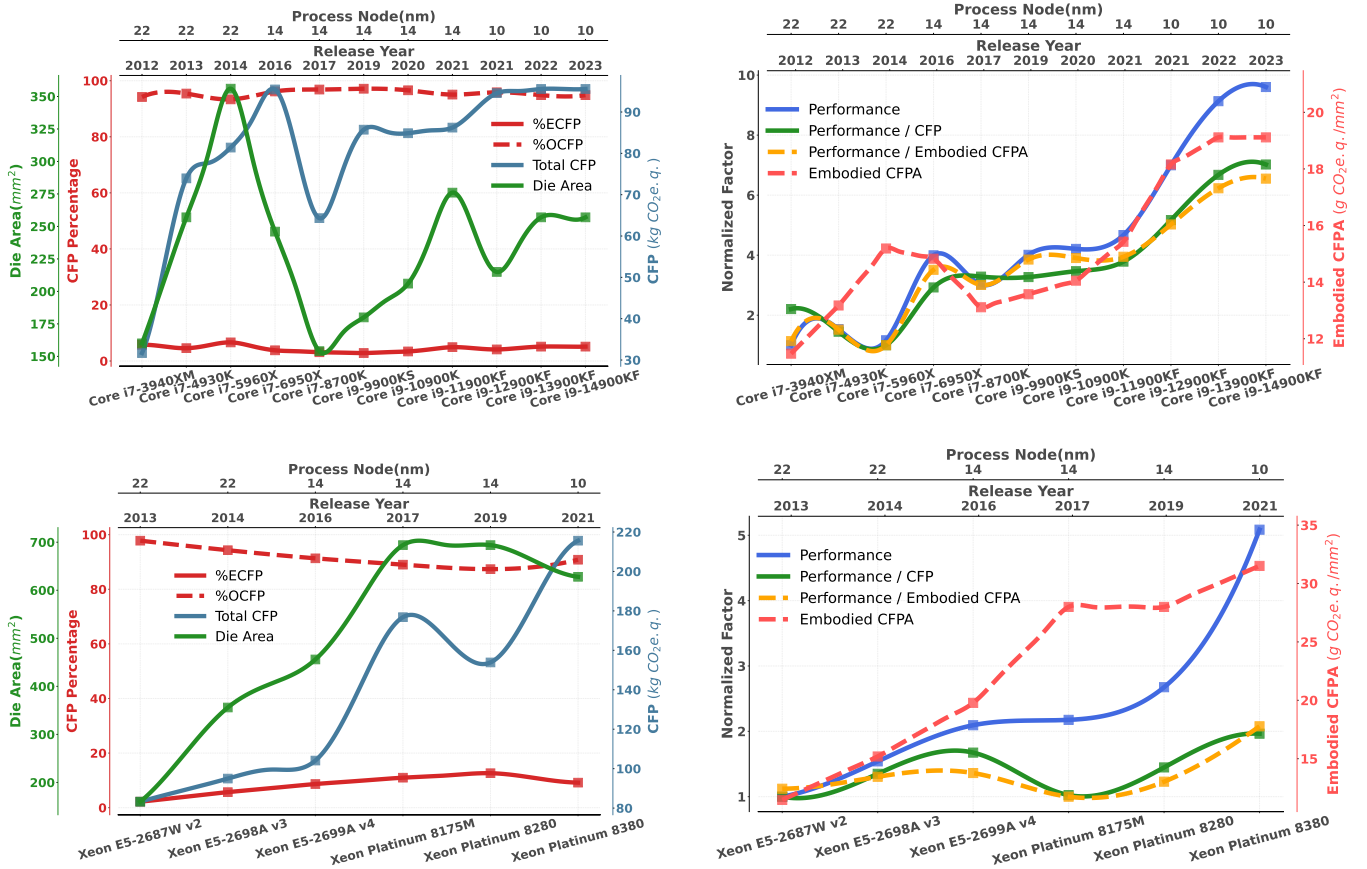


Figure 5: Sustainability trends in flagship desktop (top) and datacenter (bottom) CPUs from Intel

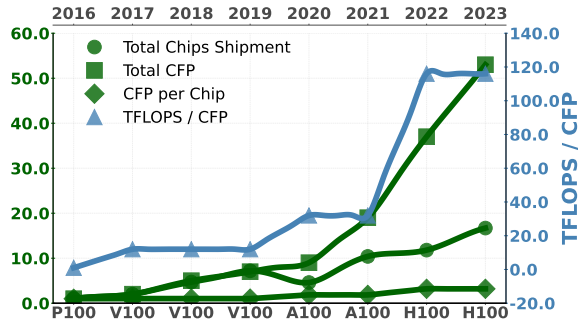


Figure 6: The AI boom greatly increased GPU shipments, raising total CFP despite the increased TFLOPS/CFP.

between these two trends becomes increasingly apparent as technology advances towards smaller nodes. This clearly demonstrates that manufacturing cost does not correlate with carbon. The plot also shows the selling price, another cost metric that could be used instead of manufacturing cost. However, we observe that it is not correlated with embodied carbon. Since the selling price includes inflation, demand, supply chain, and profit margins, it is not an ideal metric for such considerations.

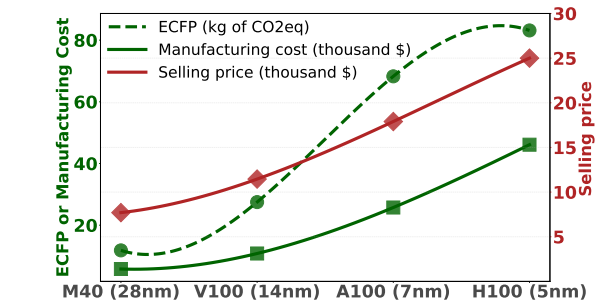


Figure 7: Manufacturing cost or selling price are not proper proxies of ECFP.

4.5 How much must processor lifetime increase by to effectively amortize ECFP?

Modern computing systems are often replaced quickly for better performance. However, extending usage helps amortize the processor's ECFP, a sunk cost, as examined in this study. Additionally, processors experience idle periods [7, 9], causing OCFP to vary significantly with utilization.

Using the NVIDIA A100-SXM GPU as an example, we analyze the impact of processor lifetime and idle time, with lifetime ranging

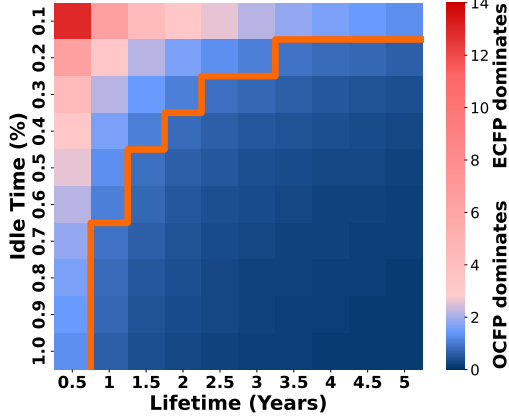


Figure 8: Ratio of ECFP to OCFP for NVIDIA A100-SXM across varying lifetime and idle time. The orange line indicates where ECFP exceeds or falls below OCFP.

from 0.5 to 5 years and idle time varying from 0% (always active) to 90% (inactive 90% of the time). Figure 8 illustrates the ECFP-to-OCFP ratio, where regions above the orange line indicate that embodied emissions outweigh operational emissions. To effectively amortize ECFP, users must either extend the device’s lifetime or reduce idle time to shift below the orange line, ensuring OCFP dominance. For instance, with 70% idle time, running the A100-SXM for more than two years enables effective ECFP amortization.

4.6 Are chiplet-based processors always more sustainable than monolithic processors?

Chiplet architecture, introduced by AMD in 2017, offers a pathway to extending Moore’s Law, but raises sustainability questions regarding yield gains versus increased area and packaging overhead. To explore this, we analyze the manufacturing CFP of AMD’s flagship chiplet CPUs over the past five years, varying chiplet counts within a fixed total chip area. Assuming an even distribution of total chip area across all chiplets, manufactured using the same process node, we also examine how manufacturing CFP scales across different chiplet configurations to assess whether chiplet architecture consistently provides a more sustainable solution. The extra packaging overhead is already modeled in our framework.

Fig.9 (top) shows the normalized manufacturing CFP of AMD chiplet CPUs to the vendor configuration in different chiplet quantities. Our analysis reveals that chiplet architecture is not always the most sustainable solution, particularly for small to medium chips. Specifically, the monolithic design yields the lowest manufacturing CFP for the Ryzen 9 series, which has the smallest chip area, while the Threadripper series benefits the most from an increased chiplet count. Additionally, for the Ryzen 9 3950X and Ryzen 9 5950X, the yield improvement from a 2-chiplet design does not sufficiently offset the overhead of a higher chiplet count, making the monolithic architecture a more sustainable choice.

Figure 9 (bottom) shows the trend of total manufacturing CFP across various chiplet configurations over a wide range of chip areas. The optimal architecture shifts with chip area, converging to designs with higher chiplet counts beyond a certain threshold.

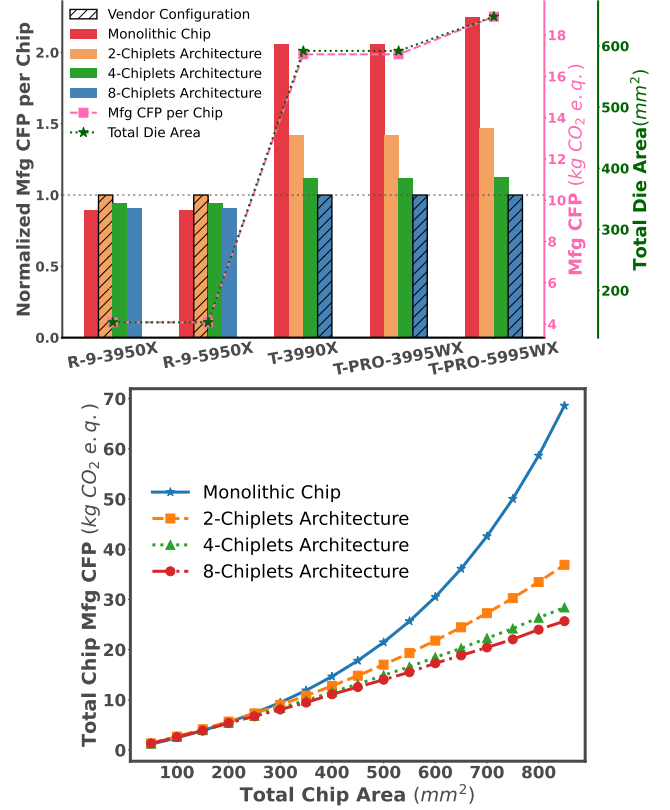


Figure 9: Manufacturing CFP of AMD flagship chiplet CPUs (top) and monolithic, 2, 4, and 8 Chiplets architectures with total chip area scaled from 50 to 850 mm^2 (bottom) all at 7nm. R=Ryzen, T=Threadripper. While more chiplets reduce CFP as area increases, monolithic architecture remains the most sustainable for chips under 200 mm^2

For chips smaller than 200 mm^2 , monolithic architecture remains the most sustainable, while for those exceeding 300 mm^2 a higher chiplet count leads to better sustainability.

In practice, sustainability is not the primary driver for adopting chiplet-based designs; instead, they offer advantages in efficiency, testability, and manufacturing cost. Despite higher carbon emissions, performance remains the priority. For the Ryzen 9 series, while the 2-chiplet architecture is the least sustainable, its manufacturing CFP is comparable to other configurations. Its superior performance and efficiency, combined with lower manufacturing cost and better testability than higher chiplet-count designs, make it a balanced trade-off.

5 POTENTIAL IMPACT OF CARBONSET

CarbonSet benchmarks processor sustainability by analyzing CFP trends over time, aiding carbon reduction and sustainable design. We showcased this through trend analysis and case studies but note its broader applicability, including:

- *Life cycle assessment (LCA)*: Our dataset enables companies to estimate device lifetime CFP for LCA, supporting corporate sustainability reports and eco-labeling for consumer awareness.

- *Optimizing designs and technology*: Historical data reveals which design aspects (e.g., manufacturing, materials, efficiency) have the highest carbon impact, guiding emissions-reducing optimizations for future processors.
- *Environmental policy and standardization*: Governments and industries can use this dataset to set carbon benchmarks, shape regulations, and incentivize low-carbon designs.
- *Education and carbon awareness*: It can support academic and industrial research focused on environmental sustainability. It can also impact consumer purchasing decisions and help create a carbon-aware mindset.

6 CONCLUSION

In this paper, we introduced CarboSet, a dataset designed for analyzing processor sustainability trends and enhancing sustainability-driven design evaluation. By leveraging this dataset, we examine key aspects of processor sustainability, including overall design trends over the past decade, the impact of the AI boom, the reliability of approximating ECFP using manufacturing costs, the required operational lifetime for effective ECFP amortization, and the sustainability implications of chiplet architectures. CarbonSet aims to guide environmentally conscious decisions in processor design, manufacturing, and lifecycle management.

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